SLG7RN45314

GreenPAK ™

RZ/G2L SMARC Boot Mode

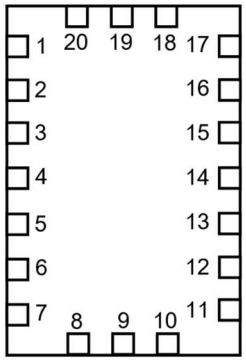
General Description

Renesas SLG7RN45314 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Pin Configuration



STQFN-20
(Top View)

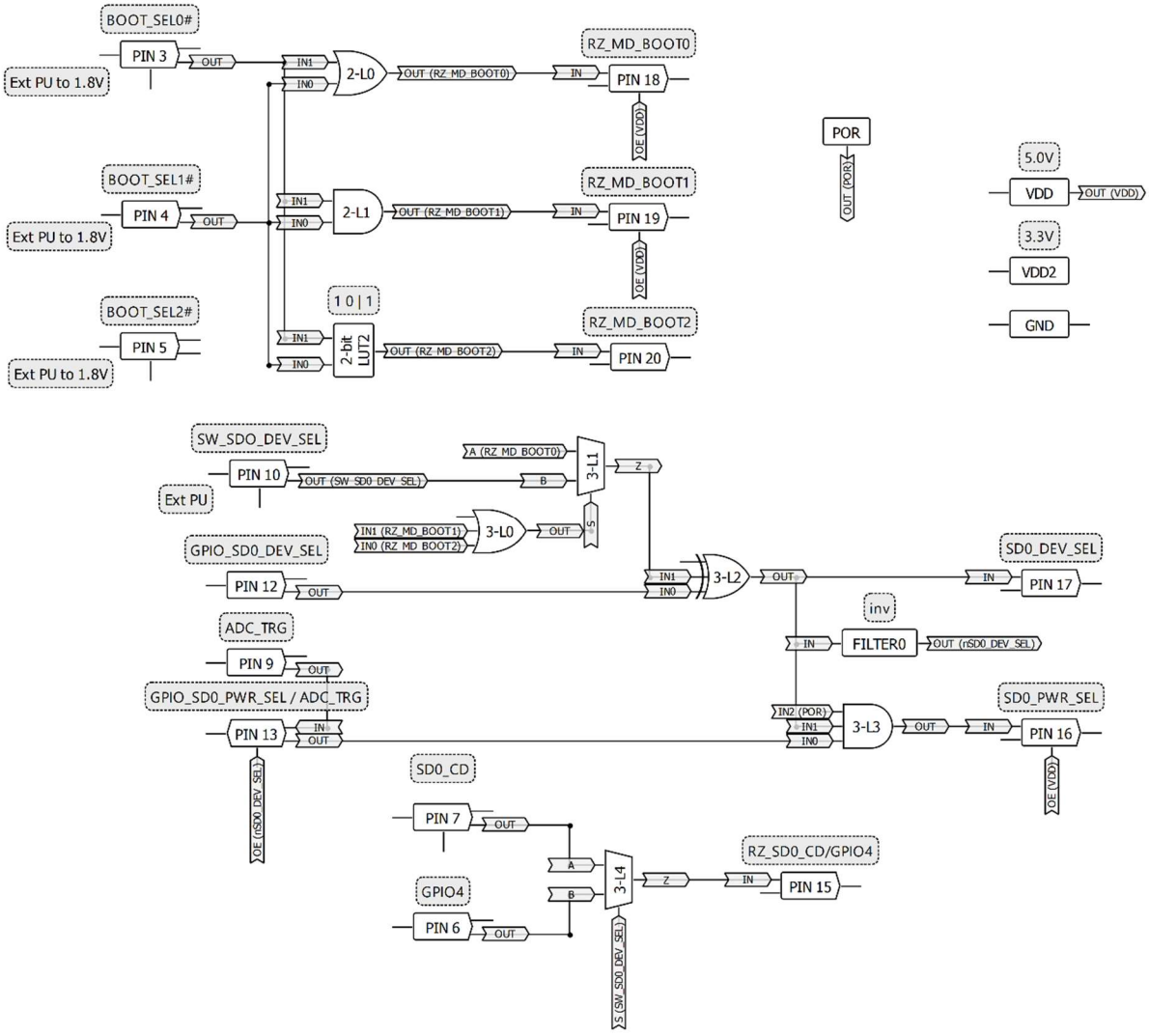
Output Summary

7 Outputs - Push Pull 1X

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	NC	12	GPIO_SD0_DEV_SEL
3	BOOT_SEL0#	13	GPIO_SD0_PWR_SEL / ADC_TRG
4	BOOT_SEL1#	14	VDD2
5	BOOT_SEL2#	15	RZ_SD0_CD/GPIO4
6	GPIO4	16	SD0_PWR_SEL
7	SD0_CD	17	SD0_DEV_SEL
8	NC	18	RZ_MD_BOOT0
9	ADC_TRG	19	RZ_MD_BOOT1
10	SW_SD0_DEV_SEL	20	RZ_MD_BOOT2

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	BOOT_SEL0#	Digital Input	Low Voltage Digital Input	floating
4	BOOT_SEL1#	Digital Input	Low Voltage Digital Input	floating
5	BOOT_SEL2#	Digital Input	Low Voltage Digital Input	floating
6	GPIO4	Digital Input	Low Voltage Digital Input	floating
7	SD0_CD	Digital Input	Low Voltage Digital Input	floating
8	NC	--	Keep Floating or Connect to GND	--
9	ADC_TRG	Digital Input	Low Voltage Digital Input	floating
10	SW_SD0_DEV_SEL	Digital Input	Low Voltage Digital Input	floating
11	GND	GND	Ground	--
12	GPIO_SD0_DEV_SEL	Digital Input	Digital Input with Schmitt trigger	10kΩ pullup
13	GPIO_SD0_PWR_SEL / ADC_TRG	Bi-directional	Digital Input with Schmitt trigger / Push Pull 1X	10kΩ pullup
14	VDD2	PWR	Supply Voltage	--
15	RZ_SD0_CD/GPIO4	Digital Output	Push Pull 1X	floating
16	SD0_PWR_SEL	Digital Output	Push Pull 1X	floating
17	SD0_DEV_SEL	Digital Output	Push Pull 1X	floating
18	RZ_MD_BOOT0	Digital Output	Push Pull 1X	floating
19	RZ_MD_BOOT1	Digital Output	Push Pull 1X	floating
20	RZ_MD_BOOT2	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN45314V	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	PINs 2, 3, 4, 5, 6, 7, 8, 9, 10	GND - 0.5	VDD + 0.5	V
	PINs 12, 13, 15, 16, 17, 18, 19, 20		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.7	5	5.5	V
V_{DD2}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	VDD = VDD2 = 5.5V; All Inputs LOW except PIN12 and PIN13	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_{IH}	HIGH-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Low-Level Logic Input at VDD=5.0V	1.15	--	VDD	V
V_{IH2}	HIGH-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Logic Input with Schmitt Trigger at VDD2=3.3V	2.14	--	VDD	V
V_{IL}	LOW-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Low-Level Logic Input at VDD=5.0V	0	--	0.77	V
V_{IL2}	LOW-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Logic Input with Schmitt Trigger at VDD2=3.3V	0	--	0.97	V
V_{OH2}	HIGH-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OH}=3mA at VDD2=3.3V	2.74	3.12	--	V
V_{OL2}	LOW-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OL}=3mA at VDD2=3.3V	--	0.13	0.23	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OH}=2.4V at VDD2=3.3V	6.05	12.08	--	mA

I_{OL2}	LOW-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OL}=0.4V at VDD2=3.3V	4.88	8.24	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 12, 13	--	10	--	kΩ
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.61	1.24	1.65	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, PINs 12, 13, 15, 16, 17, 18, 19, and 20 to another.
3. Guaranteed by Design.

Description

The table below shows the logic for the RZ_MD_BOOT# outputs.

Table 1: RZ_MD_BOOT# Logic

BOOT_SEL0#	BOOT_SEL1#	RZ_MD_BOOT0 (OR)	RZ_MD_BOOT1 (AND)	RZ_MD_BOOT2
0	0	0	0	0
0	1	1	0	0
1	0	1	0	1
1	1	1	1	0

Table 2 shows the internal logic for the SD0_DEV_SEL output. The first column is a logical OR operation of the RZ_MD_BOOT1 and RZ_MD_BOOT2 logic signals. This OR'ed signal acts as a MUX select for the RZ_MD_BOOT0 and SW_SD0_DEV_SEL signals. This MUX output is then XOR'ed with the GPIO_SD0_DEV_SEL input to produce the SD0_DEV_SEL output.

Table 2: SD0_DEV_SEL Logic

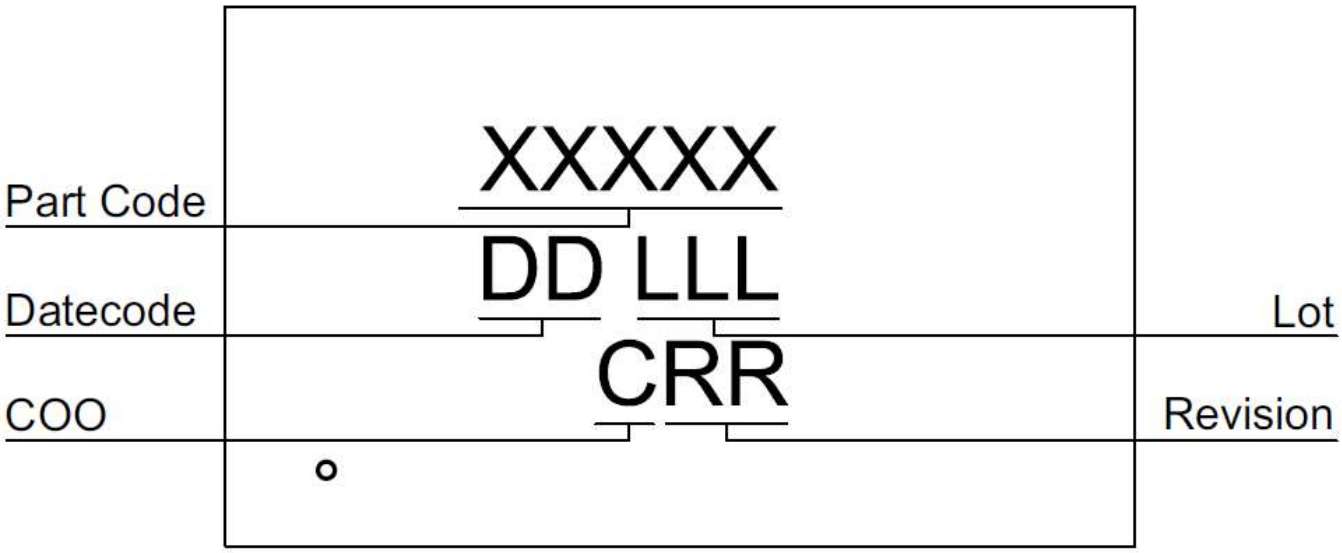
RZ_MD_BOOT1 || RZ_MD_BOOT2	RZ_MD_BOOT0	SW_SD0_DEV_SEL	GPIO_SD0_DEV_SEL	SD0_DEV_SEL
0	0	X	0	0
	0	X	1	1
	1	X	0	1
	1	X	1	0
1	X	0	0	0
	X	0	1	1
	X	1	0	1
	X	1	1	0

To generate the SD0_PWR_SEL output, this GreenPAK design performs a logical AND on the SD0_DEV_SEL and GPIO_SD0_PWR_SEL / ADC_TRIG signals.

Table 3: SD0_PWR_SEL Logic

SD0_DEV_SEL	GPIO_SD0_PWR_SEL / ADC_TRIG	SD0_PWR_SEL (AND)
0	0	0
0	1	0
1	0	0
1	1	1

Package Top Marking



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.15	003	U	0x51BACCF1	45314	AB	07/11/2023

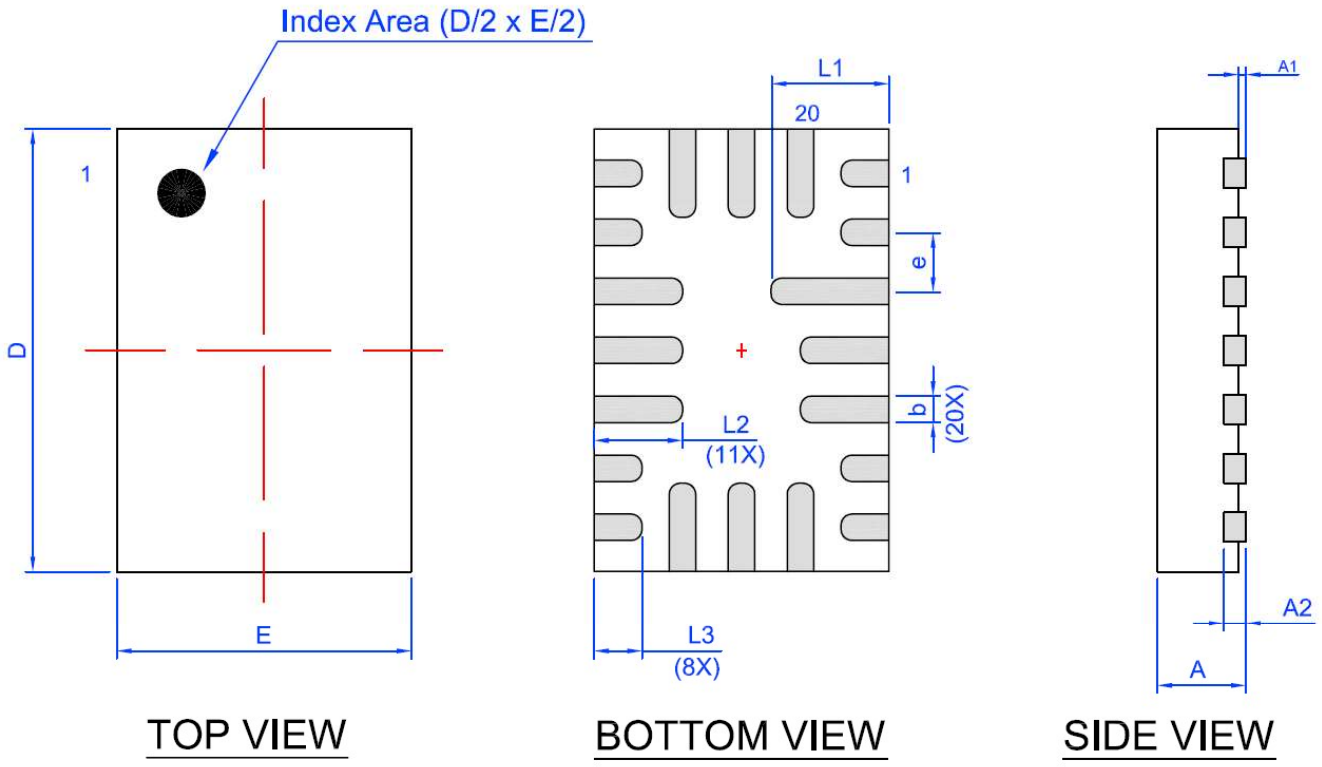
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220



TOP VIEW BOTTOM VIEW SIDE VIEW

Unit: mm

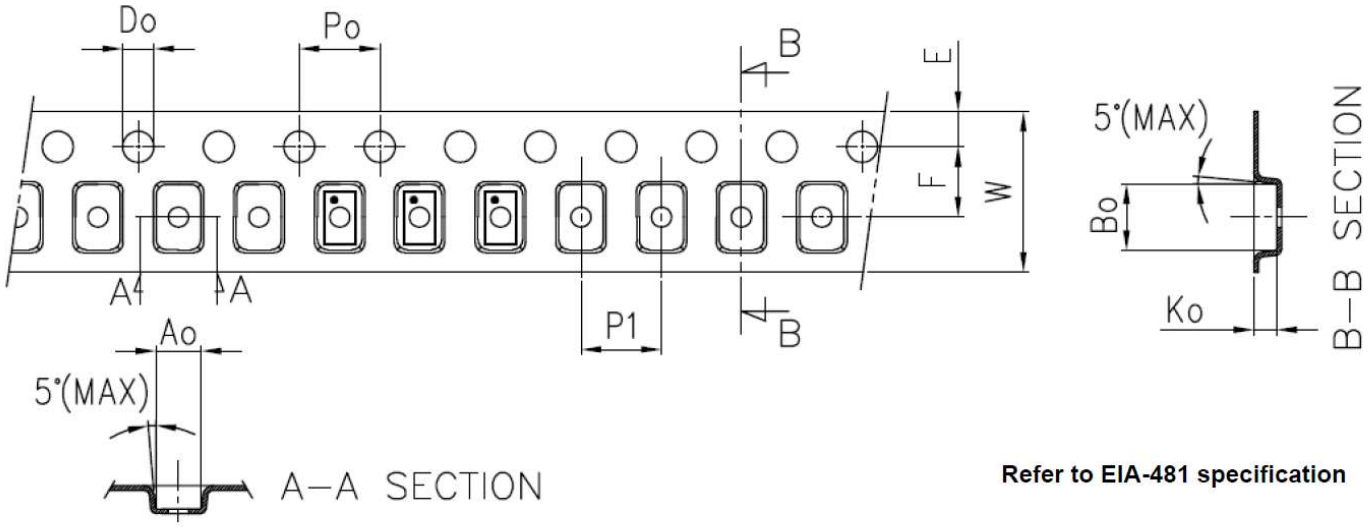
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P COL	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

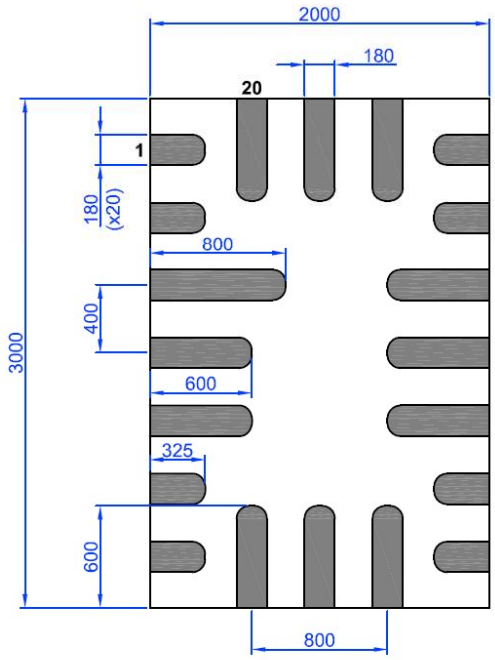
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

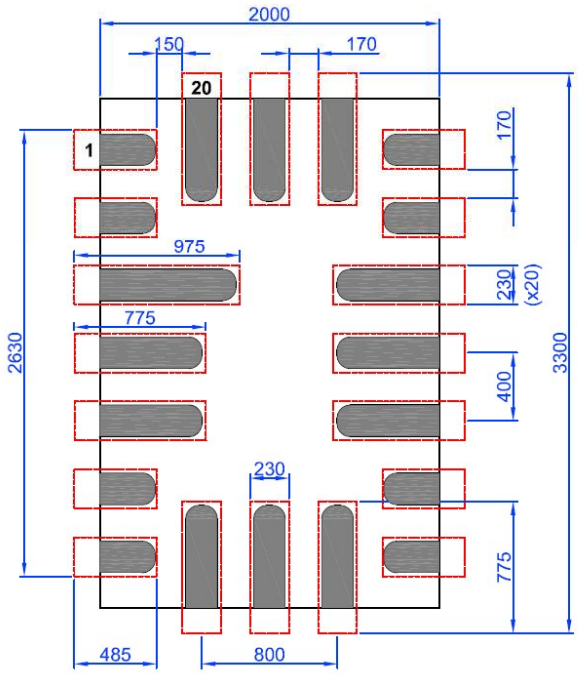
Recommended Land Pattern

Exposed Pad
(Top View)

Recommended Land Pattern
(Top View)

Units: µm





Datasheet Revision History

Date	Version	Change
10/13/2021	0.10	New design for SLG46538V chip
11/17/2021	0.11	Added RZ_SD0_CDD/GPIO4 MUX, Modified Pinout
12/02/2021	0.12	Updated Device Revision Table
12/13/2021	0.13	Updated PIN16 GPIO Structure
12/15/2021	0.14	Updated Device Revision Table
07/11/2023	0.15	Moved to Renesas template

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