

General Description

Renesas SLG7RN45315 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

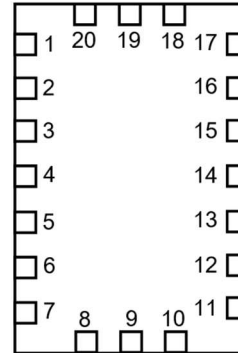
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

2 Outputs - Open Drain NMOS 1X
 2 Outputs - Open Drain NMOS 2X
 2 Outputs - Push Pull 1X
 2 Outputs - Push Pull 2X

Pin Configuration

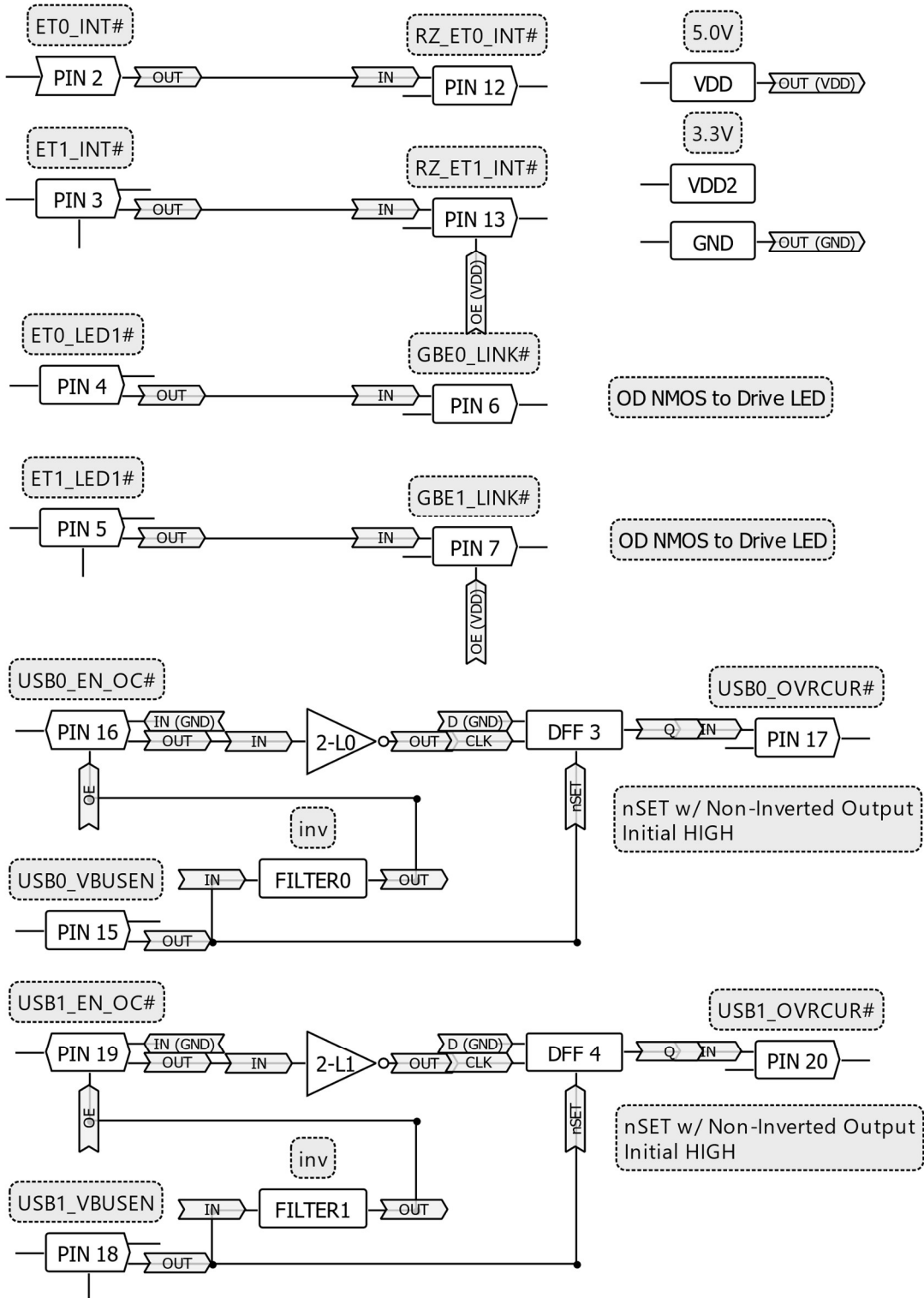


**STQFN-20
(Top View)**

Pin name

| Pin # | Pin name | Pin # | Pin name |
|-------|------------|-------|--------------|
| 1 | VDD | 11 | GND |
| 2 | ET0_INT# | 12 | RZ_ET0_INT# |
| 3 | ET1_INT# | 13 | RZ_ET1_INT# |
| 4 | ET0_LED1# | 14 | VDD2 |
| 5 | ET1_LED1# | 15 | USB0_VBUSEN |
| 6 | GBE0_LINK# | 16 | USB0_EN_OC# |
| 7 | GBE1_LINK# | 17 | USB0_OVRCUR# |
| 8 | NC | 18 | USB1_VBUSEN |
| 9 | NC | 19 | USB1_EN_OC# |
| 10 | NC | 20 | USB1_OVRCUR# |

Block Diagram



Pin Configuration

| Pin # | Pin Name | Type | Pin Description | Internal Resistor |
|-------|--------------|----------------|--|-------------------|
| 1 | VDD | PWR | Supply Voltage | -- |
| 2 | ET0_INT# | Digital Input | Low Voltage Digital Input | floating |
| 3 | ET1_INT# | Digital Input | Low Voltage Digital Input | floating |
| 4 | ET0_LED1# | Digital Input | Low Voltage Digital Input | floating |
| 5 | ET1_LED1# | Digital Input | Low Voltage Digital Input | floating |
| 6 | GBE0_LINK# | Digital Output | Open Drain NMOS 2X | floating |
| 7 | GBE1_LINK# | Digital Output | Open Drain NMOS 2X | floating |
| 8 | NC | -- | Keep Floating or Connect to GND | -- |
| 9 | NC | -- | Keep Floating or Connect to GND | -- |
| 10 | NC | -- | Keep Floating or Connect to GND | -- |
| 11 | GND | GND | Ground | -- |
| 12 | RZ_ET0_INT# | Digital Output | Push Pull 2X | floating |
| 13 | RZ_ET1_INT# | Digital Output | Push Pull 2X | floating |
| 14 | VDD2 | PWR | Supply Voltage | -- |
| 15 | USB0_VBUSEN | Digital Input | Digital Input with Schmitt trigger | floating |
| 16 | USB0_EN_OC# | Bi-directional | Digital Input with Schmitt trigger / Open Drain NMOS 1X | 10kΩ pullup |
| 17 | USB0_OVRCUR# | Digital Output | Push Pull 1X | floating |
| 18 | USB1_VBUSEN | Digital Input | Digital Input with Schmitt trigger | floating |
| 19 | USB1_EN_OC# | Bi-directional | Digital Input with Schmitt trigger / Open Drain NMOS 1X | 10kΩ pullup |
| 20 | USB1_OVRCUR# | Digital Output | Push Pull 1X | floating |

Ordering Information

| Part Number | Package Type |
|--------------|---|
| SLG7RN45315V | 20-pin STQFN - Tape and Reel (3k units) |

Absolute Maximum Conditions

| Parameter | | Min. | Max. | Unit |
|---|-------------------------------------|-----------|------------|------|
| Supply Voltage on VDD relative to GND | | -0.5 | 7 | V |
| Supply voltage on VDD2 relative to GND | | -0.5 | VDD + 0.5 | V |
| DC Input voltage | PINs 2, 3, 4, 5, 6, 7, 8, 9, 10 | GND - 0.5 | VDD + 0.5 | V |
| | PINs 12, 13, 15, 16, 17, 18, 19, 20 | | VDD2 + 0.5 | |
| Maximum Average or DC Current (Through pin) | Push-Pull 1x | -- | 11 | mA |
| | Push-Pull 2x | -- | 16 | |
| | OD 1x | -- | 11 | |
| | OD 2x | -- | 21 | |
| Current at Input Pin | | -1.0 | 1.0 | mA |
| Input leakage (Absolute Value) | | -- | 1000 | nA |
| Storage Temperature Range | | -65 | 150 | °C |
| Junction Temperature | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | 2000 | -- | V |
| ESD Protection (Charged Device Model) | | 500 | -- | V |
| Moisture Sensitivity Level | | 1 | | |

Electrical Characteristics

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|------------------|---|---|------|------|------|------|
| V _{DD} | Supply Voltage | | 4.7 | 5 | 5.5 | V |
| V _{DD2} | Supply Voltage | | 3 | 3.3 | 3.6 | V |
| T _A | Operating Temperature | | -40 | 25 | 85 | °C |
| C _{VDD} | Capacitor Value at VDD | | -- | 0.1 | -- | µF |
| C _{IN} | Input Capacitance | | -- | 4 | -- | pF |
| I _Q | Quiescent Current | Static inputs and floating outputs. PINs 15 and 18 are HIGH. PINs 2, 3, 4, 5 are LOW. | -- | 1.2 | -- | µA |
| V _O | Maximal Voltage Applied to any PIN in High-Impedance State | | -- | -- | VDD | V |
| I _{VDD} | Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 45 | mA |
| | | T _J = 110°C | -- | -- | 22 | mA |
| I _{GND} | Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2) | T _J = 85°C | -- | -- | 86 | mA |
| | | T _J = 110°C | -- | -- | 41 | mA |
| V _{IH} | HIGH-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 | Low-Level Logic Input at VDD=5.0V | 1.15 | -- | VDD | V |
| V _{IH2} | HIGH-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20 | Logic Input with Schmitt Trigger at VDD2=3.3V | 2.14 | -- | VDD | V |
| V _{IL} | LOW-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 | Low-Level Logic Input at VDD=5.0V | 0 | -- | 0.77 | V |
| V _{IL2} | LOW-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20 | Logic Input with Schmitt Trigger at VDD2=3.3V | 0 | -- | 0.97 | V |
| V _{OH2} | HIGH-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20 | Push-Pull 1X, I _{OH} =3mA at VDD2=3.3V | 2.74 | 3.12 | -- | V |

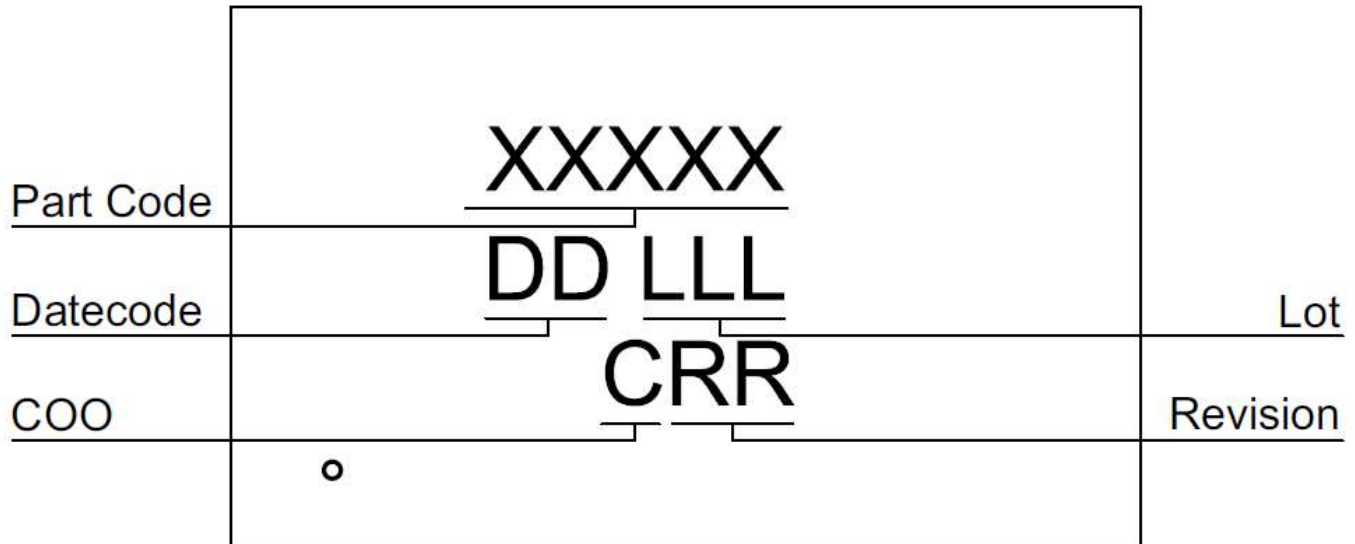
RZ/G2I SMARC USB / Ethernet Logic

| | | | | | | |
|----------------|--|---|-------|-------|------|------------|
| | | Push-Pull 2X, $I_{OH}=3\text{mA}$ at $V_{DD2}=3.3\text{V}$ | 2.87 | 3.21 | -- | V |
| V_{OL} | LOW-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 | Open Drain NMOS 2X, $I_{OL}=5\text{mA}$ at $V_{DD}=5.0\text{V}$ | -- | 0.07 | 0.08 | V |
| V_{OL2} | LOW-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20 | Push-Pull 1X, $I_{OL}=3\text{mA}$ at $V_{DD2}=3.3\text{V}$ | -- | 0.13 | 0.23 | V |
| | | Push-Pull 2X, $I_{OL}=3\text{mA}$ at $V_{DD2}=3.3\text{V}$ | -- | 0.06 | 0.11 | V |
| | | Open Drain NMOS 1X, $I_{OL}=3\text{mA}$ at $V_{DD2}=3.3\text{V}$ | -- | 0.08 | 0.15 | V |
| I_{OH2} | HIGH-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20 | Push-Pull 1X, $V_{OH}=2.4\text{V}$ at $V_{DD2}=3.3\text{V}$ | 6.05 | 12.08 | -- | mA |
| | | Push-Pull 2X, $V_{OH}=2.4\text{V}$ at $V_{DD2}=3.3\text{V}$ | 11.54 | 24.16 | -- | mA |
| I_{OL} | LOW-Level Output Current (see Note 1) PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 | Open Drain NMOS 2X, $V_{OL}=0.4\text{V}$ at $V_{DD}=5.0\text{V}$ | 17.34 | 34.76 | -- | mA |
| I_{OL2} | LOW-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20 | Push-Pull 1X, $V_{OL}=0.4\text{V}$ at $V_{DD2}=3.3\text{V}$ | 4.88 | 8.24 | -- | mA |
| | | Push-Pull 2X, $V_{OL}=0.4\text{V}$ at $V_{DD2}=3.3\text{V}$ | 9.75 | 16.49 | -- | mA |
| | | Open Drain NMOS 1X, $V_{OL}=0.4\text{V}$ at $V_{DD2}=3.3\text{V}$ | 7.31 | 12.37 | -- | mA |
| R_{PULL_UP} | Internal Pull Up Resistance | Pull up on PINs 16, 19 | -- | 10 | -- | k Ω |
| T_{SU} | Startup Time | From V_{DD} rising past PON_{THR} | 0.61 | 1.24 | 1.65 | ms |
| PON_{THR} | Power On Threshold | V_{DD} Level Required to Start Up the Chip | 1.41 | 1.54 | 1.66 | V |
| $POFF_{THR}$ | Power Off Threshold | V_{DD} Level Required to Switch Off the Chip | 1.00 | 1.15 | 1.31 | V |

Note:

- DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
- The GreenPAK's power rails are divided in two sides. PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, PINs 12, 13, 15, 16, 17, 18, 19, and 20 to another.
- Guaranteed by Design.

Package Top Marking



- XXXXX – Part ID Field: identifies the specific device configuration
- DD – Date Code Field: Coded date of manufacture
- LLL – Lot Code: Designates Lot #
- C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR – Revision Code: Device Revision

| Datasheet Revision | Programming Code Number | Lock Status | Checksum | Part Code | Revision | Date |
|--------------------|-------------------------|-------------|------------|-----------|----------|------------|
| 0.13 | 002 | U | 0xD1CEC92D | 45315 | AA | 07/12/2023 |

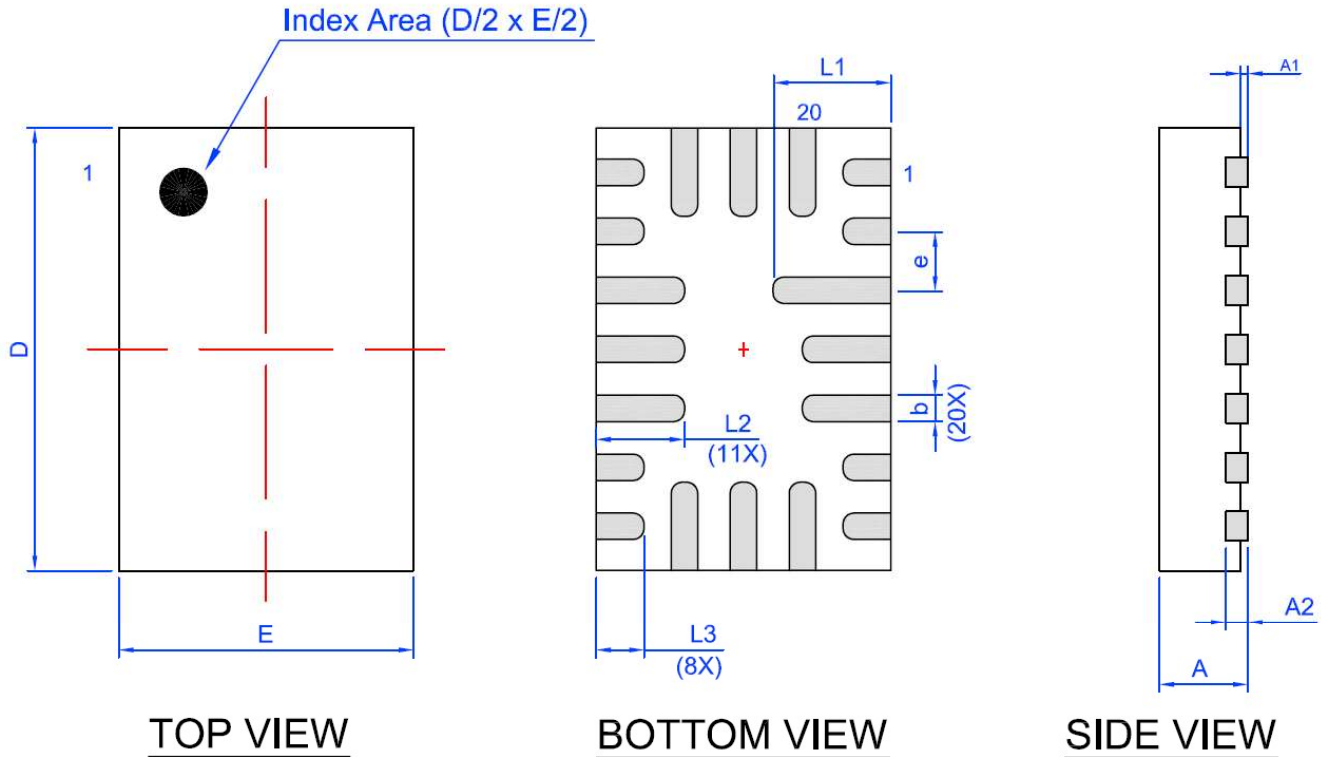
Lock coverage for this part is indicated by \checkmark , from one of the following options:

| | |
|--------------|---|
| \checkmark | Unlocked |
| | Locked for read, bits <1535:0> |
| | Locked for write, bits <1535:0> |
| | Locked for write all bits |
| | Locked for read and write bits <1535:0> |
| | Locked for read bits <1535:0> and write of all bits |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220



Unit: mm

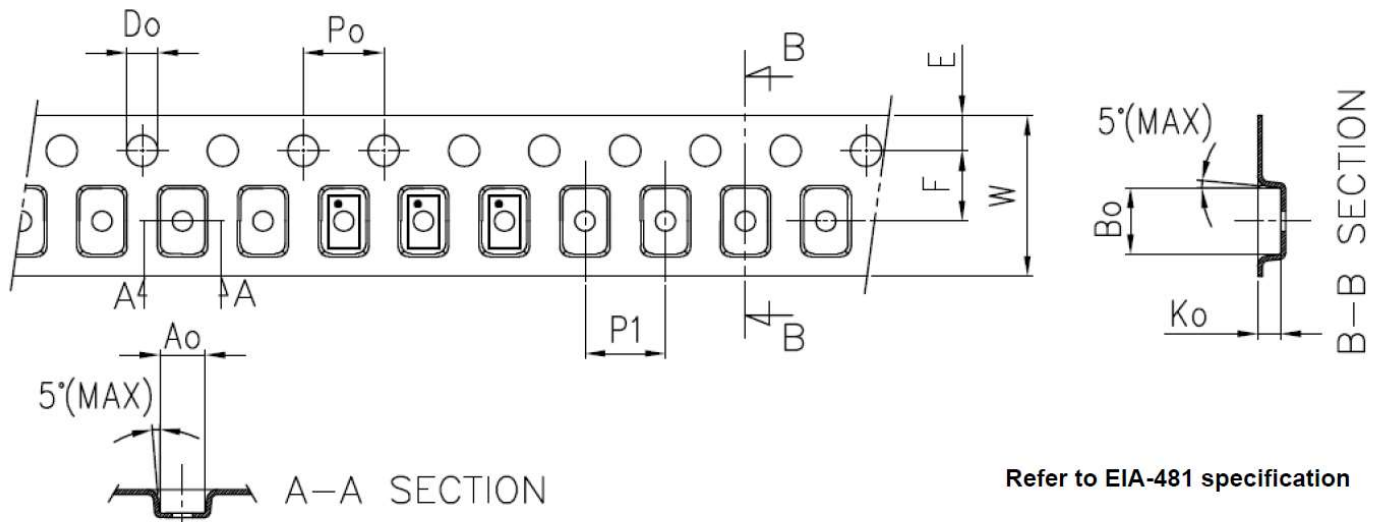
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|-------|--------|-------|-------|-------|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.050 | E | 1.95 | 2.00 | 2.05 |
| A2 | 0.10 | 0.15 | 0.20 | L1 | 0.75 | 0.80 | 0.85 |
| b | 0.13 | 0.18 | 0.23 | L2 | 0.55 | 0.60 | 0.65 |
| e | 0.40 BSC | | | L3 | 0.275 | 0.325 | 0.375 |

Tape and Reel Specification

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|--------------------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 20L 2x3mm 0.4P COL | 20 | 2x3x0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|------------------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 20L 2x3 mm 0.4P COL | 2.2 | 3.15 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |




Recommended Reflow Soldering Profile

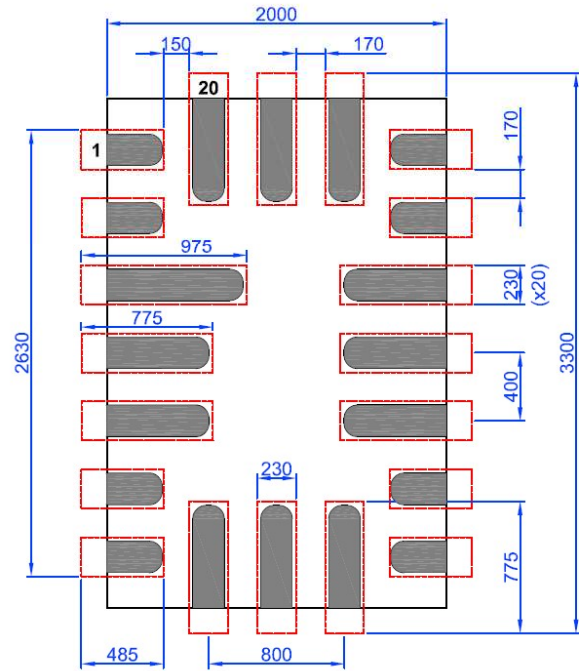
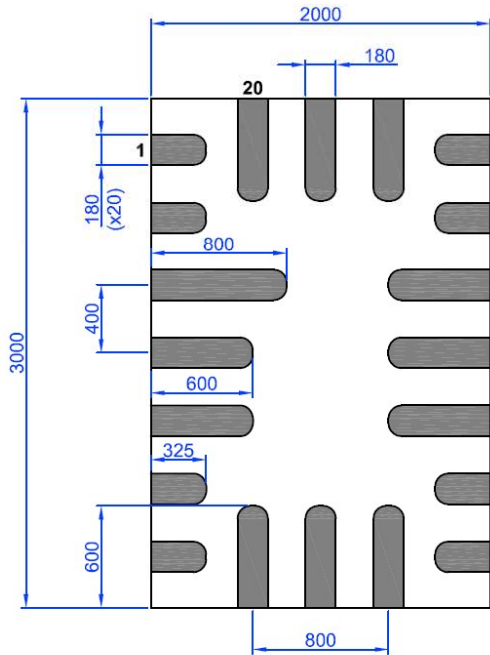
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm³ (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

 Exposed Pad
(Top View)

 Recommended Land Pattern
(Top View)

Units: μm



Datasheet Revision History

| Date | Version | Change |
|------------|---------|-------------------------------|
| 10/13/2021 | 0.10 | New design for SLG46538V chip |
| 10/29/2021 | 0.11 | Updated some logic |
| 12/02/2021 | 0.12 | Updated Device Revision Table |
| 07/12/2023 | 0.13 | Moved to Renesas template |

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