General Description

Renesas SLG7RN45336 is a low power and small form device. The SoC is housed in a 1.6mm x 1.6mm STQFN package which is optimal for using with small devices.

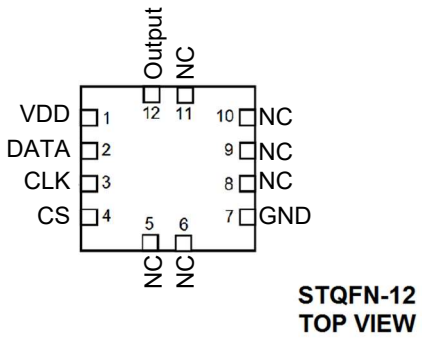
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package

Output Summary

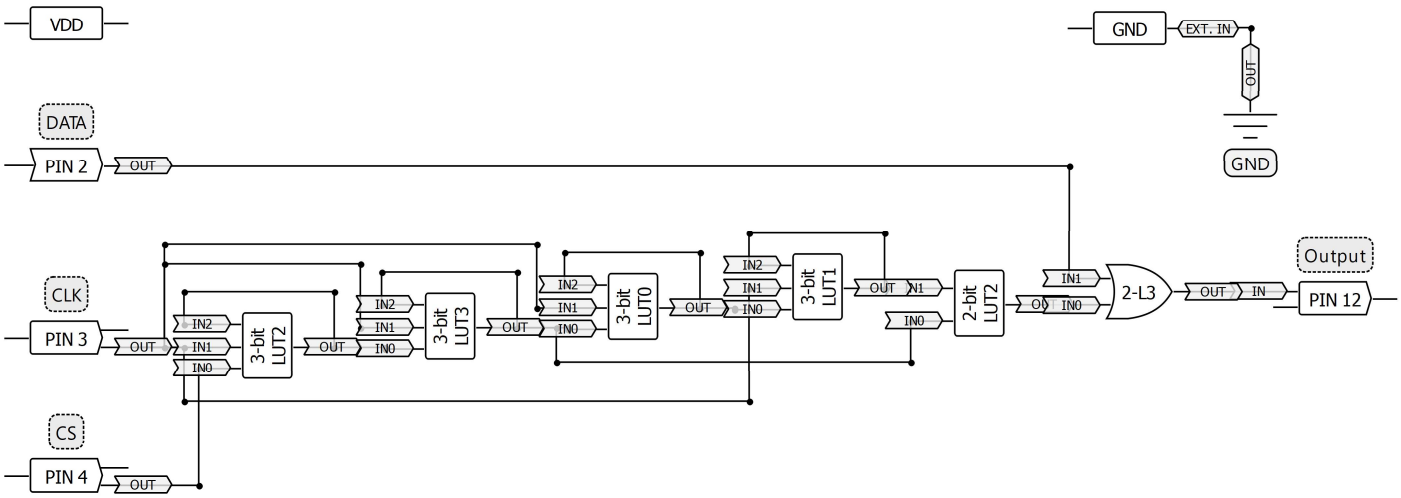
1 Output - Push Pull 1X

Pin Configuration



STQFN-12
TOP VIEW

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	DATA	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	CLK	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
4	CS	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
5	NC	--	Keep Floating or Connect to GND	--
6	NC	--	Keep Floating or Connect to GND	--
7	GND	GND	Ground	--
8	NC	--	Keep Floating or Connect to GND	--
9	NC	--	Keep Floating or Connect to GND	--
10	NC	--	Keep Floating or Connect to GND	--
11	NC	--	Keep Floating or Connect to GND	--
12	Output	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN45336V	STQFN-12 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

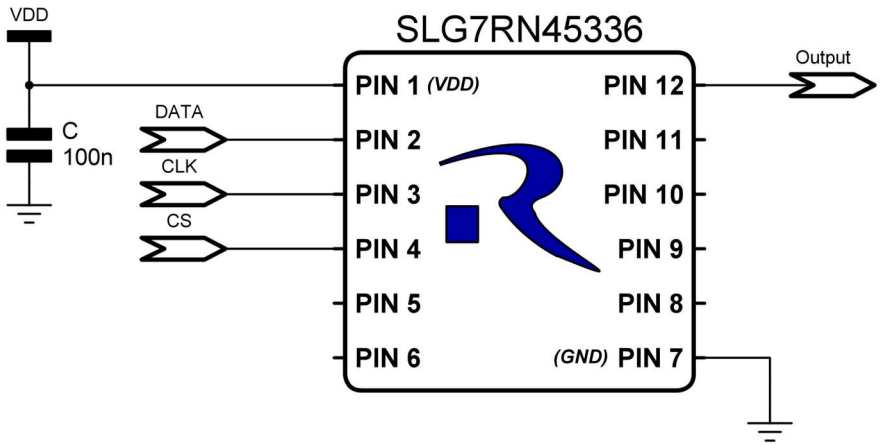
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.3	5	5.2	V
T_A	Operating Temperature		20	25	30	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	1.78	--	VDD	V
		Logic Input at VDD=5.0V	2.64	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	0	--	1.21	V
		Logic Input at VDD=5.0V	0	--	1.84	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=3mA, at VDD=3.3V	2.71	3.09	--	V
		Push-Pull 1X, Open Drain PMOS 1X, I_{OH}=5mA, at VDD=5.0V	4.15	4.73	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	0.18	0.28	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	0.23	0.33	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=2.4V, at VDD=3.3V	5.83	10.18	--	mA

		Push-Pull 1X, Open Drain PMOS 1X, V_{OH}=2.4V, at VDD=5.0V	21.808	29.1	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.06	6.44	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	6.01	9.73	--	mA
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 3, 4	--	1	--	MΩ
T_{SU}	Startup Time	From VDD rising past 1.35 V	--	0.27	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.11	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.
3. Guaranteed by Design.

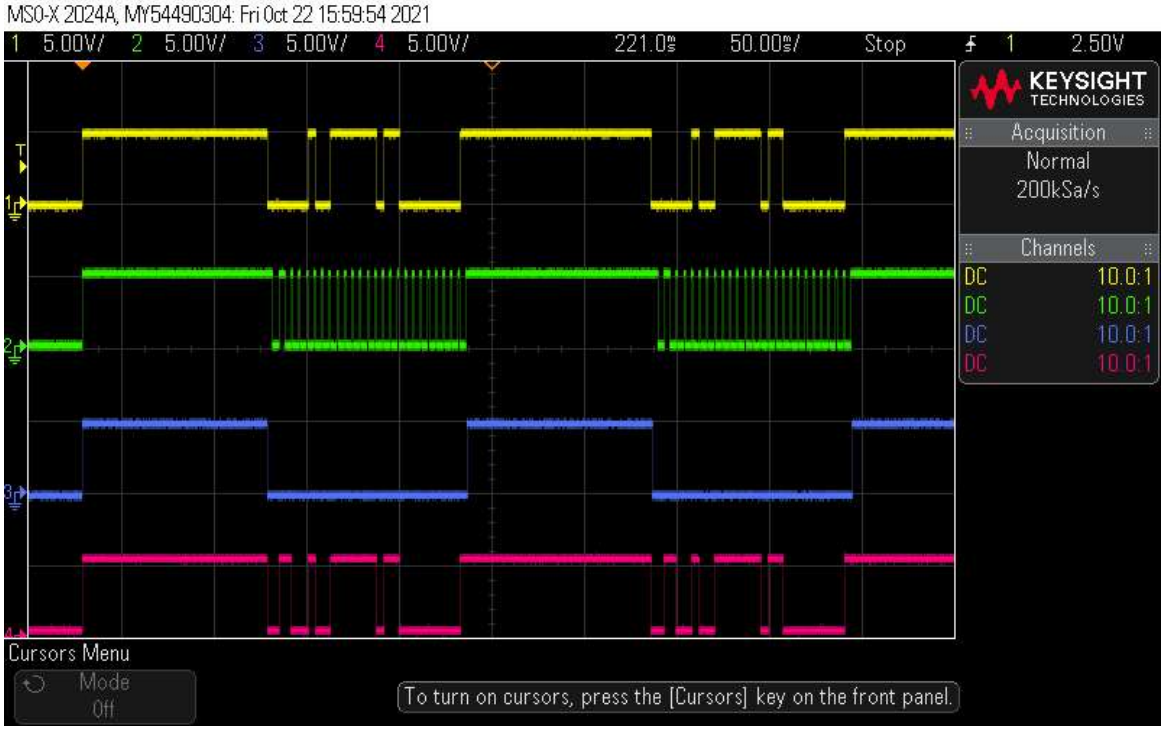
Typical Application Circuit



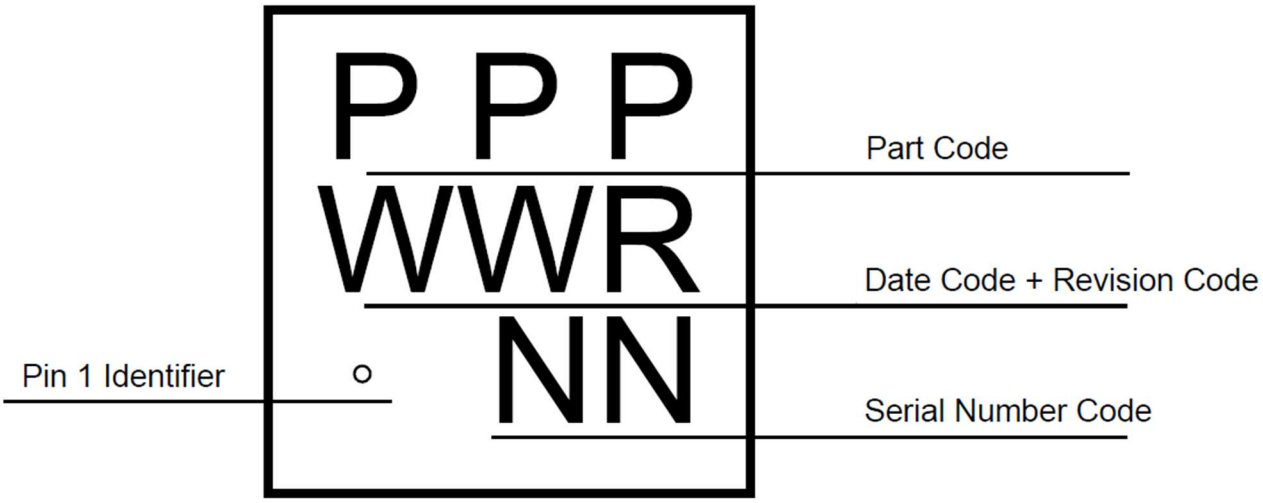
Functionality Waveforms

Channel 1 (yellow/top line) – PIN# 2 (DATA)
Channel 2 (light blue/2nd line) – PIN# 3 (CLK)
Channel 3 (magenta/3rd line) – PIN# 4 (CS)
Channel 4 (blue/bottom line) – PIN# 12 (Output)

Figure1. Chip functionality



Package Top Marking

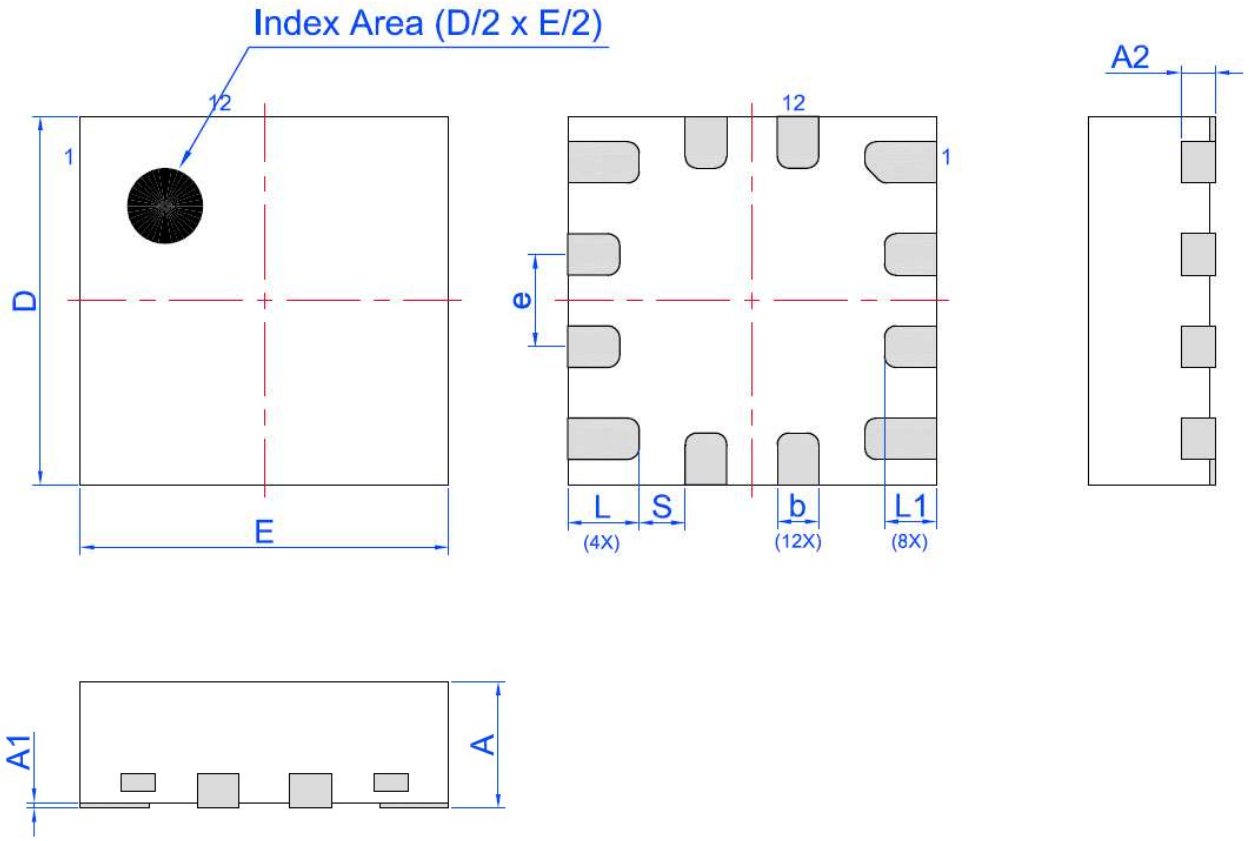


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0xE748DE4E			07/11/2023

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

12 Lead STQFN FC Package 1.6 x 1.6 mm
IC net weight: 0.0028 g



Unit: mm

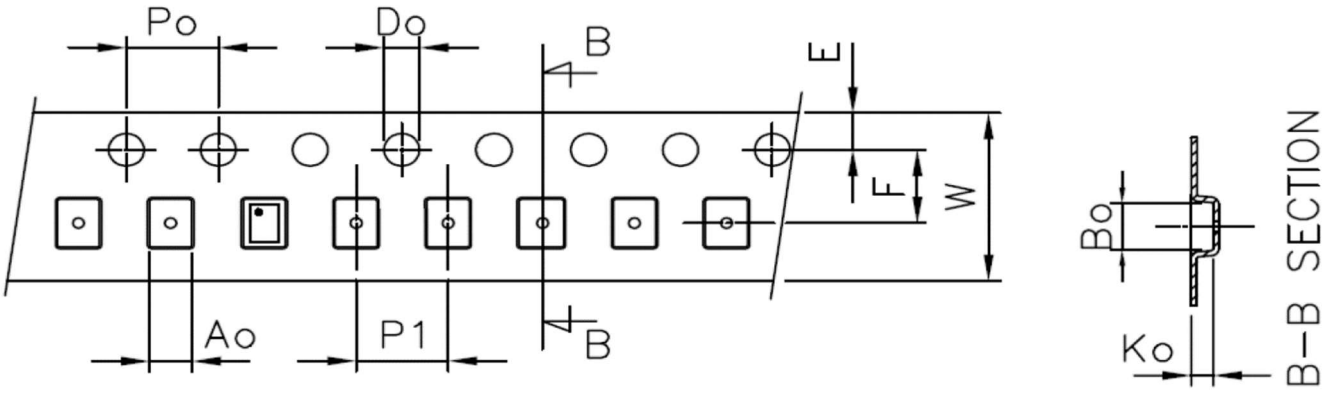
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FC 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.8±0.05	1.8±0.05	±0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

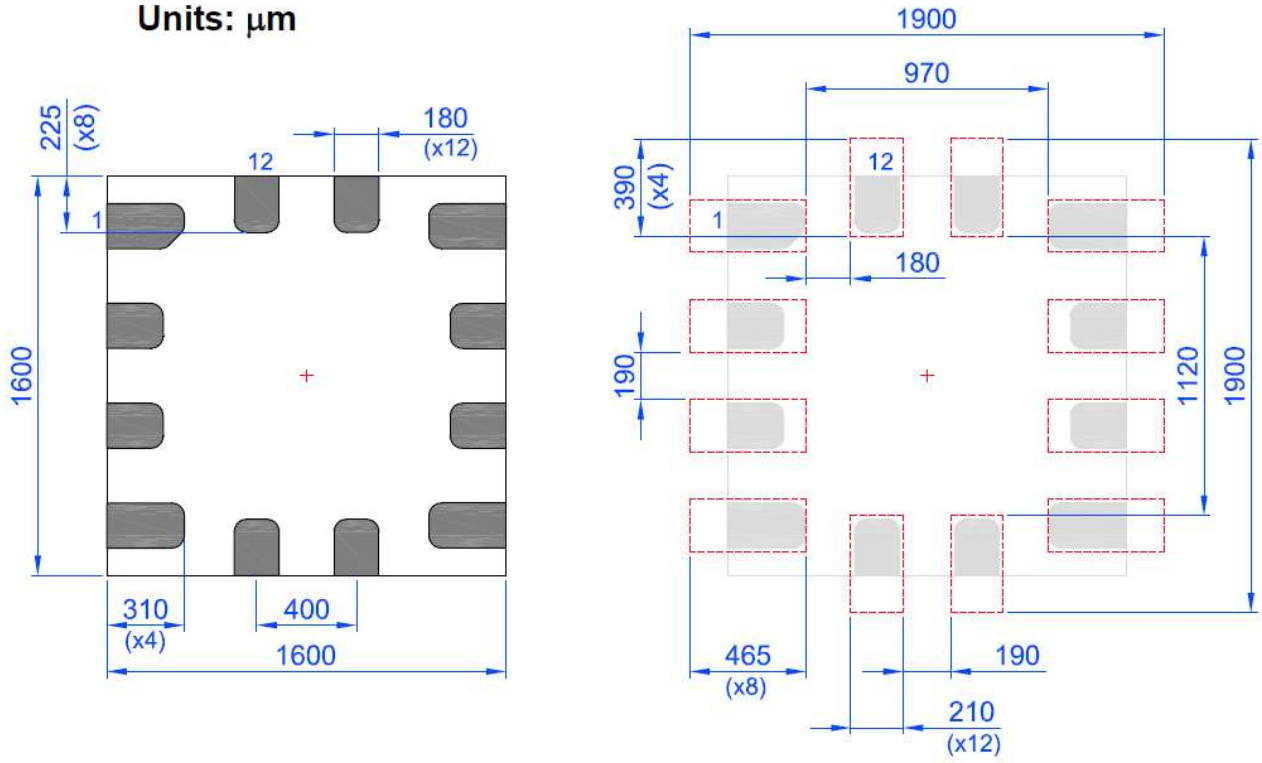
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)

Units: µm



Datasheet Revision History

Date	Version	Change
10/22/2021	0.10	New design for SLG46110 chip
07/11/2023	0.11	Moved to Renesas template

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