PDP_MB_R1.0_U5_PWRMNG_0x78_R1.0

General Description

Renesas SLG7RN46432 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

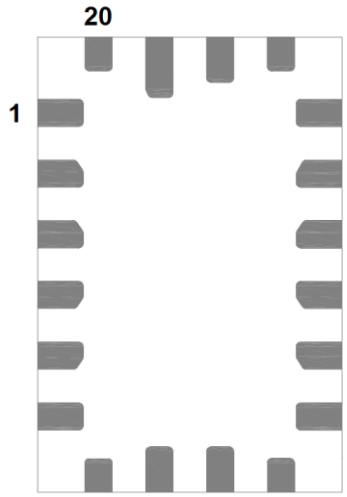
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

15 Outputs - Push Pull 2X

Pin Configuration

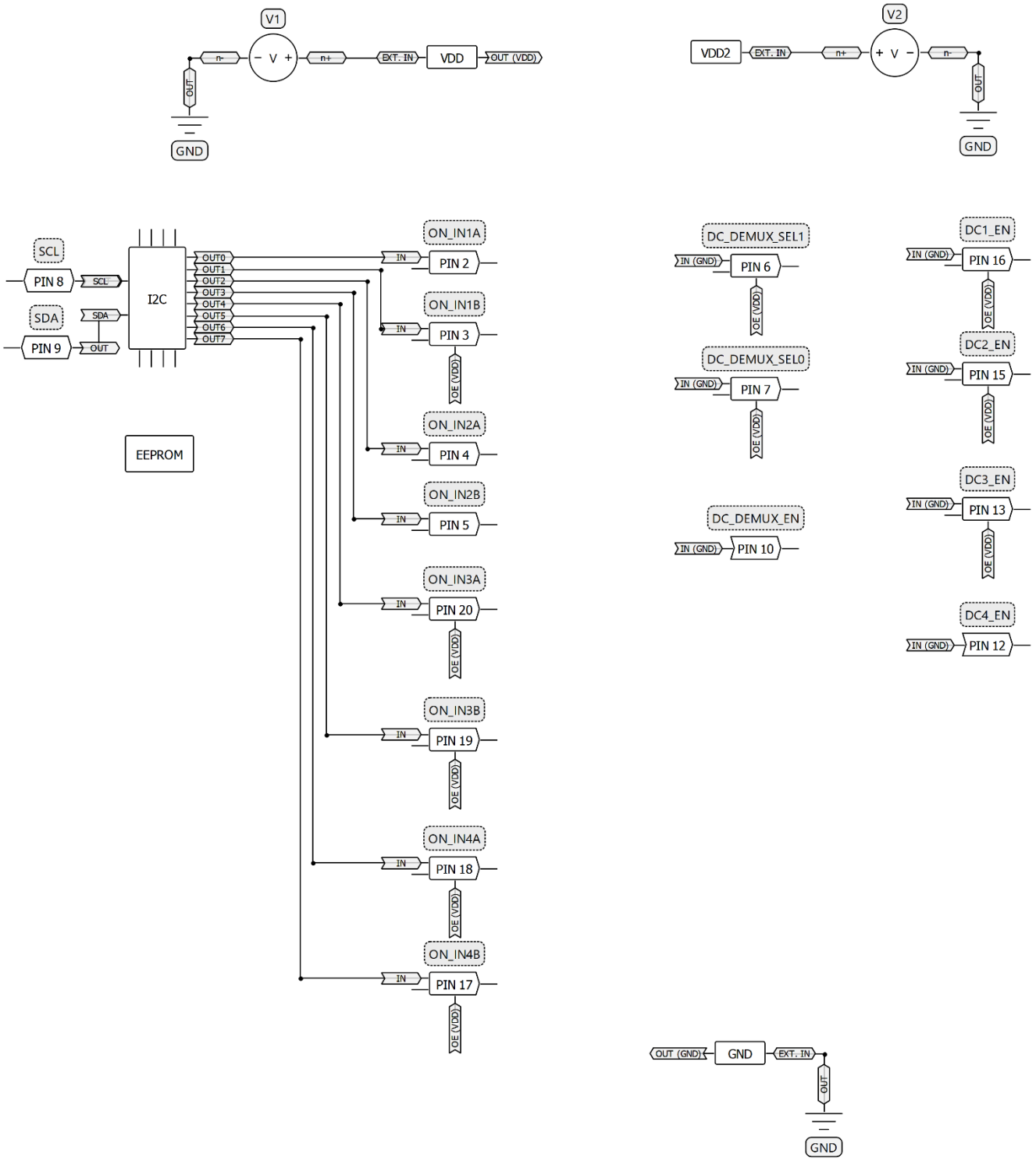


20-pin STQFN
(Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	ON_IN1A	12	DC4_EN
3	ON_IN1B	13	DC3_EN
4	ON_IN2A	14	VDD2
5	ON_IN2B	15	DC2_EN
6	DC_DEMUX_SEL1	16	DC1_EN
7	DC_DEMUX_SEL0	17	ON_IN4B
8	SCL	18	ON_IN4A
9	SDA	19	ON_IN3B
10	DC_DEMUX_EN	20	ON_IN3A

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	ON_IN1A	Digital Output	Push Pull 2X	floating
3	ON_IN1B	Digital Output	Push Pull 2X	floating
4	ON_IN2A	Digital Output	Push Pull 2X	floating
5	ON_IN2B	Digital Output	Push Pull 2X	floating
6	DC_DEMUX_SEL1	Digital Output	Push Pull 2X	floating
7	DC_DEMUX_SEL0	Digital Output	Push Pull 2X	floating
8	SCL	Digital Input	Low Voltage Digital Input	floating
9	SDA	Digital Input	Low Voltage Digital Input	floating
10	DC_DEMUX_EN	Digital Output	Push Pull 2X	floating
11	GND	GND	Ground	--
12	DC4_EN	Digital Output	Push Pull 2X	floating
13	DC3_EN	Digital Output	Push Pull 2X	floating
14	VDD2	PWR	Supply Voltage	--
15	DC2_EN	Digital Output	Push Pull 2X	floating
16	DC1_EN	Digital Output	Push Pull 2X	floating
17	ON_IN4B	Digital Output	Push Pull 2X	floating
18	ON_IN4A	Digital Output	Push Pull 2X	floating
19	ON_IN3B	Digital Output	Push Pull 2X	floating
20	ON_IN3A	Digital Output	Push Pull 2X	floating

Ordering Information

Part Number	Package Type
SLG7RN46432V	20-pin STQFN
SLG7RN46432V	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current Through V_{DD} Pin		--	90	mA
Maximum Average or DC Current Through V_{DD2} Pin		--	90	mA
Maximum Average or DC Current Through GND Pin (Per chip side, (Note 1))		--	100	mA
Maximum Average or DC Current (Through pin)	Push-Pull 2x	--	22.1	mA
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		
Note 1 The GreenPAK's GND rail is divided in two sides. IOs 0 to 6, SCL, SDA are connected to one side and IOs 7 to 14 are connected to another side.				

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.4	3.3	5	V
V_{DD2}	Supply Voltage		1.71	3.3	5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	VDD=5V; SCL and SDA HIGH; Floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Low-Level Logic Input	1.25	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Low-Level Logic Input	GND-0.3	--	0.5	V
V_{OH}	HIGH-Level Output Voltage (Note 1)	Push-Pull 2X, I_{OH}=100µA at VDD=2.5V	2.443	--	--	V
		Push-Pull 2X, I_{OH}=3mA at VDD=3.3V	3.165	--	--	V
		Push-Pull 2X, I_{OH}=5mA at VDD=5.0V	4.821	--	--	V
V_{OL}	LOW-Level Output Voltage (Note 1)	Push-Pull 2X, I_{OL}=100µA, at VDD=2.5V	--	--	0.043	V
		Push-Pull 2X, I_{OL}=3mA, at VDD=3.3V	--	--	0.107	V
		Push-Pull 2X, I_{OL}=5mA, at VDD=5.0V	--	--	0.145	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 2X, VOH=VDD-0.2V at VDD=2.5V	3.40	--	--	mA
		Push-Pull 2X, VOH=2.4V at VDD=3.3V	16.54	--	--	mA

		Push-Pull 2X, VOH=2.4V at VDD=5.0V	48.49	--	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 2X, V_{OL}=0.15V, at VDD=2.5V	3.44	--	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=3.3V	10.73	--	--	mA
		Push-Pull 2X, V_{OL}=0.4V, at VDD=5.0V	13.52	--	--	mA
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.66	2.59	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.60	1.85	2.07	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.97	1.23	1.46	V

Note:
1. PINs 1 to 10 are powered from VDD and PINs 12 to 20 are powered from VDD2.
2. Guaranteed by Design.

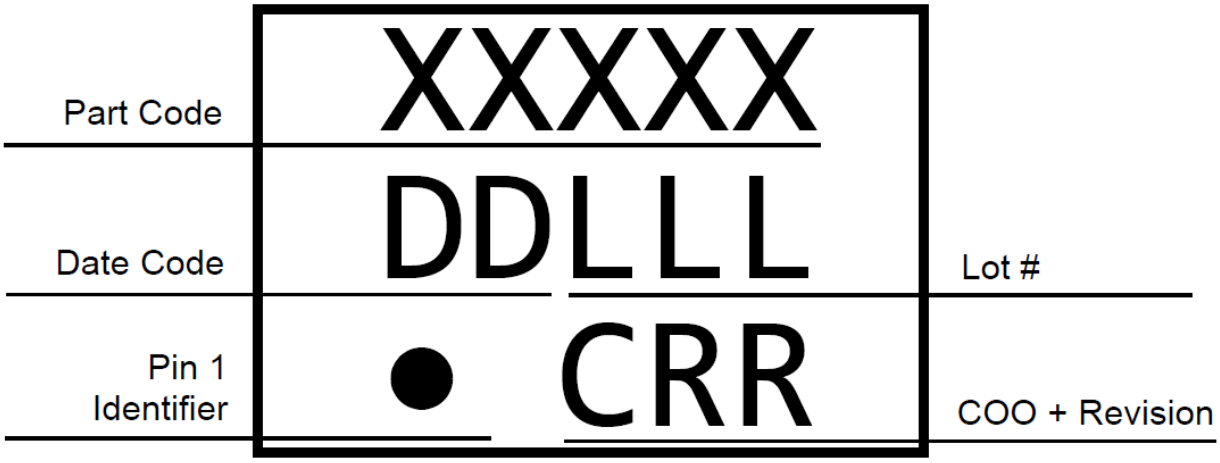
I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (2.3...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = (2.3...5.5) V	--	--	95	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (2.3...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (2.3...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (2.3...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (2.3...5.5) V	50	--	--	ns

Chip address

HEX	BIN	DEC
0x78	1111000	120

Package Top Marking



XXXXX - Part ID FieldL identifies the specific device configuration
DD - Date Code Field: Coded date of manufacture
LLL - Lot Code: Designates Lot #
C - Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR - Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0xD4DC1347	46432	AA	04/06/2023

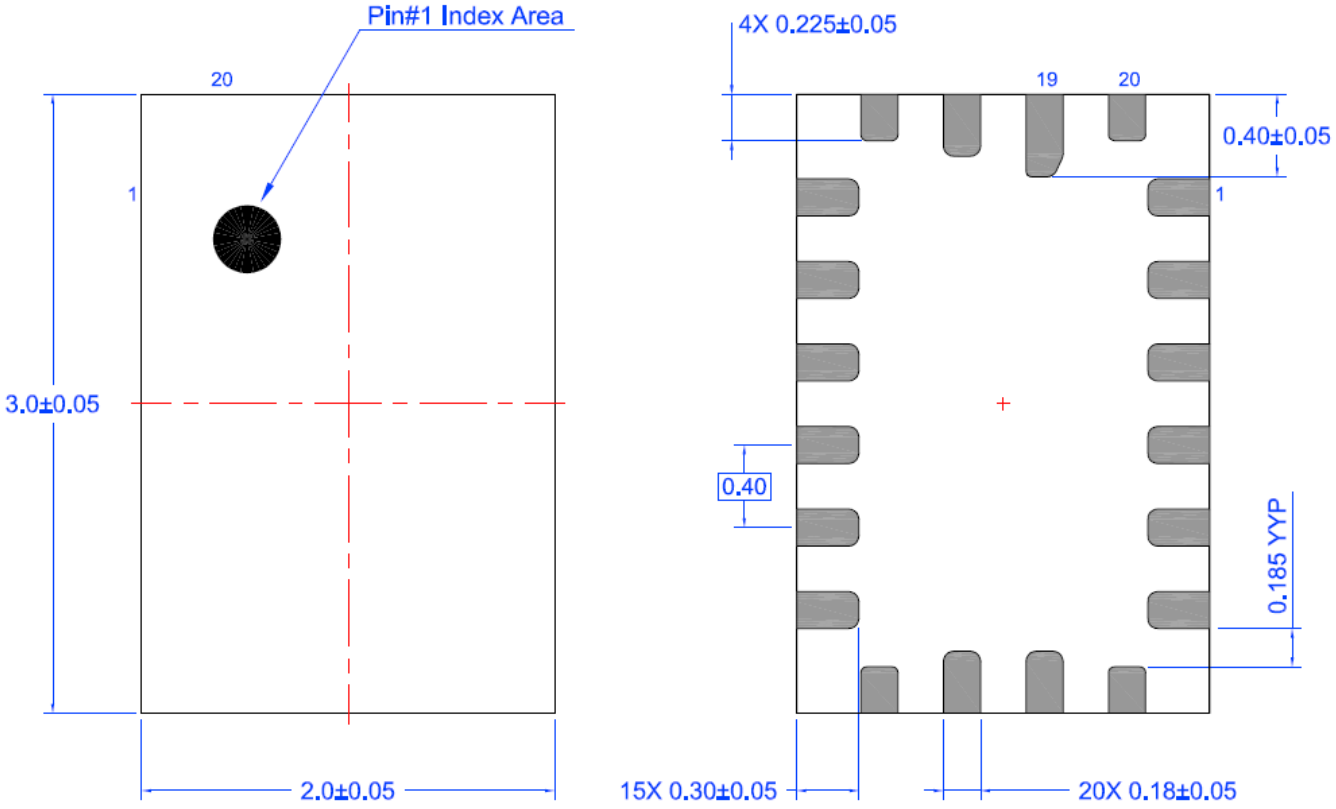
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read
	Partly lock write
	Partly lock read and write
	Partly lock read and lock write
	Lock read and partly lock write
	Read lock
	Write lock
	Lock read and write

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

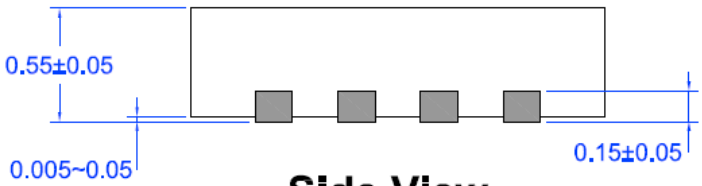
Package Outlines

STQFN 20L 2x3mm 0.4P FCD Package
IC Net Weight: 0.008 g



Marking View

BTM View



Side View

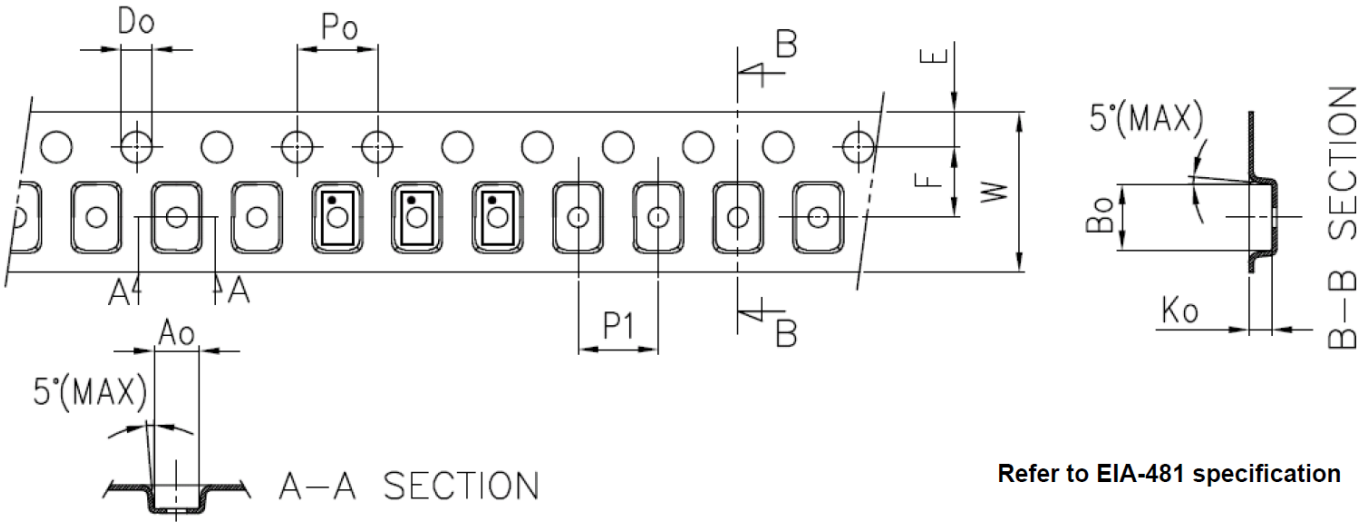
Unit: mm

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P FCD	20	2 x 3 x 0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

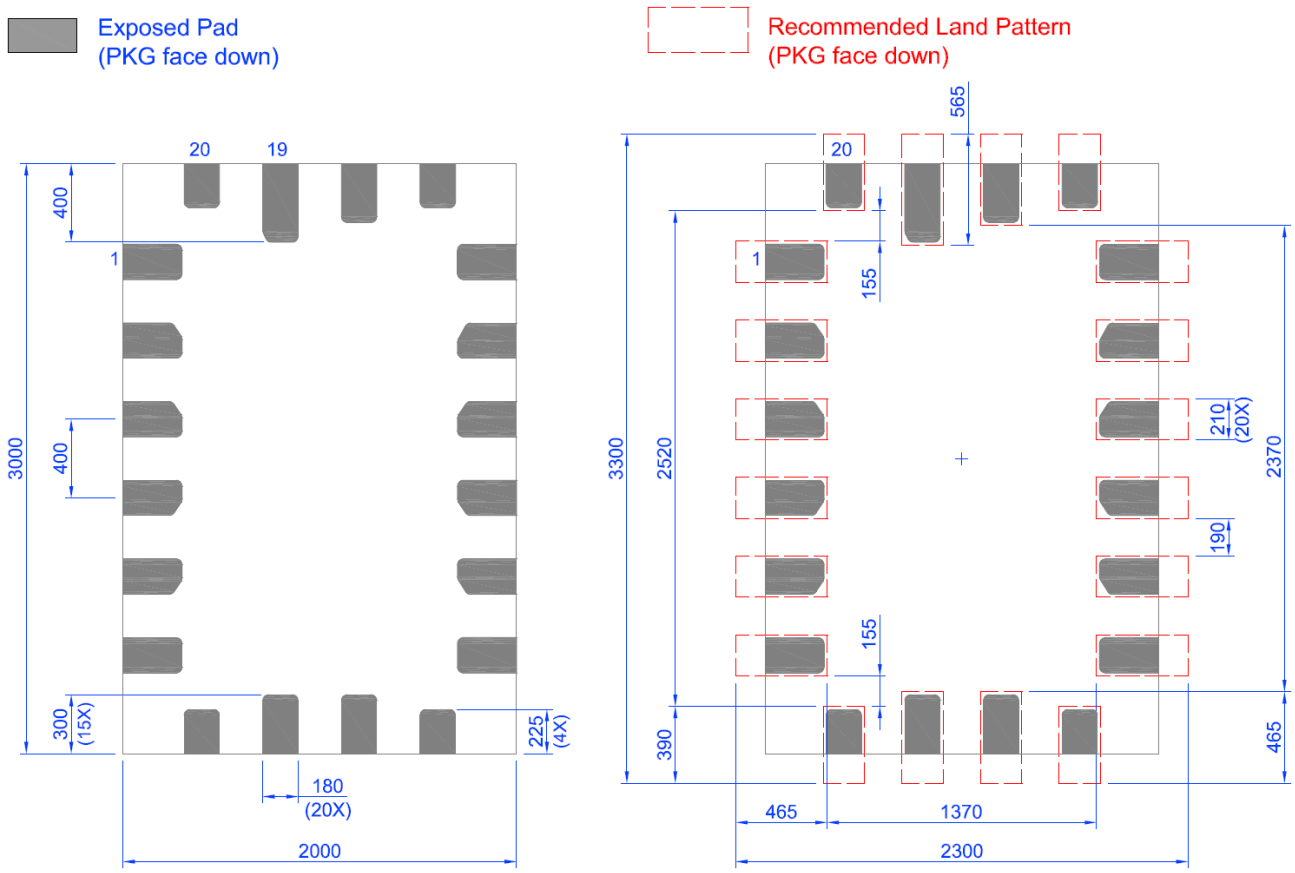


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines



Unit: µm

Datasheet Revision History

Date	Version	Change
03/27/2023	0.10	New design for SLG46826 chip
04/06/2023	0.11	Updated Device Revision Table

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