SLG7RN46454

GreenPAK ™

6GPIO I2C IO expender

General Description

Renesas SLG7RN46454 is a low power and small form device. The SoC is housed in a 1.6mm x 2.0mm STQFN package which is optimal for using with small devices.

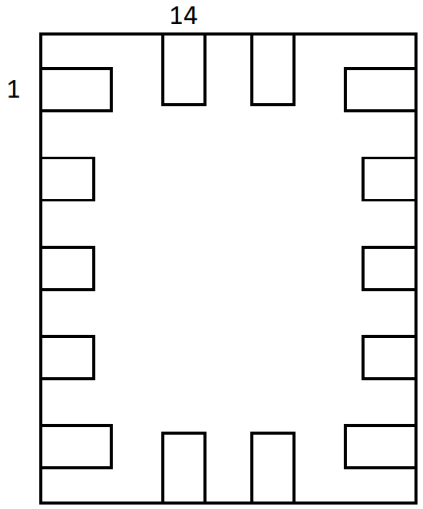
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Output Summary

1 Output - Open Drain NMOS 1X
6 Outputs - Push Pull 1X

Pin Configuration

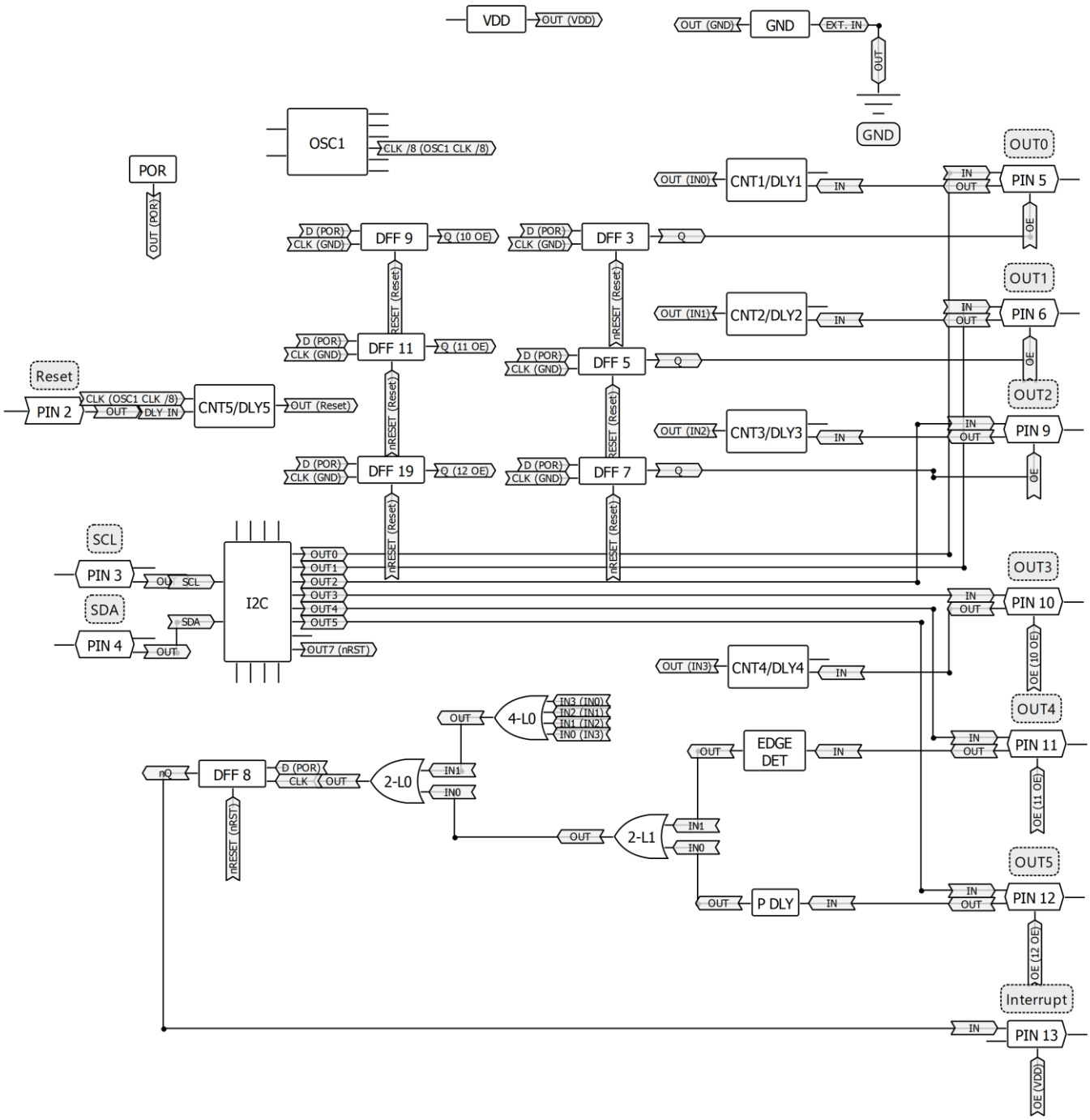


14-pin STQFN (Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	Reset	9	OUT2
3	SCL	10	OUT3
4	SDA	11	OUT4
5	OUT0	12	OUT5
6	OUT1	13	Interrupt
7	NC	14	NC

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	Reset	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	SCL	Digital Input	Digital Input without Schmitt trigger	floating
4	SDA	Digital Input	Digital Input without Schmitt trigger	floating
5	OUT0	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
6	OUT1	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
7	NC	--	Keep Floating or Connect to GND	--
8	GND	GND	Ground	--
9	OUT2	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
10	OUT3	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
11	OUT4	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
12	OUT5	Bi-directional	Digital Input without Schmitt trigger / Push Pull 1X	floating
13	Interrupt	Digital Output	Open Drain NMOS 1X	floating
14	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG7RN46454V	14-pin STQFN
SLG7RN46454V	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	V_{DD}+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	OD 1x	--	11	
Current at Input Pin		-1.0	1.0	mA
Input leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=1mA at VDD=2.5V	2.15	--	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD=3.3V	2.7	--	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD=5.0V	4.16	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=1mA, at VDD=2.5V	--	--	0.103	V
		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.218	V
		Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	--	0.270	V
		Open Drain NMOS 1X, I_{OL}=1mA, at VDD=2.5V	--	--	0.043	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	--	0.087	V
		Open Drain NMOS 1X, I_{OL}=5mA, at VDD=5.0V	--	--	0.107	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, V_{OH}=VDD-0.2V at VDD=2.5V	1.37	--	--	mA

		Push-Pull 1X, V_{OH}=2.4V at VDD=3.3V	5.61	--	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD=5.0V	20.42	--	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=2.5V	1.52	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	5.42	--	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	7.36	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.15V, at VDD=2.5V	4.11	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	13.35	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=5.0V	17.90	--	--	mA
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	--	1	--	MΩ
T_{DLY5}	Delay5 Time	At temperature 25°C	0.98	1	1.02	ms
		At temperature -40 +85°C (Note 3)	0.98	1	1.04	ms
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.

I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (2.3...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5V ± 8%	--	--	95	ns
		V_{DD} = 3.3V ± 10%	--	--	95	ns
		V_{DD} = 5.0V ± 10%	--	--	111	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (2.3...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (2.3...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (2.3...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (2.3...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (2.3...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (2.3...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (2.3...5.5) V	50	--	--	ns

Chip address

HEX	BIN	DEC
0x08	0001000	8

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<2027:2024>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

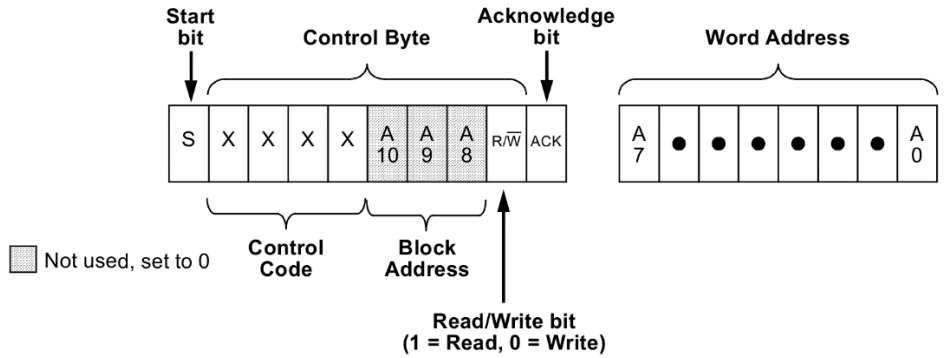


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

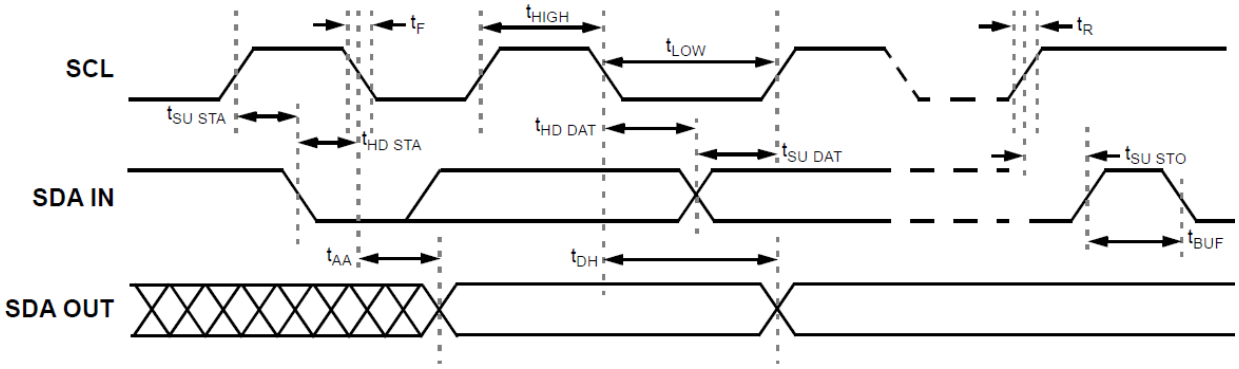


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46454 to the correct data byte to be written. After the SLG7RN46454 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46454 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46454 generates the Acknowledge bit.

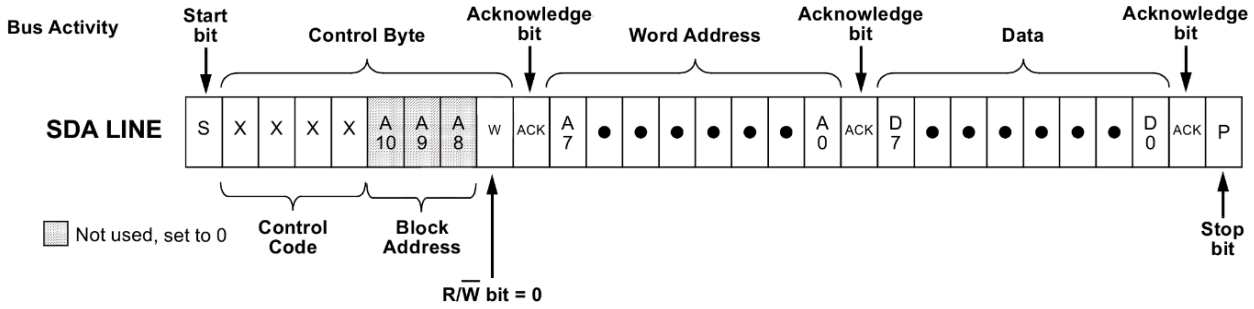


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7RN46454 issues an Acknowledge bit, followed by the requested eight data bits.

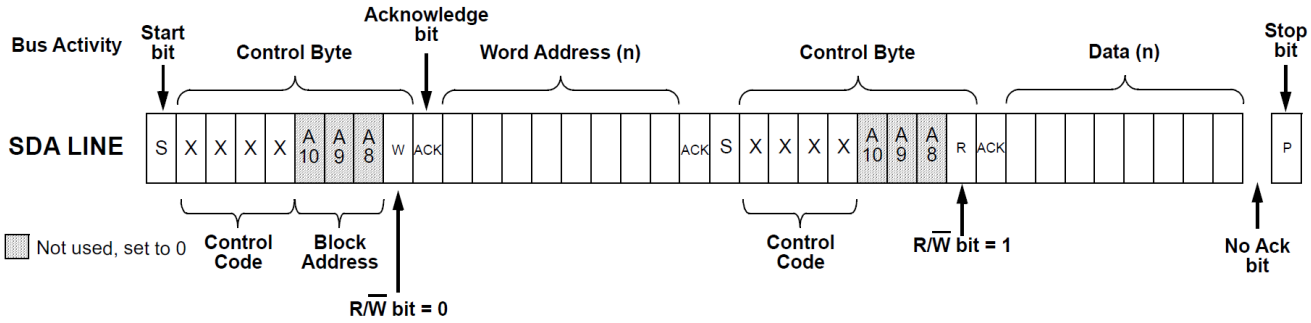


Figure4. I2C Random Read Command

4. I2C register control data

Address Byte	Register Bit	Block	Function
0x4C	reg<608>	Virtual Input <0>	Enable (0) and disable (1) VOUT0 Default is 0.
	reg<609>	Virtual Input <1>	Enable (0) and disable (1) VOUT1 Default is 0.
	reg<610>	Virtual Input <2>	Enable (0) and disable (1) VOUT2 Default is 0.
	reg<611>	Virtual Input <3>	Enable (0) and disable (1) VOUT3 Default is 0.
	reg<612>	Virtual Input <4>	Enable (0) and disable (1) VOUT4 Default is 0.
	reg<613>	Virtual Input <5>	Enable (0) and disable (1) VOUT5 Default is 0.
	reg<615>	Virtual Input <7>	nRST signal for DFF8 Interrupt, default is 1
0x4D	reg<621>	GPIO2 Digital Input	Read GPIO2 Digital Input status
	reg<622>	GPIO3 Digital Input	Read GPIO3 Digital Input status
	reg<623>	GPIO4 Digital Input	Read GPIO4 Digital Input status
0x4E	reg<624>	GPIO5 Digital Input	Read GPIO5 Digital Input status
	reg<625>	GPIO6 Digital Input	Read GPIO6 Digital Input status
	reg<626>	GPIO7 Digital Input	Read GPIO7 Digital Input status
0x06	reg<48:53>	CLK Input of DFF3	Set Pin5 as Output
0x07	reg<60:63>	nRST of DFF3	Reset Pin5 to Input
0x08	reg<64:65>		
0x0A	reg<84:87>	CLK Input of DFF5	Set Pin6 as Output
0x0B	reg<88:89>		
0x0C	reg<96:101>	nRST of DFF5	Reset Pin6 to Input
0x0F	reg<120:125>	CLK Input of DFF7	Set Pin9 as Output
0x10	reg<132:135>	nRST of DFF7	Reset Pin9 to Input
0x11	reg<136:137>		
0x13	reg<156:159>	CLK Input of DFF9	Set Pin10 as Output
0x14	reg<160:161>		
0x15	reg<168:173>	nRST of DFF9	Reset Pin10 to Input
0x18	reg<192:197>	CLK Input of DFF11	Set Pin11 as Output
0x19	reg<204:207>	nRST of DFF11	Reset Pin11 to Input
0x1A	reg<208:209>		
0x21	reg<264:269>	CLK Input of DFF19	Set Pin12 as Output
0x22	reg<276:279>	nRST of DFF19	Reset Pin12 to Input
0x23	reg<280:281>		

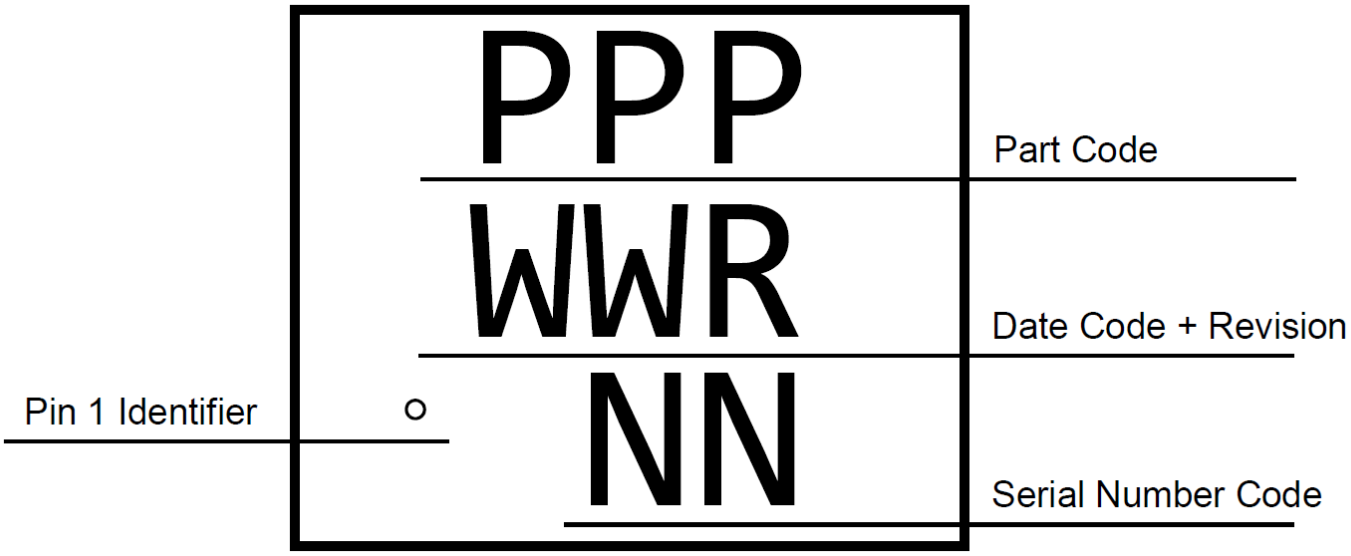
5. I2C Commands:

1. [start] [0x08] [w] [0x4C] [xxxxxxx(OUT0)] [stop] // enable (OUT0 = 0) or disable (OUT0 = 1)
2. [start] [0x08] [w] [0x4C] [xxxxxx(OUT1)x] [stop] // enable (OUT1 = 0) or disable (OUT1 = 1)
3. [start] [0x08] [w] [0x4C] [xxxxx(OUT2)xx] [stop] // enable (OUT2 = 0) or disable (OUT2 = 1)
4. [start] [0x08] [w] [0x4C] [xxxx(OUT3)xxx] [stop] // enable (OUT3 = 0) or disable (OUT3 = 1)
5. [start] [0x08] [w] [0x4C] [xxx(OUT4)xxxx] [stop] // enable (OUT4 = 0) or disable (OUT4 = 1)
6. [start] [0x08] [w] [0x4C] [xx(OUT5)xxxxx] [stop] // enable (OUT5 = 0) or disable (OUT5 = 1)
7. [start] [0x08] [w] [0x4C] [(OUT7)xxxxxxx] [stop] // write 0 to reg<615> then write 1 to reg <615> to reset DFF8
8. [start] [0x08] [w] [0x4D] [stop] [start] [0x08] [R] [(GPIO4) (GPIO3) (GPIO2)xxxxx] [stop] // read GPIO4, GPIO3, GPIO2 input status
9. [start] [0x08] [w] [0x4E] [stop] [start] [0x08] [R] [xxxxx(GPIO7) (GPIO6) (GPIO5)] [stop] // read GPIO5, GPIO6, GPIO7 input status
10. [start] [0x08] [w] [0x06] [0xBE] [stop] // write 0xBE to reg[0x06]
11. [start] [0x08] [w] [0x06] [0x80] [stop] // write 0x80 to reg[0x06]
    Command 10 and 11 together change PIN5 to Output mode, can use command 1 to write PIN5 status
12. [start] [0x08] [w] [0x07] [0x08][0x0F][0x00] [stop] // write 0x0F and 0x00 to reg] [0x07] [0x08]

13. [start] [0x08] [w] [0x07] [0x08][0x8F][0x01] [stop] // write 0x8F and 0x01 to reg] [0x07] [0x08]
    Command 12 and 13 together reset PIN5 to Input mode
14. [start] [0x08] [w] [0x0A] [0x0B][0xE0][0xFB] [stop] // write 0xE0 and 0xFB to reg] [0x0A] [0x0B]
15. [start] [0x08] [w] [0x0A] [0x0B][0x00][0xF8] [stop] // write 0x00 and 0xF8 to reg] [0x0A] [0x0B]
    Command 14 and 15 together change PIN6 to Output mode, can use command 2 to write PIN6 status
16. [start] [0x08] [w] [0x0C] [0x00] [stop] // write 0x00 to reg[0x0C]
17. [start] [0x08] [w] [0x0C] [0x18] [stop] // write 0x18 to reg[0x0C]
    Command 16 and 17 together reset PIN6 to Input mode
18. [start] [0x08] [w] [0x0F] [0xBE] [stop] // write 0xBE to reg[0x0F]
19. [start] [0x08] [w] [0x0F] [0x80] [stop] // write 0x80 to reg[0x0F]
    Command 18 and 19 together change PIN9 to Output mode, can use command 3 to write PIN9 status
20. [start] [0x08] [w] [0x10] [0x11][0x0F][0x04] [stop] // write 0xE0 and 0xFB to reg [0x10] [0x11]
21. [start] [0x08] [w] [0x10] [0x11][0x8F][0x05] [stop] // write 0x8F and 0x05 to reg [0x10] [0x11]
    Command 20 and 21 together reset PIN9 to Input mode
22. [start] [0x08] [w] [0x13] [0x14][0xE9][0xFB] [stop] // write 0xE9 and 0xFB to reg] [0x13] [0x14]
23. [start] [0x08] [w] [0x13] [0x14][0x09][0xF8] [stop] // write 0x09 and 0xF8 to reg] [0x13] [0x14]
    Command 22 and 23 together change PIN10 to Output mode, can use command 4 to write PIN10 status
24. [start] [0x08] [w] [0x15] [0x00] [stop] // write 0x00 to reg[0x15]
25. [start] [0x08] [w] [0x15] [0x18] [stop] // write 0x18 to reg[0x15]
    Command 24 and 25 together reset PIN10 to Input mode
26. [start] [0x08] [w] [0x18] [0xBE] [stop] // write 0xBE to reg[0x18]
27. [start] [0x08] [w] [0x18] [0x80] [stop] // write 0x80 to reg[0x080]
    Command 26 and 27 together change PIN11 to Output mode, can use command 5 to write PIN11 status
28. [start] [0x08] [w] [0x19] [0x1A][0x0F][0x00] [stop] // write 0x0F and 0x00 to reg [0x19] [0x1A]
29. [start] [0x08] [w] [0x19] [0x1A][0x8F][0x01] [stop] // write 0x8F and 0x01 to reg [0x19] [0x1A]
    Command 28 and 29 together reset PIN11 to Input mode
30. [start] [0x08] [w] [0x21] [0x3E] [stop] // write 0xBE to reg[0x21]
31. [start] [0x08] [w] [0x21] [0x00] [stop] // write 0x80 to reg[0x021]
    Command 30 and 31 together change PIN12 to Output mode, can use command 6 to write PIN12 status
32. [start] [0x08] [w] [0x22] [0xE0] [stop] // write 0xE0 to reg [0x22]
33. [start] [0x08] [w] [0x22] [0xE6] [stop] // write 0xE6 to reg [0x22]
    Command 32 and 33 together reset PIN12 to Input mode

Note: PIN2 Reset is active L signal, when PIN2 is pull Low for more than 1ms, all OUT0 to OUT5 will reset back to Input mode. When PIN2 assert back to High, can use I2C write command to change the OUT0 and OUT5 to output mode.
Note: Read GPIO status need change the GPIO to Input first

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	002	U	0x201A2406			05/02/2023

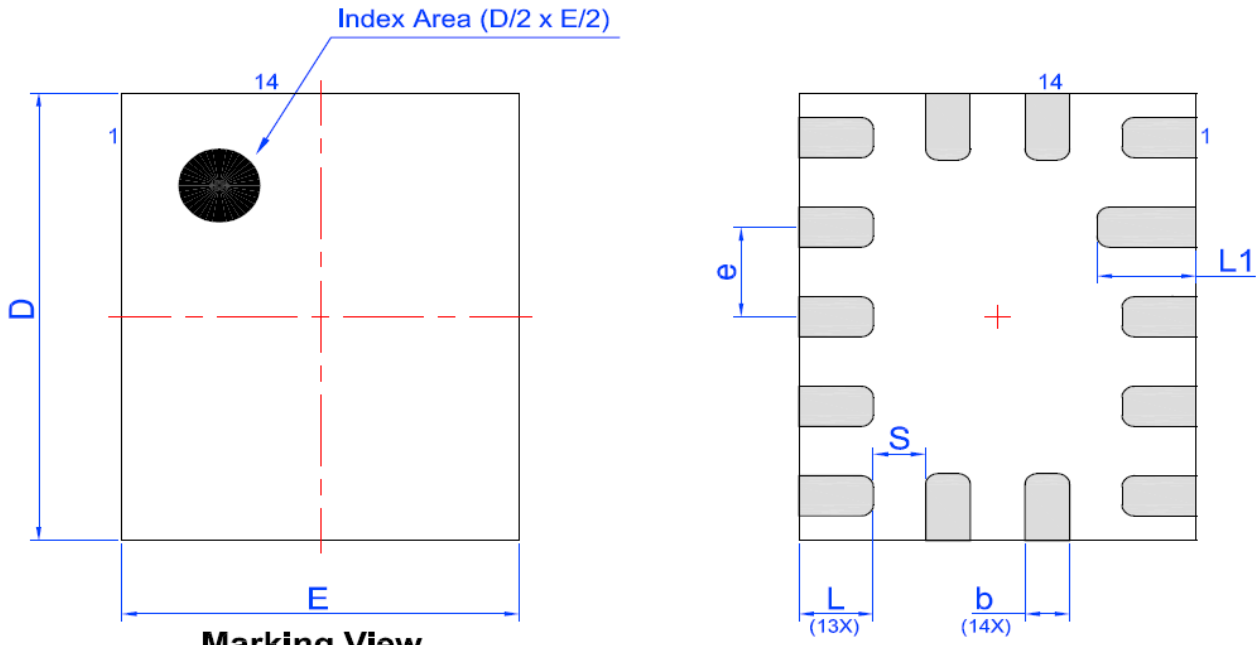
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

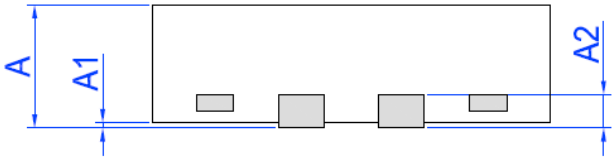
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Marking View



Marking View

Unit: mm

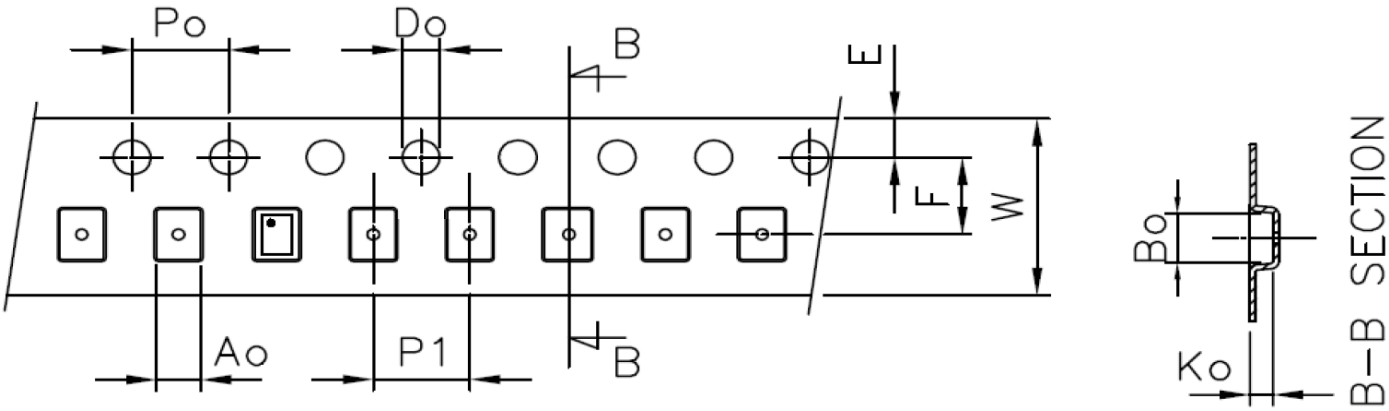
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

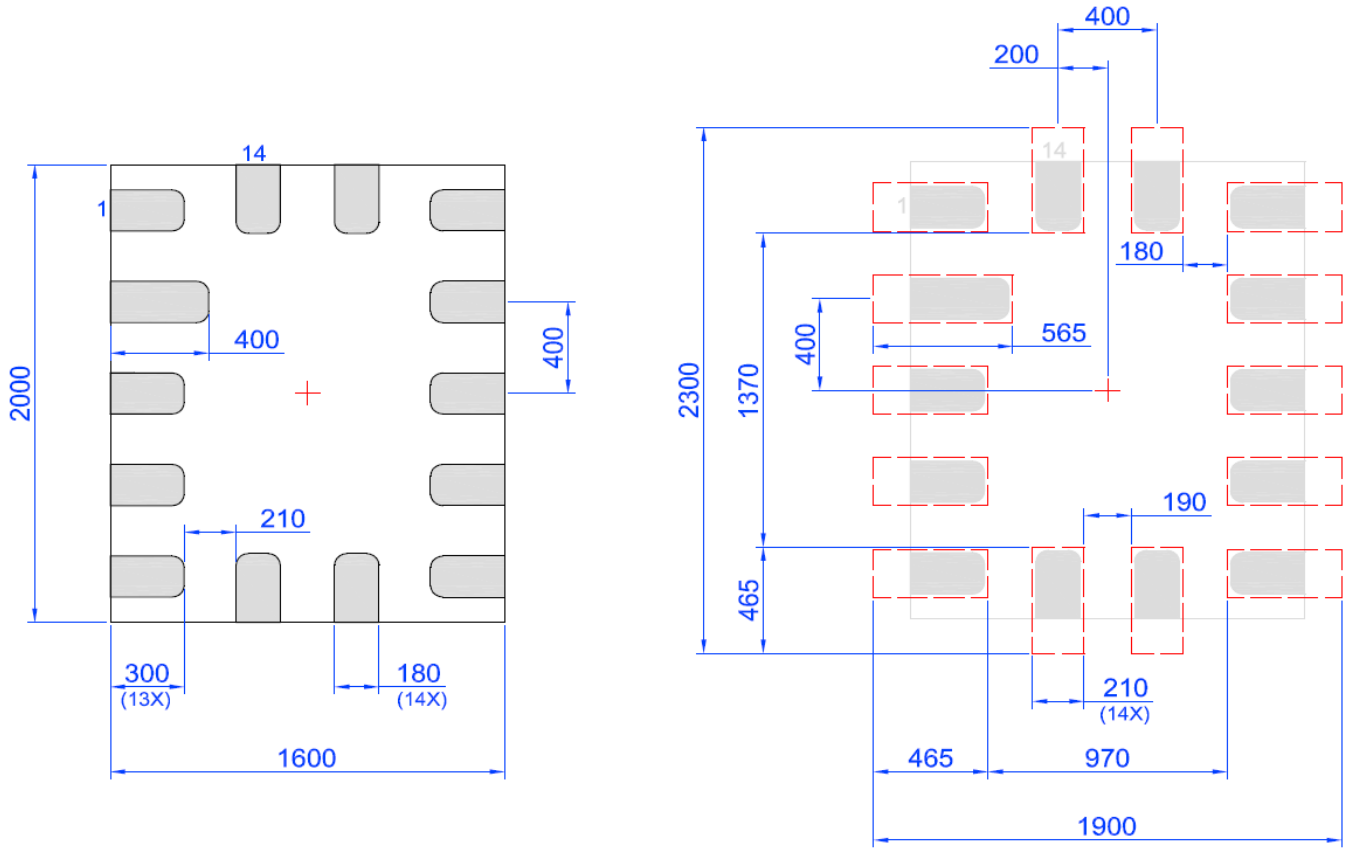
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Layout Guidelines



Unit: um

Datasheet Revision History

Date	Version	Change
04/04/2023	0.10	New design for SLG46855 chip
05/02/2023	0.11	Add Interrupt and reset function

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