8V19N882

Evaluation Board Manual

Description

This document describes following about the 8V19N882 Evaluation Board:

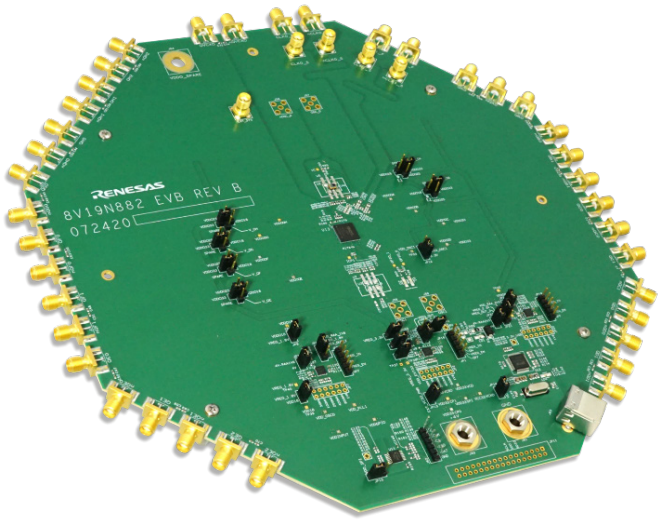
- Basic hardware and GUI setup
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file
- Hardware modifications required for different conditions

Features

The board has SMA connectors to relevant I/O of the device.

- Two differential clock inputs
- 16 differential outputs – Most outputs can be configured to clock outputs or Sysref outputs
- One different output for direct VCXO buffer
- External VCXO
- External footprint for VCO up to 6GHz
- Selectable output buffer voltage
- Laboratory power supply connectors
- Serial port for configuration and register read out

Board Diagram



PC Requirements

- Renesas Timing Commander Software installed
- 8V19N882 GUI
- USB 2.0 or USB 3.0 Interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space:
  - Minimum 600MB (1.5GB 64-bit)
  - Recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system

Kit Contents

- 8V19N882 Evaluation Board
- USB Type B Cable
- Quick Start Guide

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1. Functional Description

The evaluation kit supports evaluation process of the 8V19N882NVGI, a fully integrate FemtoClock RF Sampling Clock Generator and Jitter Attenuator. The device also supports JESD204B/C. The 8V19N882 is two stage PLL architecture. The first stage PLL use external VCXO and the second stage has option to use either internal VCO or external VCO. The internal VCO is built-in 3.93216GHz. The external VCO frequency can be selected up to 6GHz. This evaluation kit provide layout footprints for the 1st stage external VCXO and the 2nd stage external VCO.

1.1 Operational Characteristics

When powering the board with a direct 4V supply, allow for excess current by setting the current limit to 2A. Before writing any registers to the device roughly 1A should be seen pulled from the direct supply. The input voltage should not exceed 5V.

The board has been designed to operate over the industrial temperature range from -40C to 85C, ambient temperature.

It is recommended that the person operating the board use proper grounding to avoid ESD damage to the EVB.

1.2 Setup and Configuration

The setup and configuration is split into two separate areas being the hardware, GUI setup, and example Sysref output setup. The hardware setup consists of jumper orientations and a general overview of test instrument connection. The GUI setup shows how to establish a connection with the device through the Timing Commander software. Sysref output setup will show how to establish Sysref outputs for JESD204B compliance.

1.2.1. Hardware Setup

A direct 4V power supply should be attached to the evaluation board with the positive terminal at J60 and the ground source at J61. The USB type B cable should be connected at J63 and the computer that will be loading the Timing Commander software. For the initial setup, a differential clock source can be connected to CLK/nCLK and configured to 122.88 MHz with 400 mV to 800mV amplitude (there is on board AC coupling and self bias).

For proper functionality out of the box, the jumpers on board should be placed to allow the correct voltages at each LDO and domain. The jumpers should be arranged as seen in Table 1.

Table 1. Default Jumper Configurations

Jumper	Label	Default Orientation
E1	V_QA	Between VDDO33 and center
E2	V_QB	Between VDDO33 and center
E3	V_QE	Between VDDO33 and center
E4	V_QF	Between VDDO33 and center
E5	V_QG	Between VDDO33 and center
E6	V_QH	Between VDDO33 and center
JP1	VREG_IN, VREG_EN	OFF
JP3	VREG_3.3V, VDD33	ON
JP4	VREG_3.3V, VDDO33	ON

Jumper	Label	Default Orientation
JP5	VREG_3.3V,	ON
JP6	VREG_IN, VREG_EN	OFF
JP8	VREG_1.8V	ON
JP9	VDDO18	ON
JP10	VDD_SPI	Between the left most pin and the center.
JP12	VDD_OSCI	Between VDD33_OSCI and 3.3V
JP13	EXT_VCSO_PWR	ON
JP14	VCXO_PWR	ON
JP15	VREG_OUT, VREG_3.3V, VDD_RAA_3V3	Between VDD_RAA_3V3 and VREG_3.3V
JP16	4V-RAA3V3	ON
JP17	VDD_RAA_1V8, VREG_1.8V, VREG_OUT_2	Between VDD_RAA_1V8 and VREG_1.8V
JP18	4V-RAA1V8	ON
JP19	VREG_IN, VREG_EN	OFF
JP21	VDD_RAA_2V5, VREG_2.5V, VREG_OUT_3	Between VDD_RAA_2V5 and VREG_2.5V
JP22	VDDO25	ON
JP23	4V-RAA2V5	ON

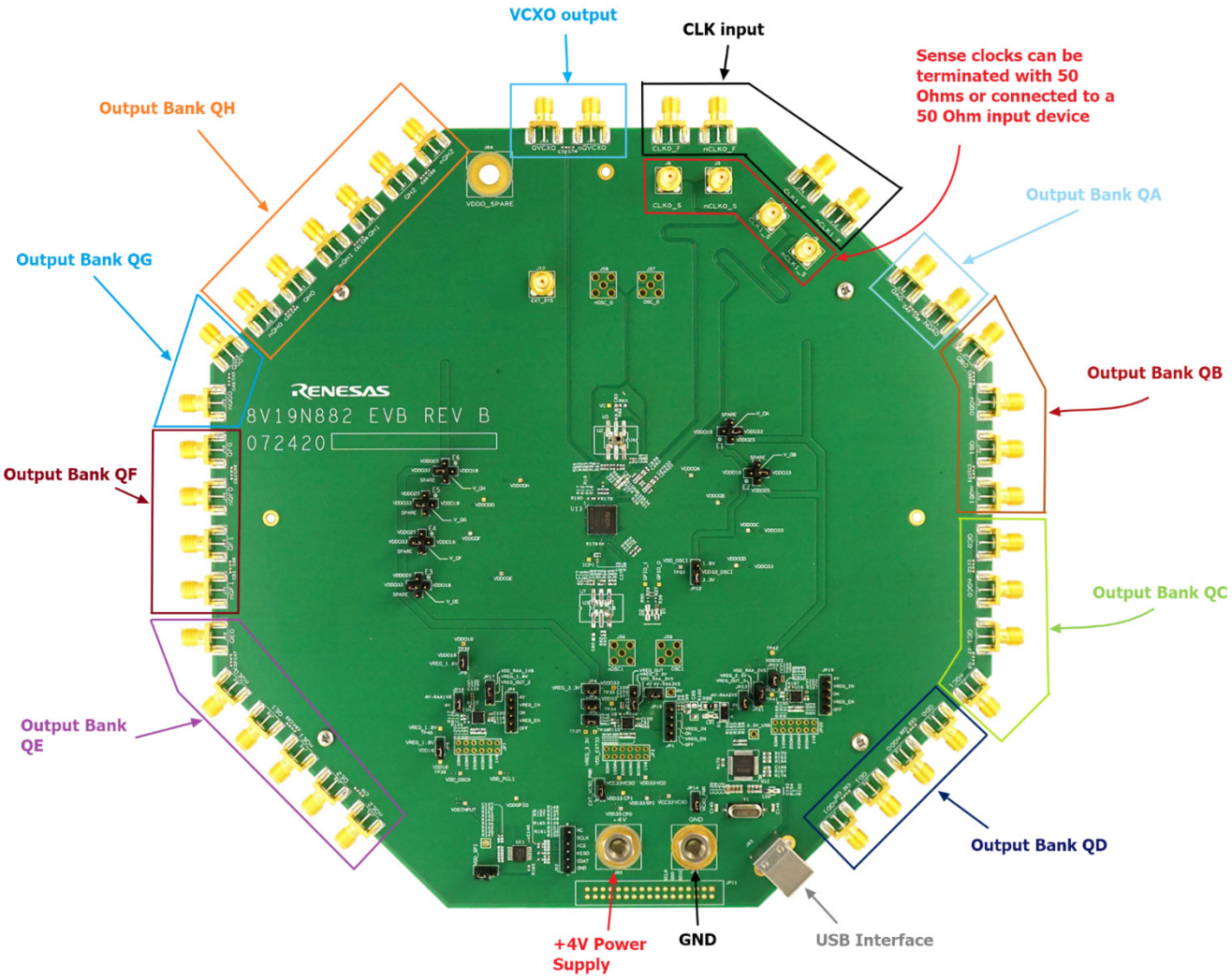


Figure 1. Labeled Board Image

1.2.2. Prepare the Software

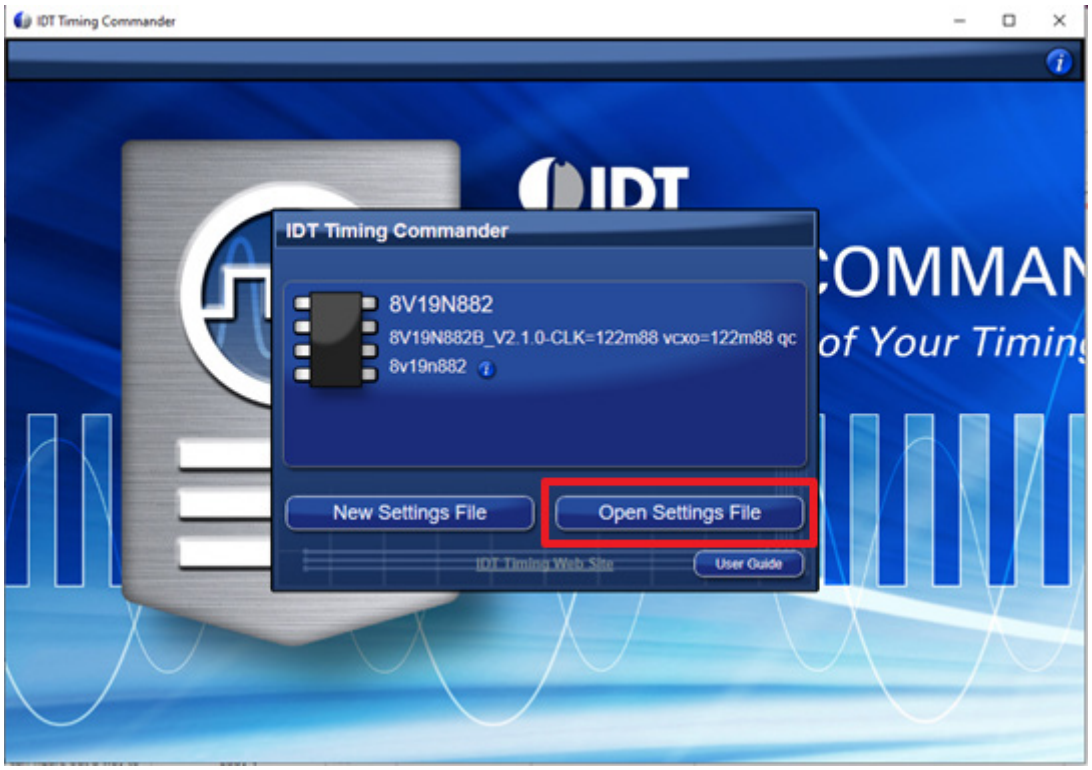
1. Prior to execution of the GUI, the Timing Commander software must be downloaded and installed.

   If Timing Commander is already installed on the computer, skip this step.

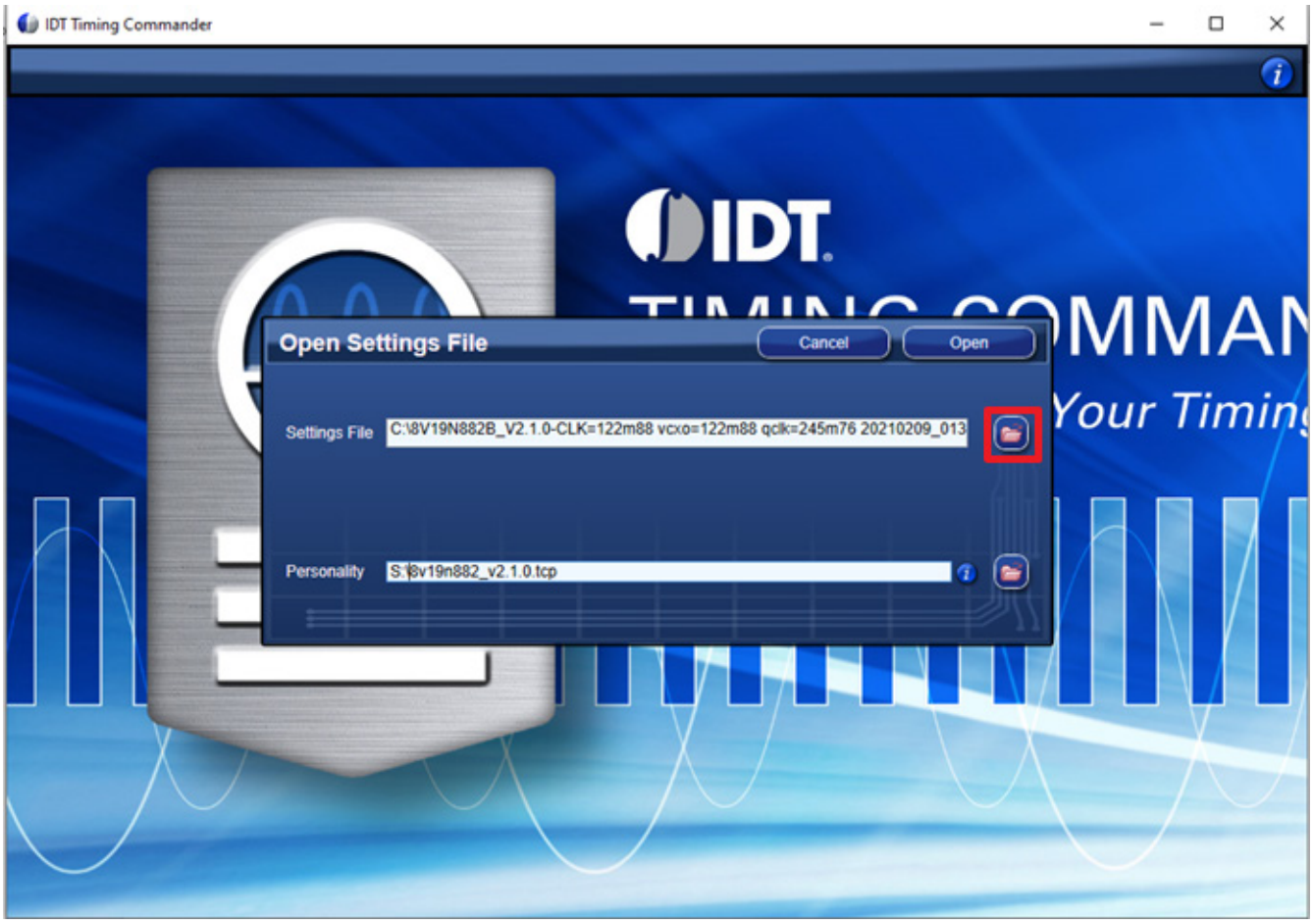
2. If the Timing Commander is not yet installed, please download and install the software from the Timing Commander webpage.
3. After the software file is downloaded, double-click on the TimingCommanderSetup.exe and follow the on-screen instructions to complete the setup.

1.2.3. Bring Up the GUI

1. After successfully installing the Timing Commander software, activate the software from the Window <start> at the bottom left-corner of the screen.
2. Start > IDT > Timing Commander.
3. Click <Open Setting File>.



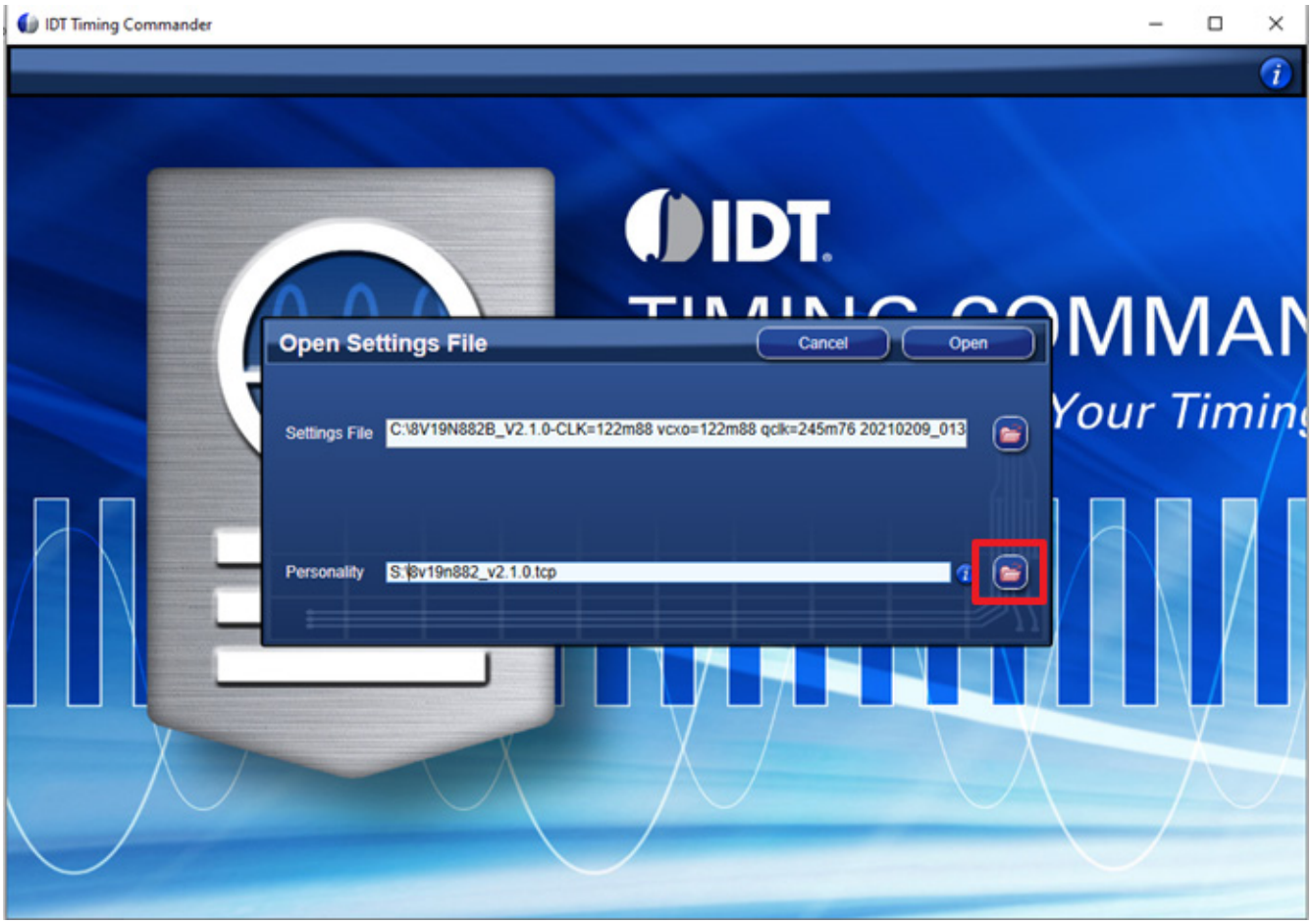
4. For the first-time use, if the proper part number does not appear, click the < Browse> button and choose the settings file from the current working directory.



5. Select the example Timing Commander Settings file (.tcs) from the current working directory.

6. Click the < Browser> button to the choose Personality file from the folder.

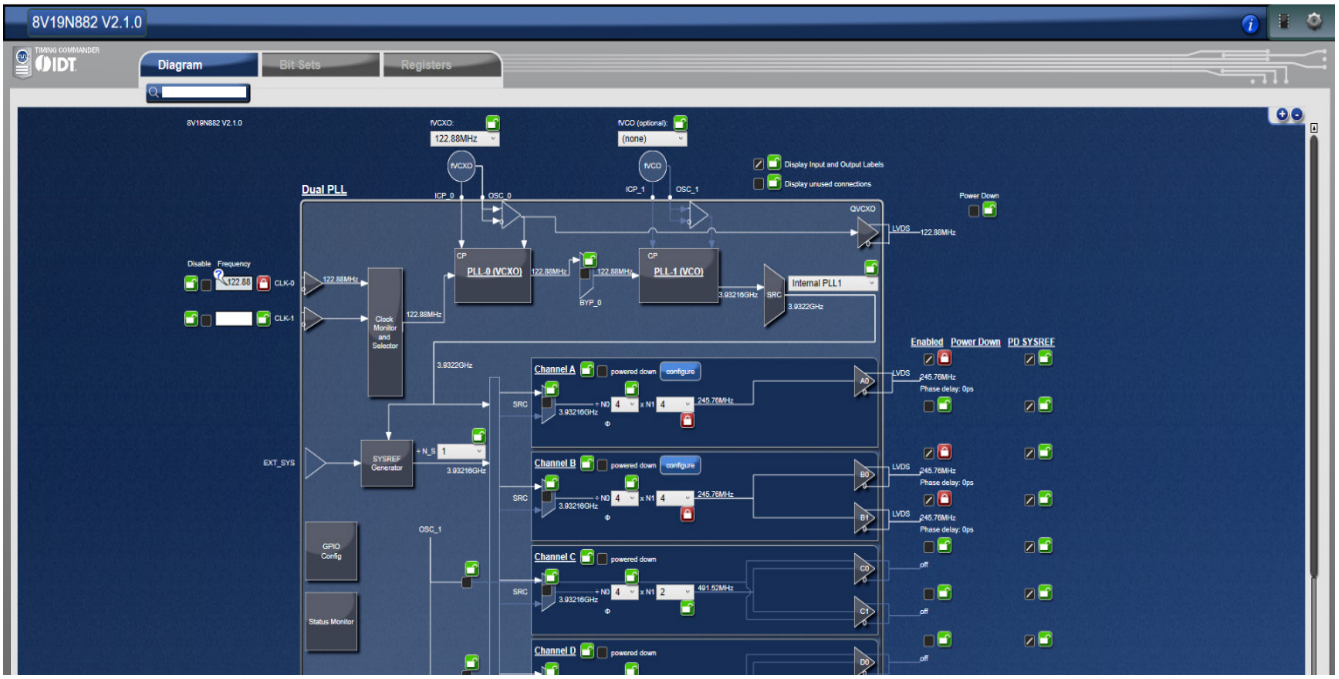
   The latest version of the Timing Commander Personality file (.tcp) can be downloaded from the 8V19N882 webpage.



7. Pick the personality file (.tcp) from the current working directory and click <Open>.

8. Set up example or similar GUI appear as below. Frequencies can be varied (roll the mouse wheel to zoom in/out the display).

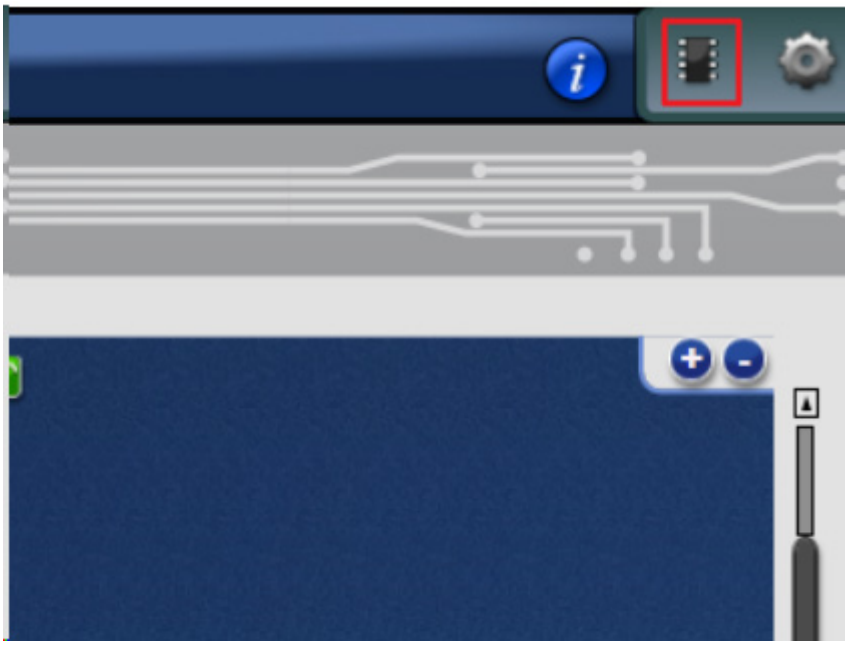
   If needed, the parameters can be modified (e.g., frequencies for input, output, VCO, output driver, charge pump, mux select, etc.).



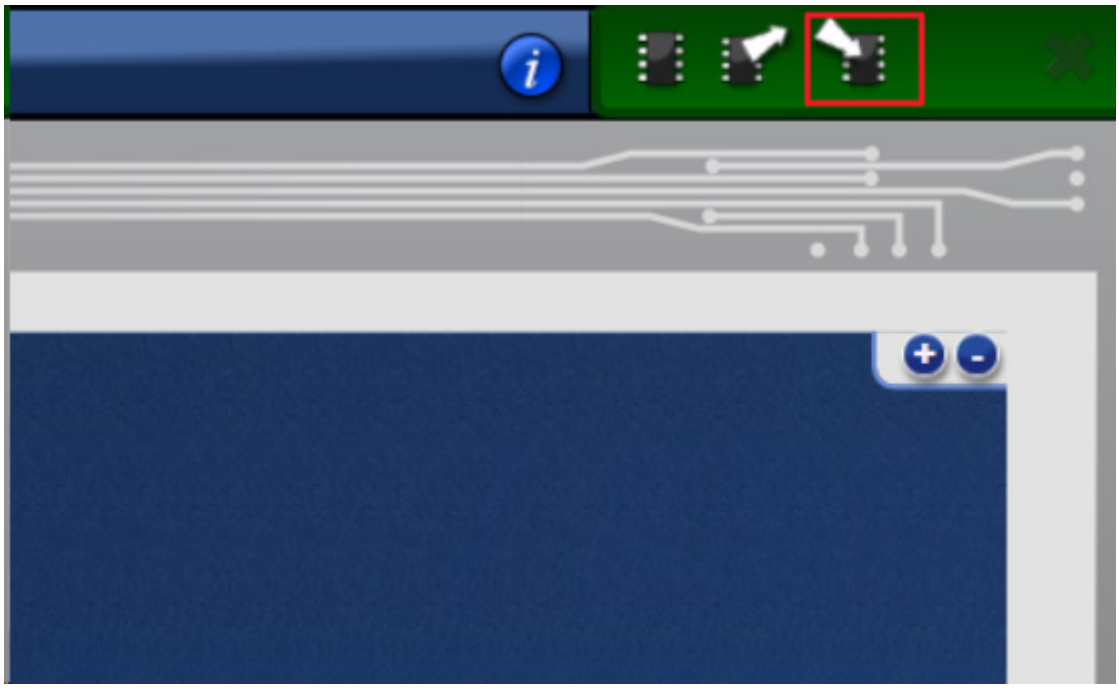
9. Click on any of the blocks to see the lower level block diagram.

1.2.4. Configure the Evaluation Board

1. Click the top right corner chip logo to establish a connection to the evaluation board



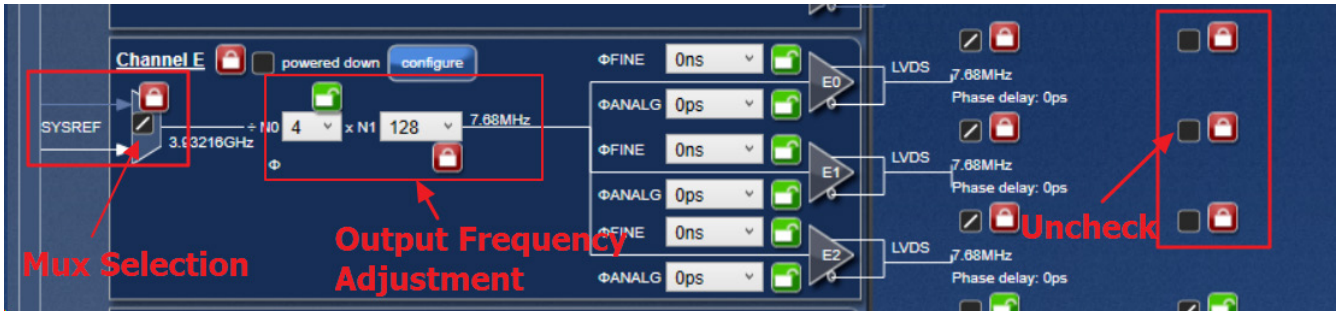
2. Click the arrow pointed down to the chip to write the data to the DUT registers



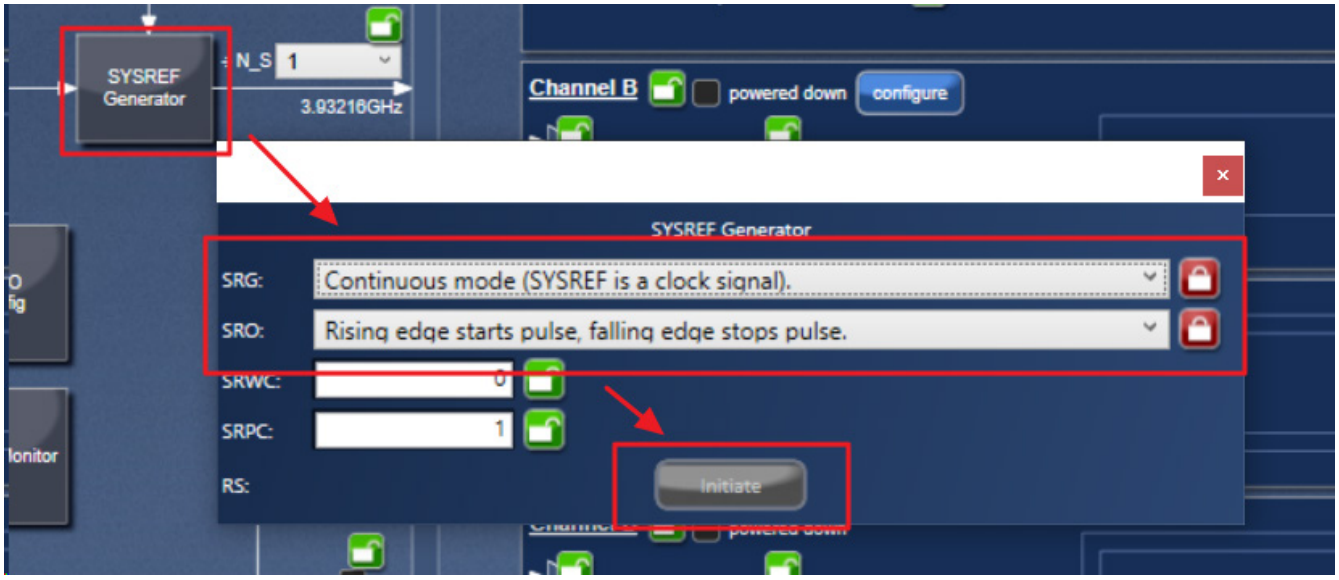
3. Click the <Initialize DUT> to activate the clock output

1.2.5. Sysref Setup

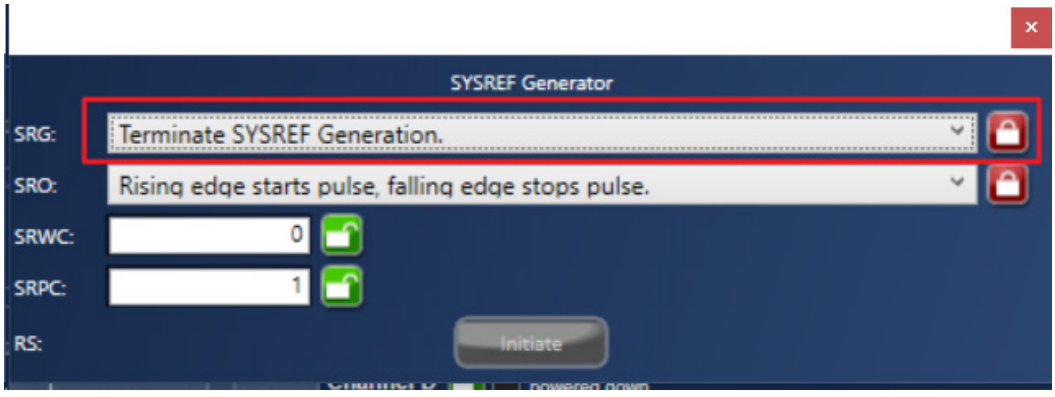
1. Assign output a Sysref Output by select the mux.
2. Set the dividers to generate the desired Sysref frequency.
3. Uncheck the power-down Sysref (PD SYSREF).



4. Click Sysref Generator Block to open the pop-out window.
5. Select the Sysref type from the SRG drop-down menu.
6. Select the pulse type from the SRO drop-down menu.
7. Click on <Initiate> to activate the Sysref output.



8. To Stop the Sysref signal select <Terminate SYSREF Generation> under the SRG drop-down menu.



2. Board Design

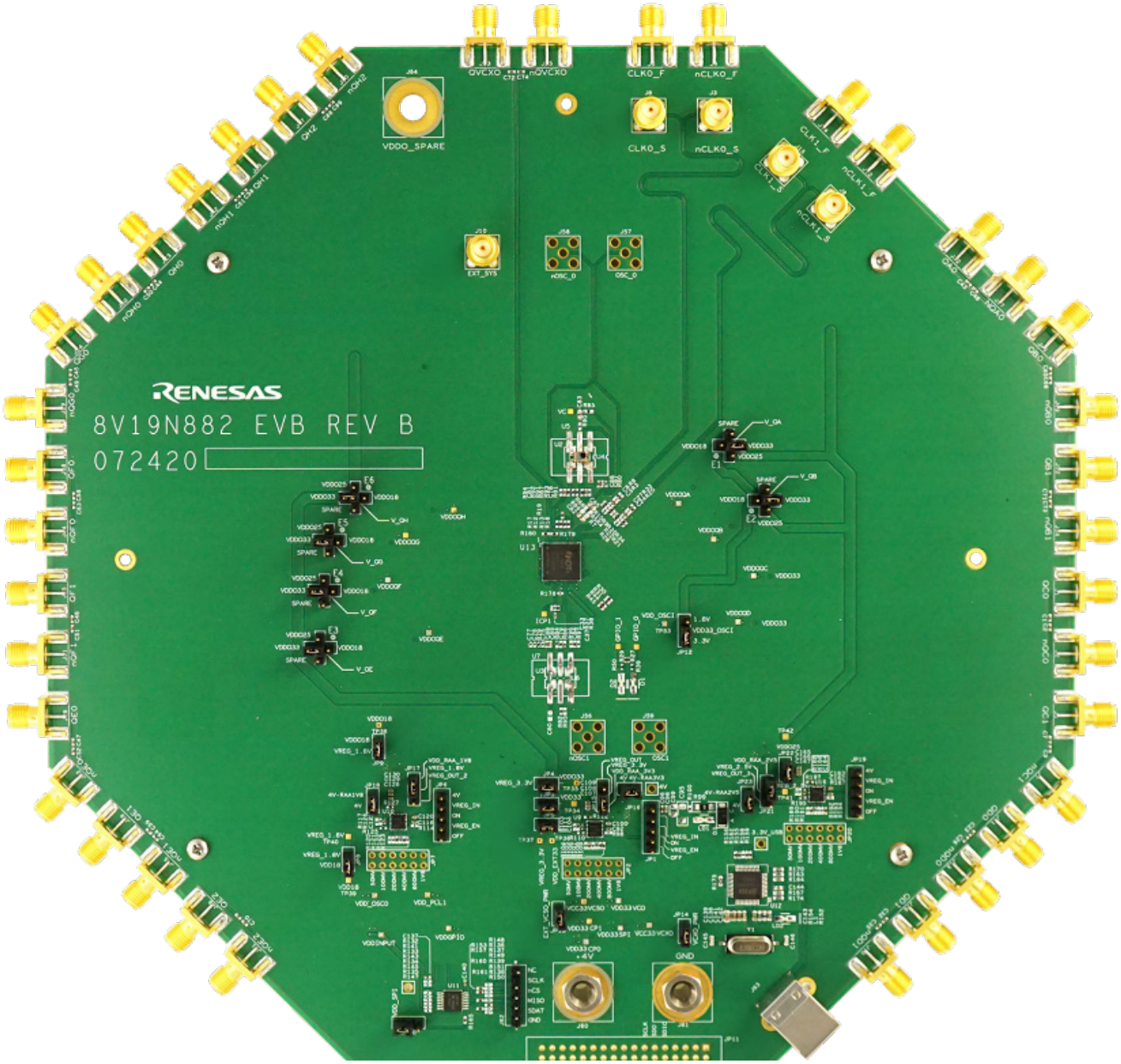


Figure 2. 8V19N882 Evaluation Board (Top)

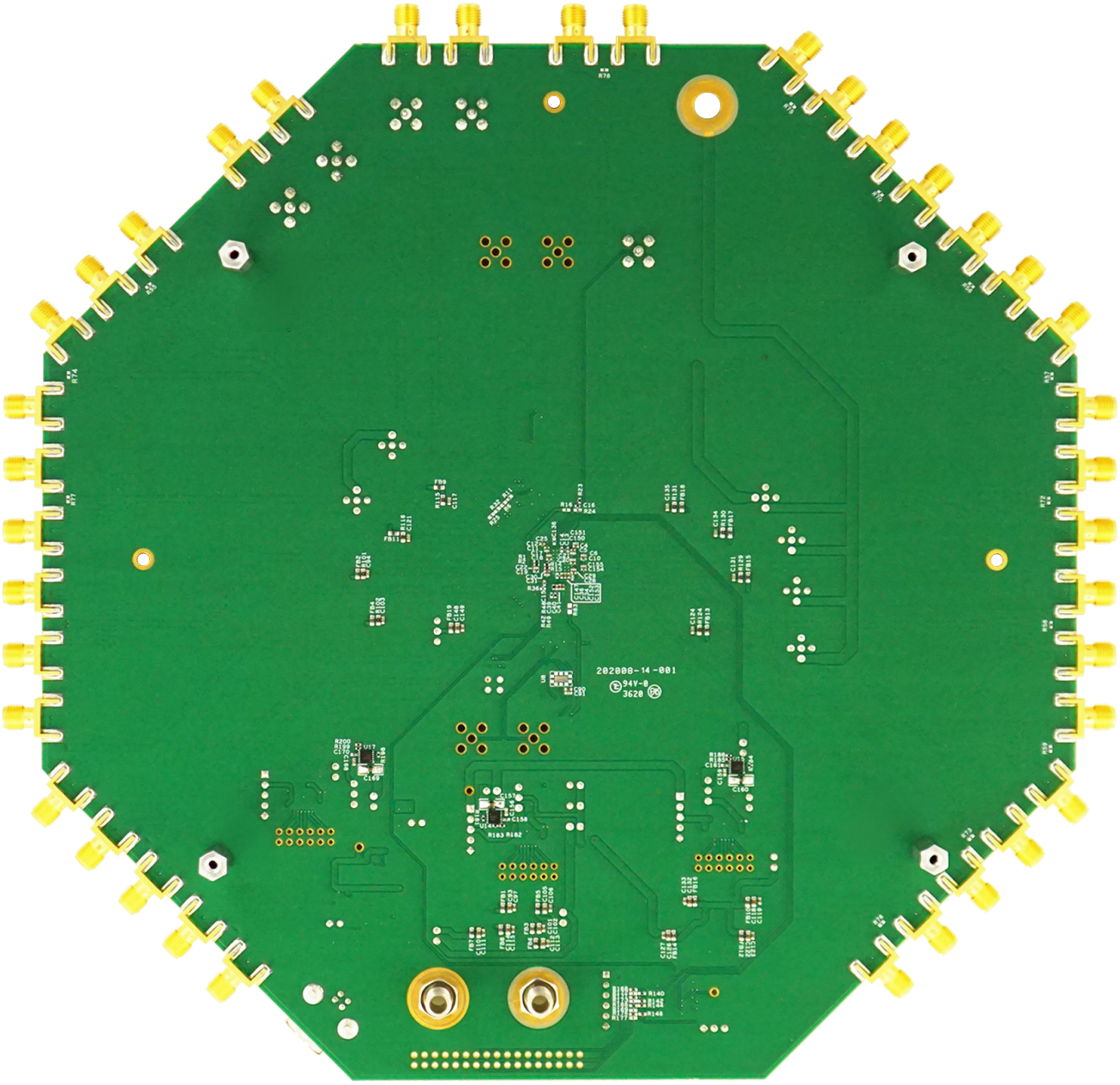


Figure 3. 8V19N882 Evaluation Board (Bottom)

2.1 Schematic Diagrams

For the schematic diagrams, see the end of this document.

2.2 Bill of Materials

Item	Qty	Reference	Part	Manufacturer Part Number
1	40	C1,C2,C3,C7,C8,C9,C23,C24,C27,C26,C32,C35,C43,C44,C45,C46,C47,C48,C49,C50,C51,C52,C56,C58,C59,C61,C63,C64,C65,C66,C67,C68,C69,C70,C71,C72,C73,C74,C78,C81	0.1u	GRM155R71C104KA88D
2	22	C4,C10,C12,C13,C14,C15,C18,C19,C20,C25,C28,C30,C34,C40,C41,C92,C104,C116,C125,C150,C152,C154	0.1u	GRM155R71C104KA88D
3	11	C5,C6,C11,C17,C21,C22,C29,C31,C151,C153,C155	100p	GRM1555C1H101JA01D
4	1	C16	0 Ohm	RMCF0402ZT0R00
5	1	C33	33p	CC0402JRNPO9BN330
6	4	C36, C158, C161, C170	1u	EMK105BJ105KV-F
7	1	C39	22u	CL05A226MQ5QUNC
11	2	C79,C84	0 Ohm	RMCF0402ZT0R00
13	1	C82	0.1u	GRM155R71C104KA88D
14	1	C83	33n	GRM155R71H333KE14D
15	1	C85	10uF	CL05A106MQ5NUNC
16	6	C86,C88,C90,C96, C162, C164	0.1uF	GRM155R71C104KA88D
17	3	C87,C89,C91	100pF	GRM1555C1H101JA01D
18	14	C93,C101,C105,C110,C112,C114,C118,C122,C126,C132,C148, C157, C160, C169	10u	C1608X5R1A106M
19	9	C94,C98,C103,C117,C121,C124,C131,C134,C135	10uF	CL05A106MQ5NUNC
21	11	C97,C102,C106,C111,C113,C115,C119,C123,C127,C133,C149	0.01u	EMK105B7103KV-F
23	15	C100,C107,C108,C109,C120,C128,C129, C130, C156, C159, C163, C165, C166, C167, C168	10u	CL05A106MQ5NUNC
25	2	C137,C140	1.0uF	EMK105BJ105KV-F
26	3	C138,C141,C143	0.1 uF	GRM188R71H104KA93D
27	1	C139	10 uF	C0805X5R100-106KNE
28	1	C142	10000PF	GRM188R71H103MA01D
29	1	C144	0.047 uF	C0402X7R160-473KN
30	2	C145,C146	33PF	GRM1885C2A330JA01D
32	3	LD1,D1,D2	LED, Green, Vf=1.7V	LG L29K-F2J1-24-Z
33	1	D3	CGRA4004-G	CGRA4004-G
34	19	FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8,FB9, FB10,FB11,FB12,FB13,FB14,FB15,FB16,FB17,FB18,FB19	FERRITE_BEAD	BLM18BB221SN1D

Item	Qty	Reference	Part	Manufacturer Part Number
35	3	JP1,JP6, JP19	Header_5Pin	TSW-105-07-F-S (or TSW-103-07-F-S + TSW-102-07-F-S)
37	11	JP3,JP4,JP5,JP8,JP9,JP13, JP16, JP18, JP22, JP23,JP14	Header_2Pin	TSW-102-07-F-S
38	4	JP10, JP15, JP17, JP21	LVL_SHIFT_EN	TSW-103-07-F-S
40	1	JP12	VDD_OSCI	TSW-103-07-F-S
41	38	J1,J2,J4,J5,J6,J7,J11,J12,J13,J14,J16,J18,J22,J23,J24,J25,J26,J27,J29,J30,J31,J32,J36,J38,J39,J42,J44,J45,J46,J47,J48,J49,J50,J51,J52,J53,J54,J55	SMA_END_LAUNCH_PCB_375_PIN	142-0701-801
42	5	J3,J8,J9,J10,J15	SMA_STRAIGHT	142-0701-201
44	1	J60	+4V	108-0740-001
45	1	J61	GND	108-0740-001
46	1	J62	22-28-4062	22-28-4062
47	1	J63	USB Port	897-43-004-90-000000
48	1	LD2	LED, Green, Vf=1.7V	LG L29K-F2J1-24-Z
49	1	L1	600 Ohm 500mA	BLM18AG601SN1
50	10	R1,R2,R14,R15,R30,R31,R44,R45,R179,R180	150	RC0402FR-07150RL
51	26	R3,R8,R19,R20,R33,R87,R91,R105,R108,R109,R112,R120,R122,R127,R153,R157,R160,R161,R162,R166,R168,R171,R176,R190, R194, R197	0	RMCF0402ZT0R00
52	2	R4,R5	5.1k	ERJ-2GEJ512X
55	16	R9,R10,R34,R35,R110,R125, R181, R183,R184, R185, R186,R156,R158, R195,R198. R200, R159	10K	ERJ-2RKF1002X
56	2	R12,R13	82.5	ERJ-2RKF82R5X
58	2	R17,R18	133	RC0402FR-07133RL
59	2	R21,R22	5.1k	ERJ-2GEJ512X
60	1	R23	49.9	ERJ-2RKF49R9X
61	2	R27,R29	100	ERJ-2RKF1000X
63	1	R38	220	ERJ-2RKF2200X
64	2	R39,R50	1k	ERJ-2RKF1001X
65	1	R46	1	ERJ-2GEJ1R0X
66	1	R49	49.9	ERJ-2RKF49R9X
68	1	R79	0	RMCF0402ZT0R00
70	2	R82,R100	1K	ERJ-2RKF1001X
72	1	R85	1k	ERJ-2RKF1001X

Item	Qty	Reference	Part	Manufacturer Part Number
73	1	R88	2K	ERJ-2RKF2001X
74	2	R92,R93	180	ERJ-2RKF1800X
75	1	R99	0	RC1206JR-070RL
76	8	R101,R102,R115,R116,R124,R129,R130, R131	2	ESR03EZPJ2R0
78	5	R140,R142,R144,R146,R165	100	ERJ-2RKF1000X
79	1	R151	33	ERJ-2RKF33R0X
80	1	R152	680	ERJ-3GEYJ681V
81	1	R154	470	ERJ-3GEYJ471V
82	2	R163,R164	27	ERJ-3GEYJ270V
83	1	R167	1.5K	ERJ-3GEYJ152V
85	3	R170,R174,R175	10K	RC0603FR-0710KL
96	3	U9,U10, U16	TPS7A8300	TPS7A8300ARGRT
97	1	U11	LSF0204PWR_TSSOP14	LSF0204PWR
98	1	U12	ft2232_chip	FT2232D
99	1	U13	8V19N882	
100	1	Y1	6MHz	ECS-60-32-5P
101	6	E1, E2, E3, E4, E5, E6	5 pin header	TSW-103-07-F-S TSW-102-07-F-S
102	1	R182	26.7k	ERJ-2RKF2672X
103	1	R199	17.8k	ERJ-2RKF1782X
104	3	U14, U15, U17	LDO	RAA214020
105	1	C37	47nF	GRM155R71C473KA01J

3. Typical Performance Graphs

The following figure shows example phase noise performance from the loaded example configuration.

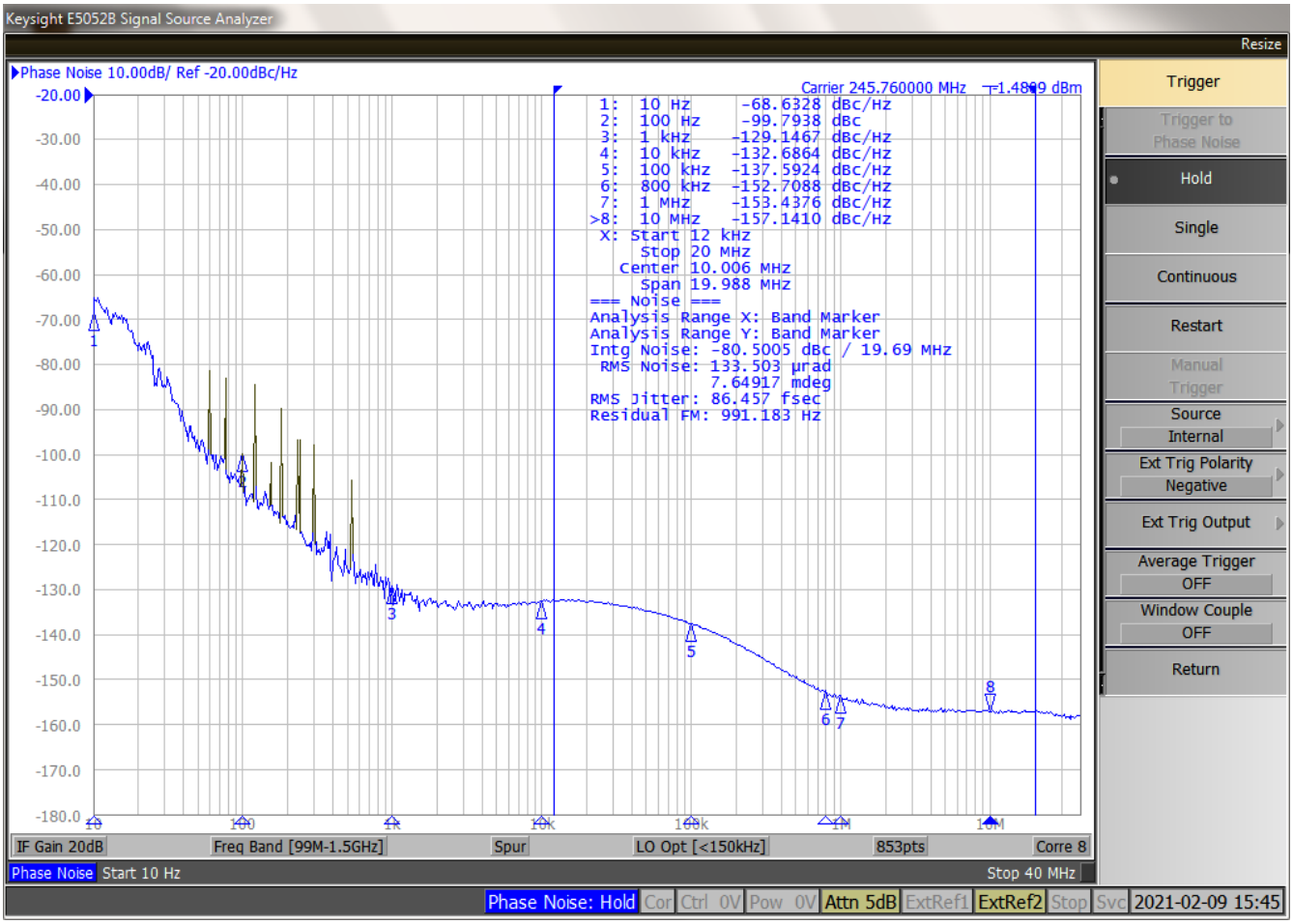


Figure 4. Example Configuration Phase Noise

4. Ordering Information

Part Number	Description
8V19N882-EVK	8V19N882 Evaluation Board

5. Revision History

Revision	Date	Description
1.0	Mar 30, 2021	Initial release.

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