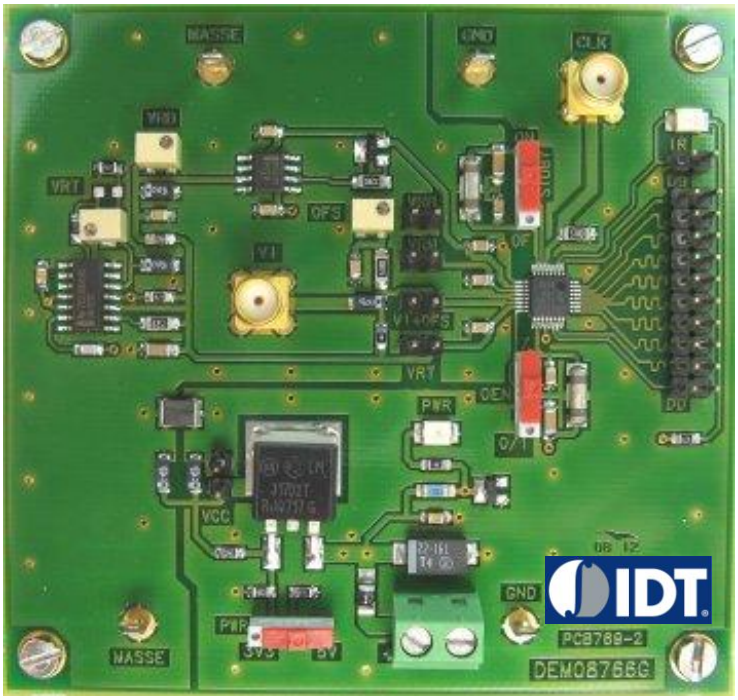
Quick Start

DEMO8766G Demonstration Board for ADC1002S020

Rev. 2.0 — 2 July 2012 **Quick Start**

Document information

Info	Content
Keywords	DEMO8766G, PCB769-2, Demonstration board, ADC, Converter, ADC1002S020
Abstract	This document describes how to use the demonstration board DEMO8766G for the analog-to-digital converter ADC1002S020.
Overview	

Revision history

Rev	Date	Description
2.0	20120702	Rebranded.
0.1	20080612	Initial version.

1. Quick start

1.1 Setup overview

Figure Fig 1 presents the connections to measure DEMO8766G.

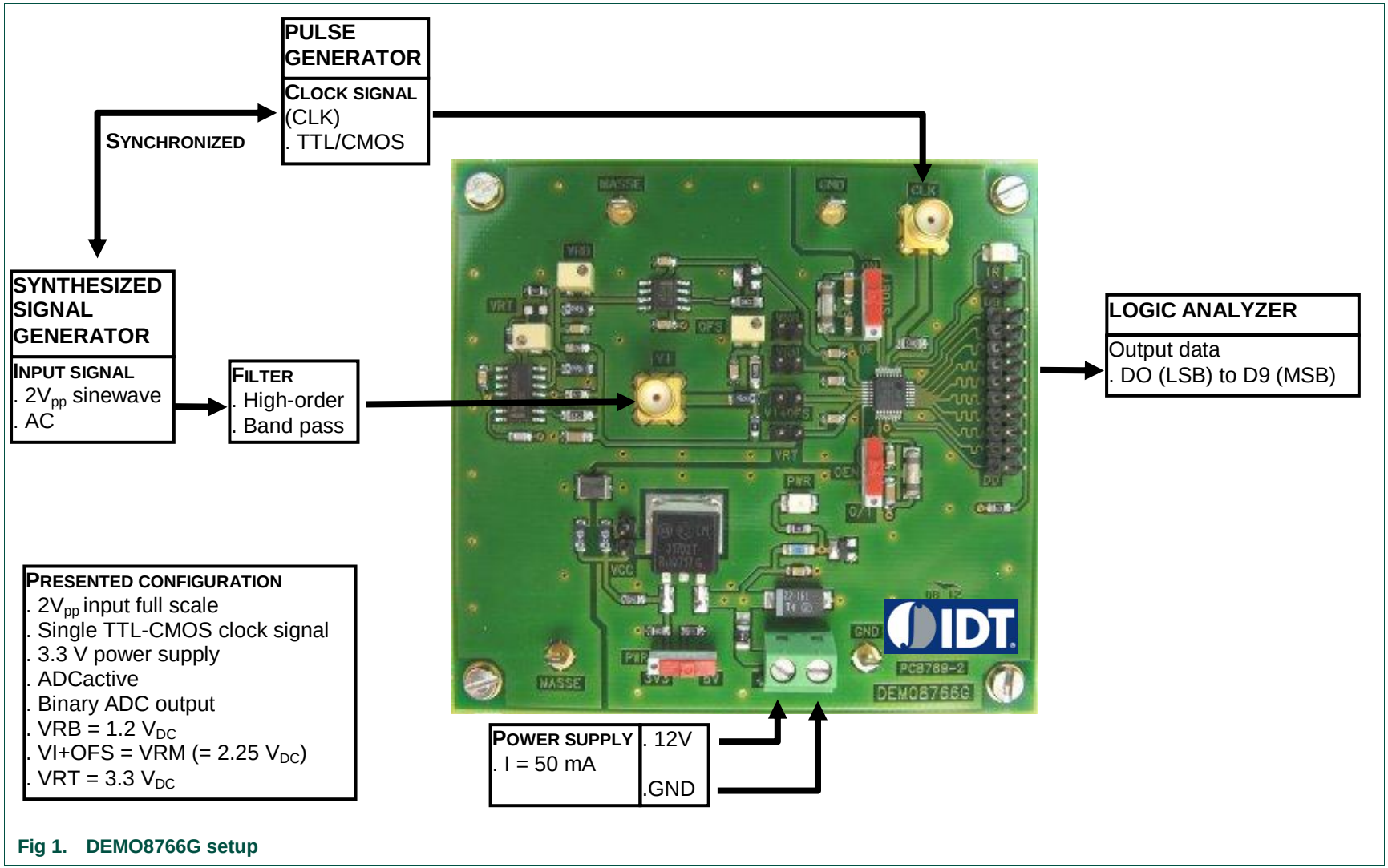
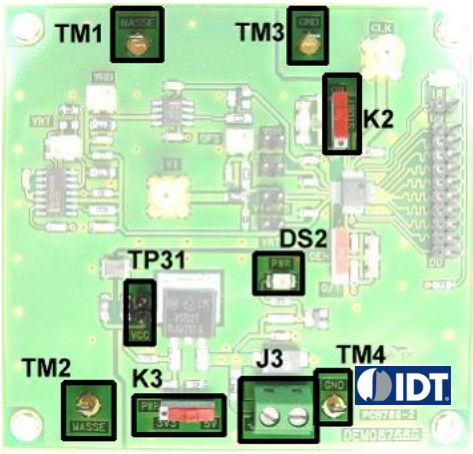


Fig 1. DEMO8766G setup

1.2 Power supply

The board is powered with a single 12 V_{DC} power supply. A power supply regulator is used to supply all the circuitry on the board.

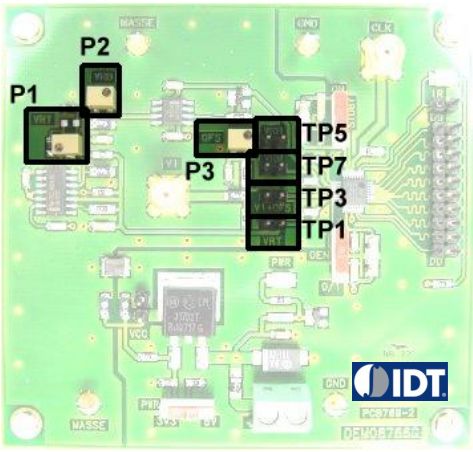
Table 1. General power supply

Name	Function	View
J3	Green connector – Power supply 12 V_{DC} / 50 mA.	
DS2	PWR green light – It indicates the good supply plugging	
K3	PWR switch – ADC power supply selection  3.3 V  5 V	
TP31	VCC test point – ADC power supply	
TM1, TM2	MASSE test point – Analog ground	
TM3, TM4	GND test point – Digital ground	
K2	STDBY switch – ADC stand-by activation ADC active  ADC OFF 	

1.3 DC voltage adjustments

The ADC1002S020 allows to adjust the full scale input signal from 1.6 V to 2.4 V.

Table 2. DC voltage adjustments

Name	Function	View
P1	VRT trimmer – TOP reference adjustment	
TP1	VRT test point – TOP reference value (typ 3.3 V)	
P2	VRB trimmer – BOT reference adjustment	
TP5	VRB test point – BOT reference value (typ 1.2 V)	
P3	OFS trimmer – Input signal DC offset adjustment	
TP3	VI+OFS test point – Input signal DC offset (typ 2.25 V)	
TP7	VRM test point – MIDDLE reference value (typ 2.25 V)	

1.4 Input signals (VI, CLK)

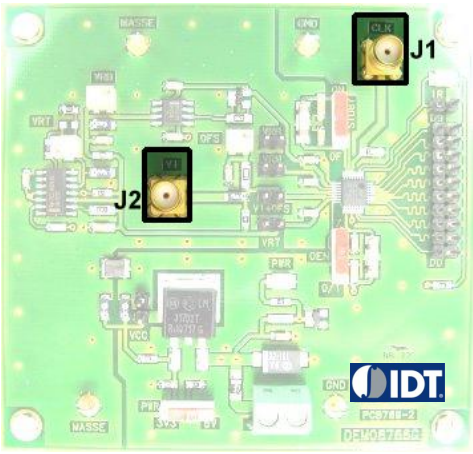
To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

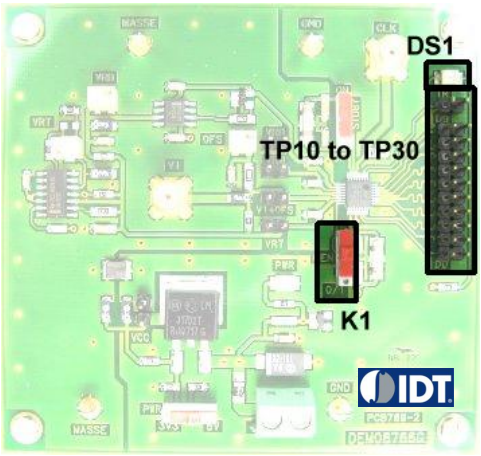
, where M is an odd number of period and N is the number of samples.

Table 3. Input signals

Name	Function	View
J2	VI connector – Analog input signal (50Ω matching)	
J3	CLK connector – Clock input signal (50Ω matching)	

1.5 Output signals (D0 to D9, IR)

Table 4. **Output signals**

Name	Function	View
TP10 to TP30	Array connector – ADC digital output(D0 to D9) and In range signal (IR)	
DS1	IR green light – It indicates that the analog input signal is in the full scale range	
K1	OEN switch – Output enable selection Active output  High impedance output 	

2. Example

2.1 Setup example

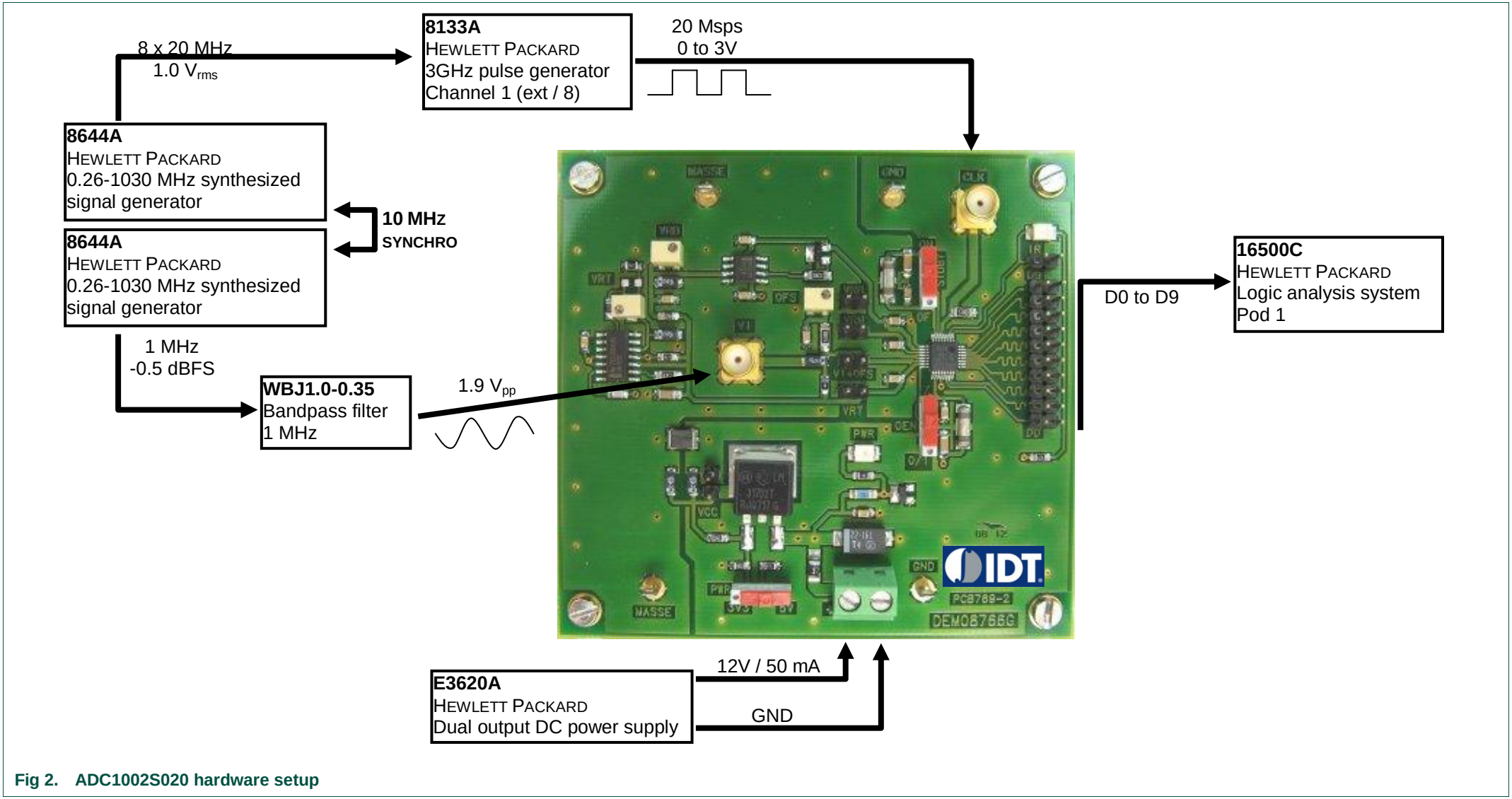


Fig 2. ADC1002S020 hardware setup