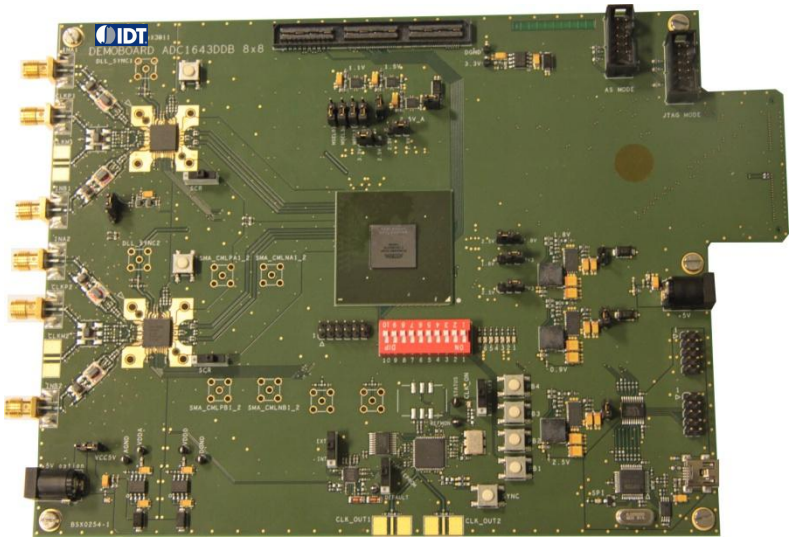
Quick start ADC1x43D DB

Demonstration board for ADC1443D series

Rev. 02 — 2 July 2012 **Quick start**

Document information

Info	Content
Keywords	ADC1x43D DB,ADC1X43xxxW1DB, ADC1443D series, demonstration board, ADC, Converter,JESD204B, BSX0254.
Abstract	This document describes how to use the demonstration board ADC1443D DB for the analog-to-digital converter ADC1443D dual channel ADC with JESD204B interface.
Overview	

The Board is available in 3 version 125, 160 and 200 Msps sampling rate, with relative naming ADC1443D125W1/DB; ADC1443D160W1/DB; ADC1443D200W1/DB

Revision history

Rev	Date	Description
1	17th October 2011	Initial version
2	2 July 2012	Rebranded

Revision history

1. Overview of the demo board ADC1x43D DB

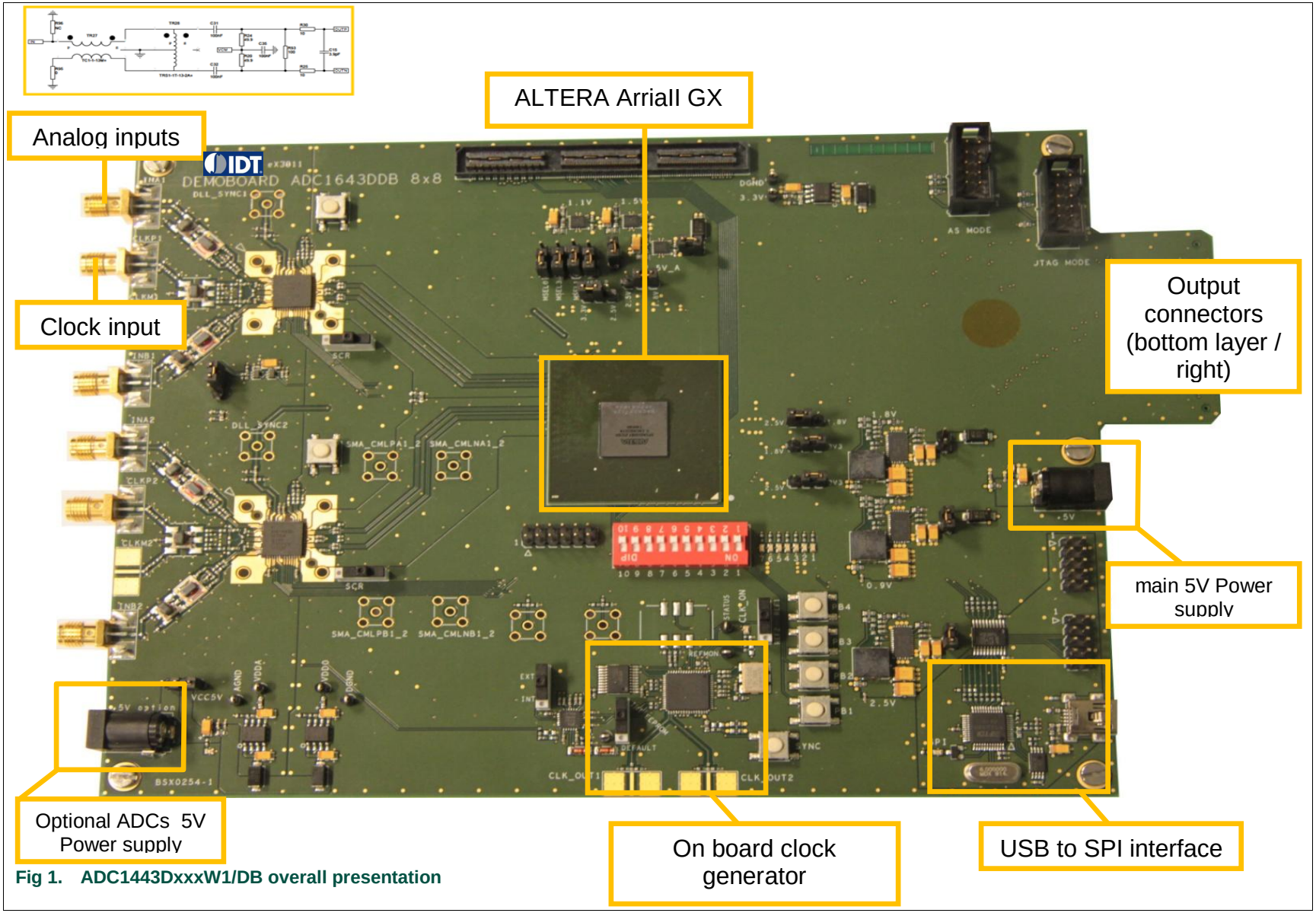


Fig 1. ADC1443DxxxW1/DB overall presentation

2. Switch and Jumpers default state

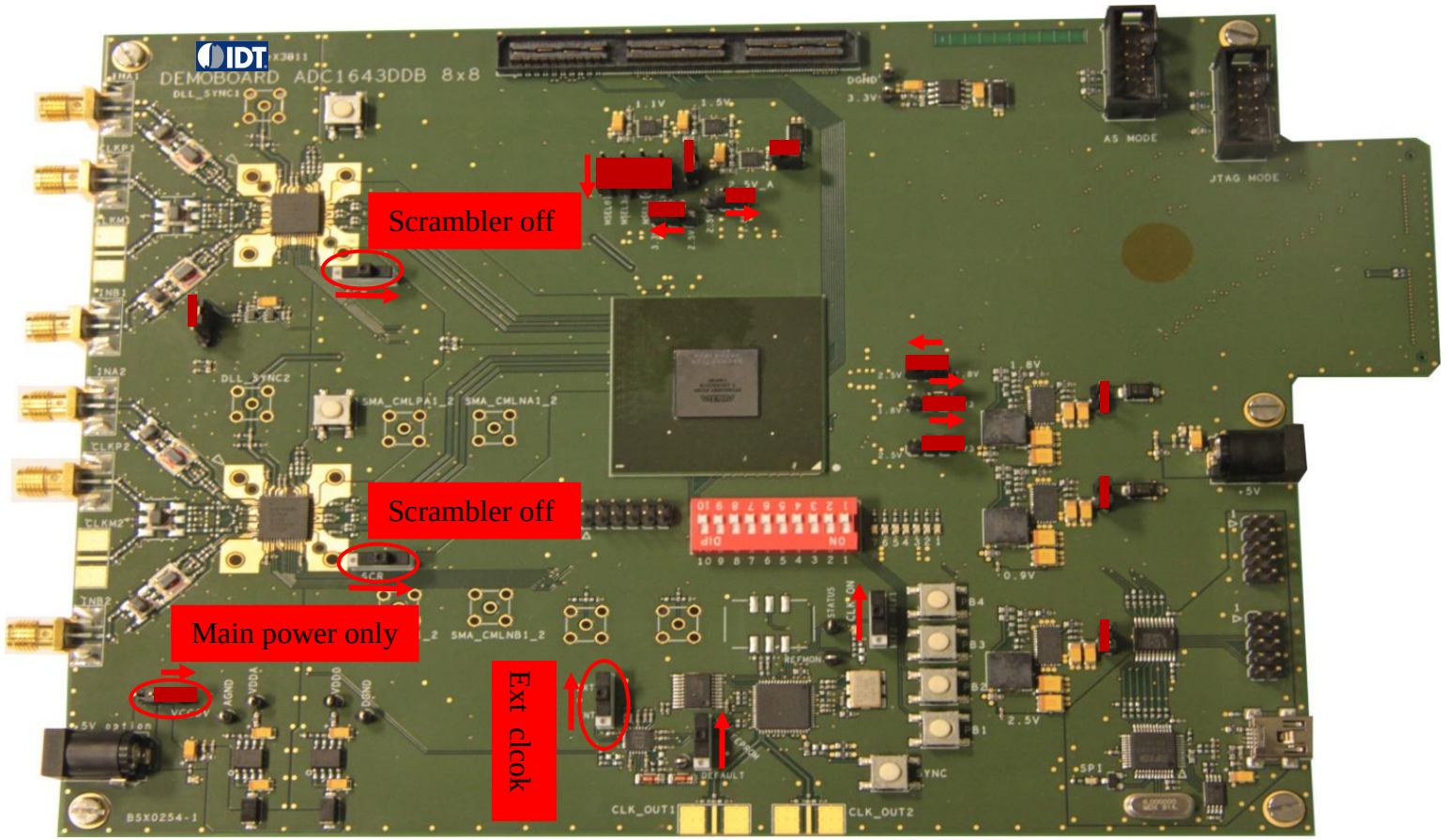


Fig 2. Overall presentation of default switchs and jumpers

3. Board goal and general description

The ADC1443DxxxW1/DBboard is aimed to provide a full and complete set to evaluate and demonstrate the ADC1x43D series, analog to digital converters, compliant with JESD204B JEDEC serialize tion standard.

- **The ADCs**

The board embeds 2 dual ADC devices both connected to the ALTERA ArriaII GX FPGA to de-serialize the ADC output according to the JESD204B physical and protocol layer.

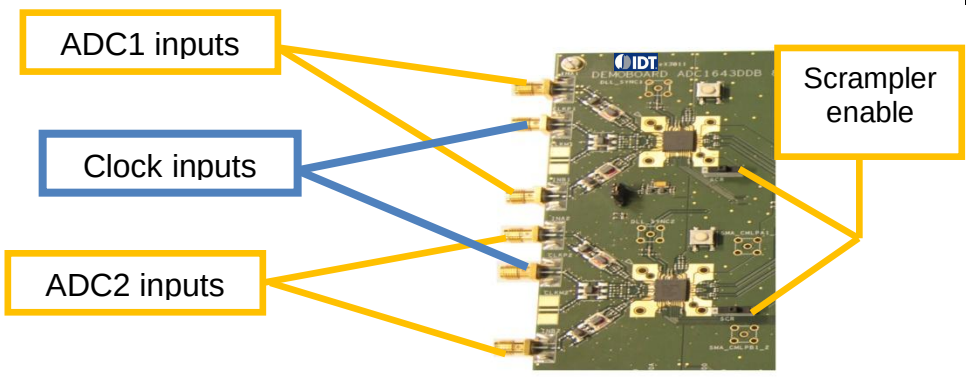


Fig 3. Analog and clock inputs

Each ADC is dual channel and need to be fed with single ended input (from SMA connector).

Input clock is also single ended when using an external clock generator.

- **The Clock Generator**

An embedded clock generator is also on the board. The HSDC_SW_ADC_4.exe application allow to configure and control the clock generation.

When using it, some PCB soldering modification needs to be operated on the board (see board schematic for more information).

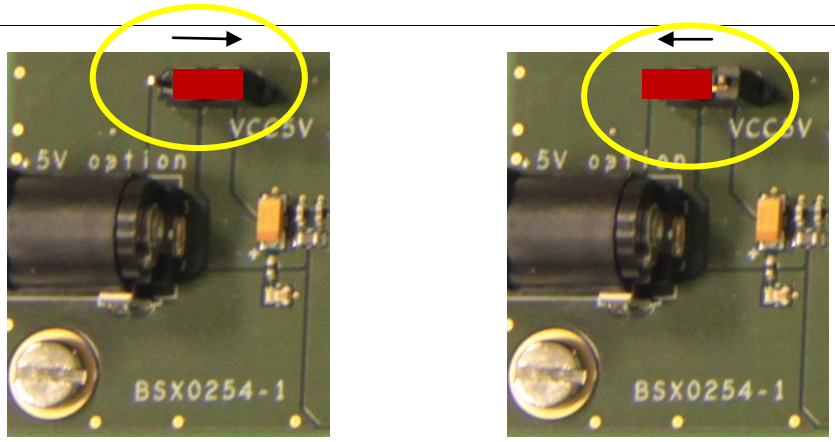
The default configuration is for use with external clock generator, and hence, main selector Jumper J301 has to be set to “EXT” position.

- **Power supplies**

The board embeds two 5V power supplies connector (one main, on right side to power-up all the board components, and a second optional, on the left side of the board, to power-up the ADCs linear regulators.

Selection of the 5V that power the ADCs regulators is done through the Jumper VCC5V.

When Jumper is set to the right (see figure 4), only powering from main connector is required



(A) (B)

Fig 4. Jumper VCC5V in one single 5V supply (A) and in two 5V power schemes(B)

Other jumpers are kept on their default value.

Best SNR performances are seen when using separate power supplies for ADC, since the Switching FPGA power supplies add some noise to the supplies layers

- **Receiving the serial pattern**

The AriiaII GX FPGA is provided with Binary code already burned in internal 64M serial EEPROM memory (bottom side), both FPGA and the EEPROM are accessible via the 2 connectors AS MODE and JTAG mode.

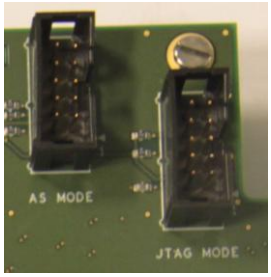


Fig 5. AS mode and JTAG mode connector

To operate any FPGA programming, you need to get the free Quartus tool from ALTERA and the ALTERA USB BLASTER that you plug to either AS Mode connector, when

burning to the Active Serial EEPROM or to JTAG Mode when accessing directly the FPGA.

The FPGA is responsible for de-serializing the serial stream coming From the ADC, according to the JESD204B standard.

Since we have 2 dual ADC on the board, each with 2 lanes,the HSDC_SW_ADC_4.exe application allow to configure the FPGA and to choose which channel, ADC, lanes we are talking to.

FPGA is accessible via SPI and also though some GPIO (DIP switch SW700) and push button PB1 to PB4.

Main used are Dip switch “1” to allow Scrambling in the FPGA and PB3 to do a manual FPGA reset.

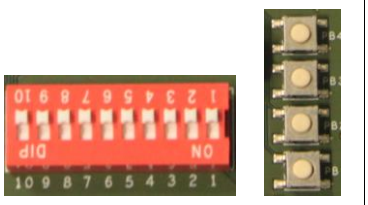


Fig 6. DIP Switch and Push Button

LED Information from the FPGA are available also,

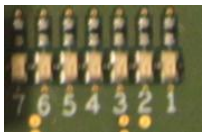


Fig 7. 8 LED from FPGA

LED 7 and 8 show , when toggling , that ADC is fed with clock and that CDR (clock and data recovery) is operating.

LED 5, shows SPI activity when FPGA is selected.

Once the FPGA has decoded the Serial stream, It is stocked into a size variable internal memory (from 4K to 64k) and could be uploaded via SPI-to-USB to the HSDC_SW_ADC_4.exe application and displayed as an FFT with all relevant information extracted.

Digital parallel pattern could be send in LVDS DDR ou LVCMOS to a Sametc output connector (on the bottom side of the board) if the user want to connect an external acquisition system.

Addition High speed mezzanine connector (HSMC) is connected to the FPGA Tx and Rx SerDes and could allow plugging an extension board.

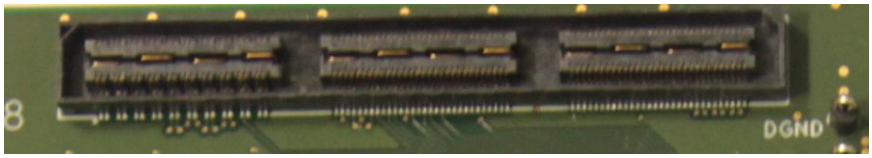


Fig 8. HSMC female connector for extension board

- **USB interface**

The USB interface acts like a programming interface.

The main chip is an FTDI FT2232D that interface the USB Physical layer to the SPI interface for the Two ADCs and the clock generator.

The Board comes with the HSDC_SW_ADC_4.exe application that controls all these components via USB.

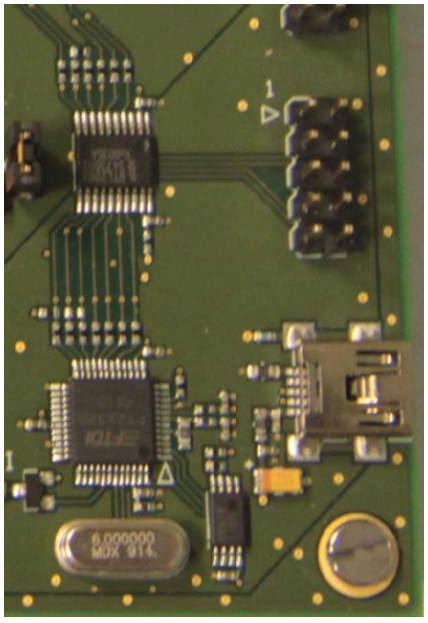
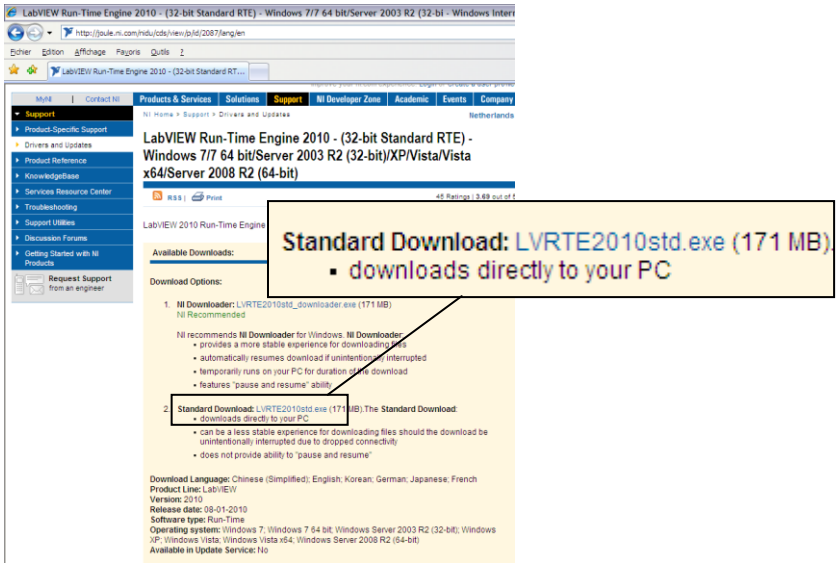
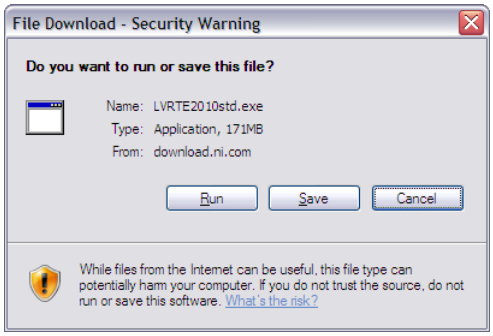


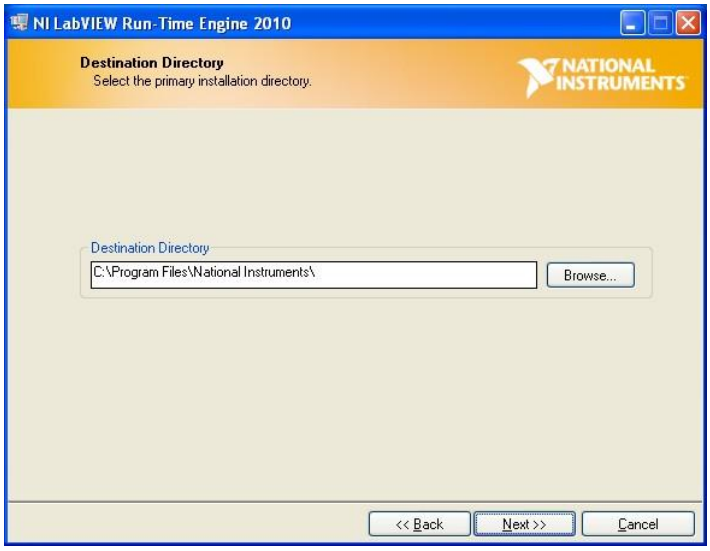
Fig 9. USB-to-SPI interface

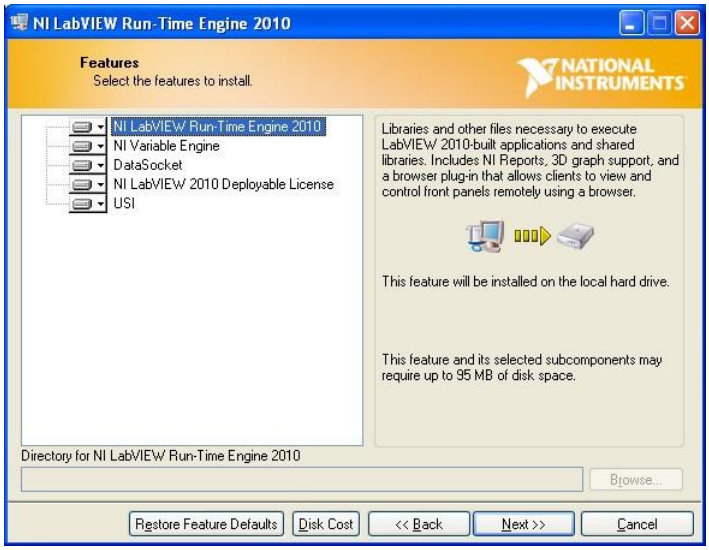
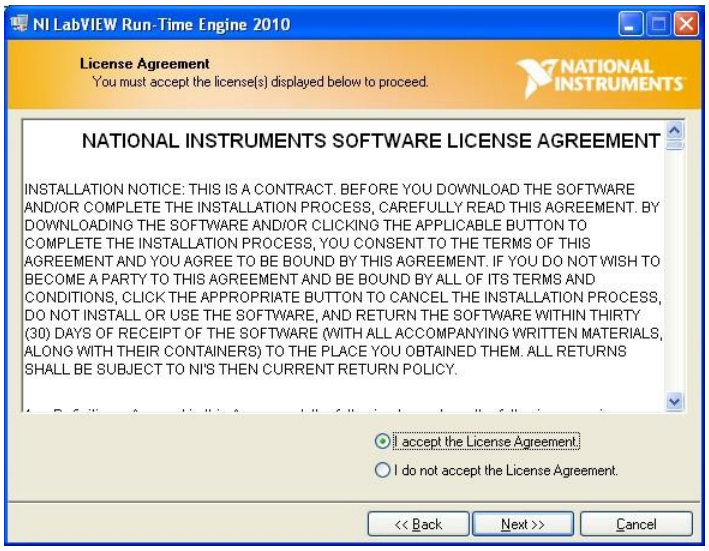
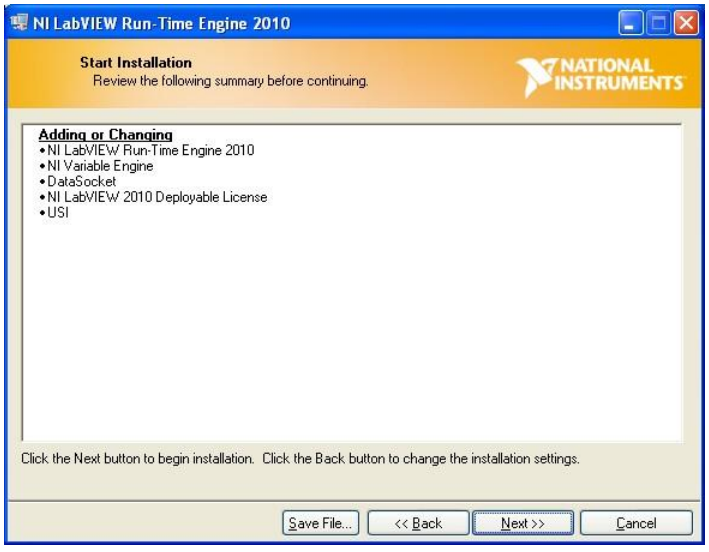
Further instructions on how to install and operate the software are detailed in next section.

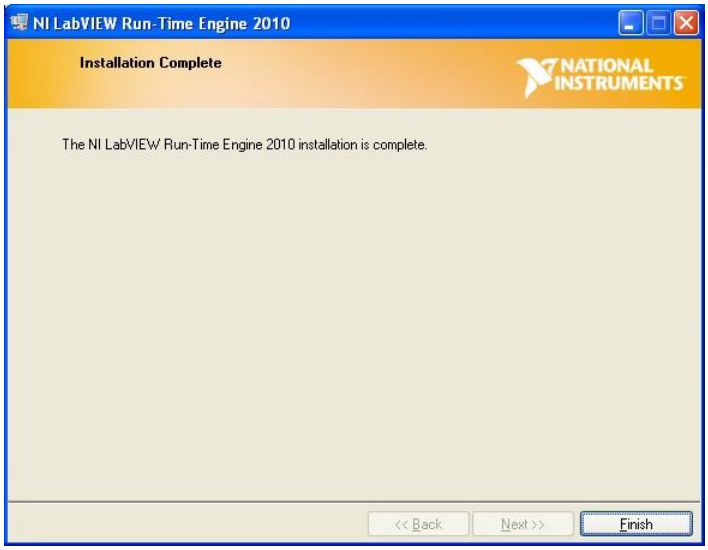
4. Software and drivers install

4.1 Labview Runtime 2010 install

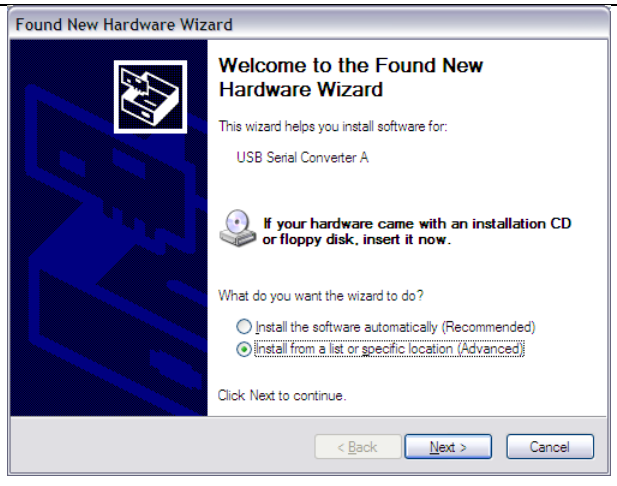
1	Go to National Instruments web page http://joule.ni.com/nidu/cds/view/p/id/2087/lang/en	
2	Download 'LVRTE2010std.exe'	
3	Save	
4	Run the application 'LVRTE2010std.exe'	
5	OK	
6	Unzip	

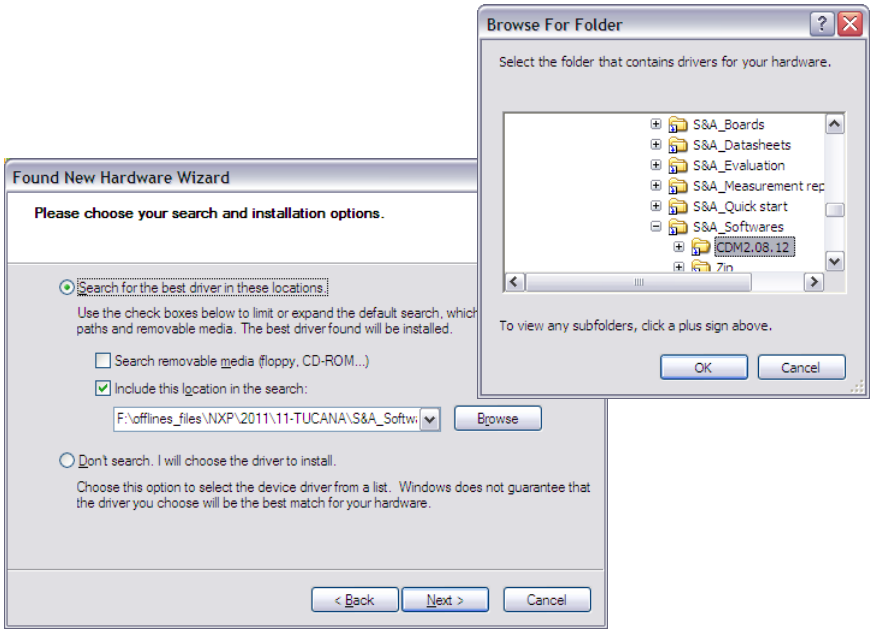
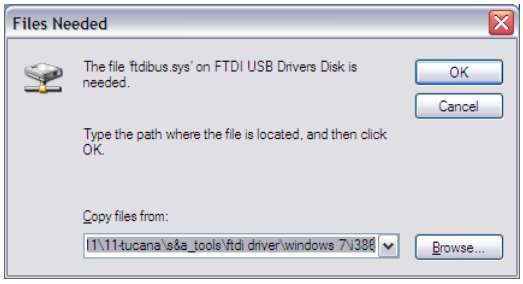
7	OK	
8	Next	
9	Next	

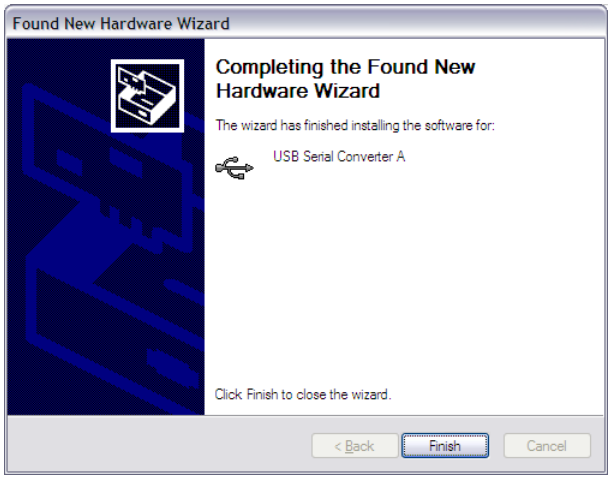
10	Next	
11	Select '**I accept the License Agreement**' Next	
12	Next	

13	Finish	
14	Restart	

4.2 Demoboard - USB-SPI driver install

1	Plug the USB cable in the demoboard USB connector	
2	The wizard will help to install the USB Serial Converter A	
3	Select '**Install from a list or specific location**' Next	

4	Select '**Search for the best driver in these locations**' Select '**Include this location in the search**' Browse Select the folder '**CDM2.08.12**' Next	
5	Continue Anyway (Windows XP only)	
6	Browse Select the file '**ftdibus.sys**' in the folder '**CDM2.08.12\i386**' OK	

7	Finish	
8	The wizard will help to install the USB Serial Converter B (same as USB Serial Converter A)	
9	The wizard will help to install the USB serial port The file '**ftser2k.sys**' is in the folder '**CDM2.08.12\i386**'	

5. ADC acquisition tool

5.1 Software start-up

To install the software, please refer to appendix A ‘Software and drivers install’.

Run the application “HSDC_SW_ADC_4.exe”. This application will allow:

- the user to control features through the SPI;
- as well as performing any online data acquisition to evaluate the performances.

5.2 Start-up screen

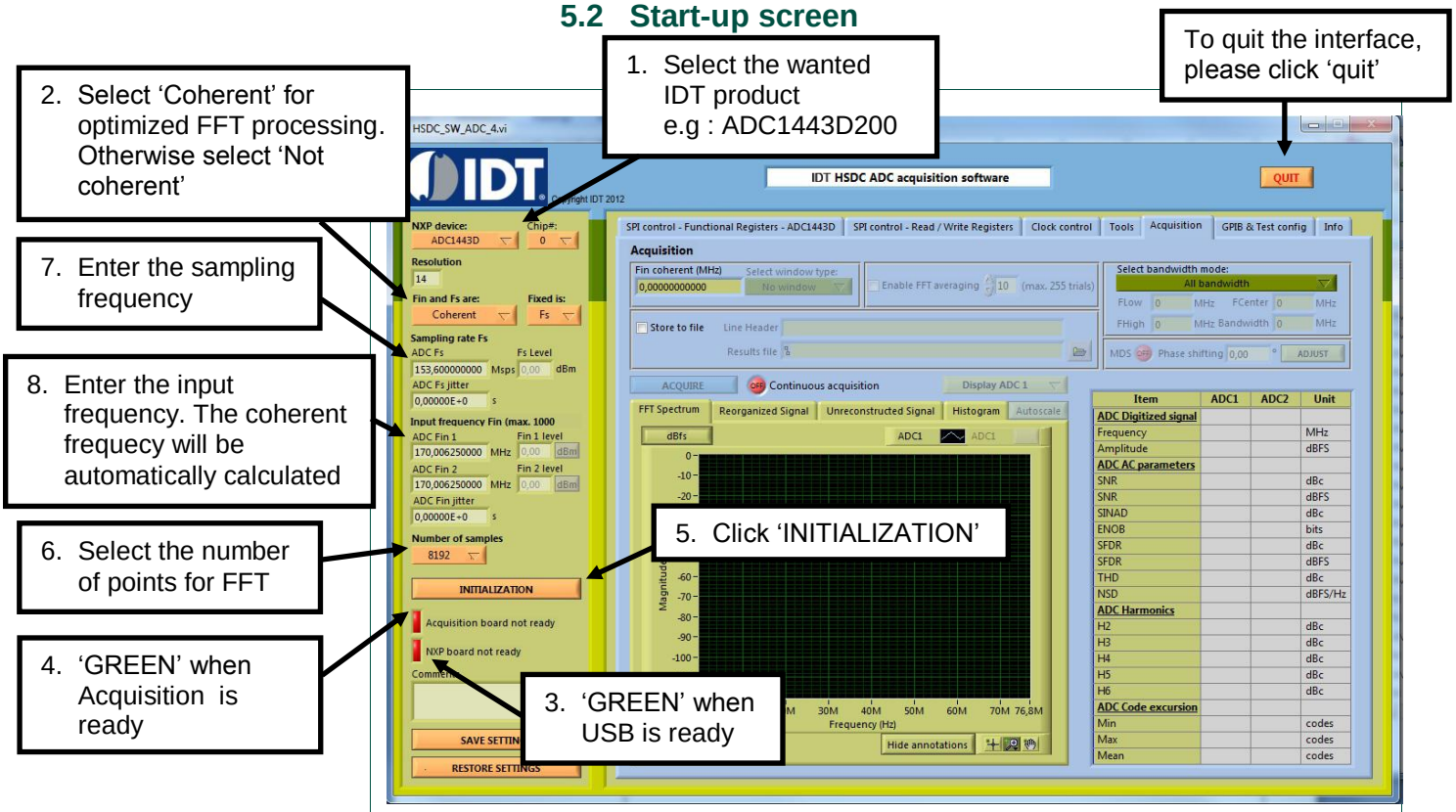


Fig 10. Start-up screen

5.3 Read / Write Registers

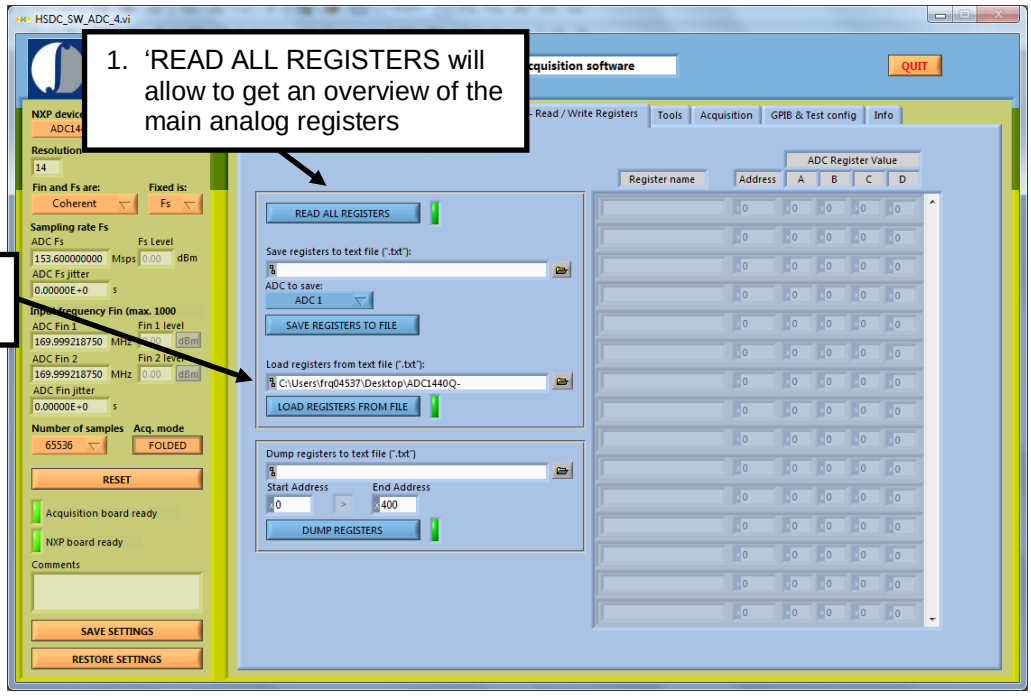


Fig 11. Read / Write Registers

5.4 Functional Registers

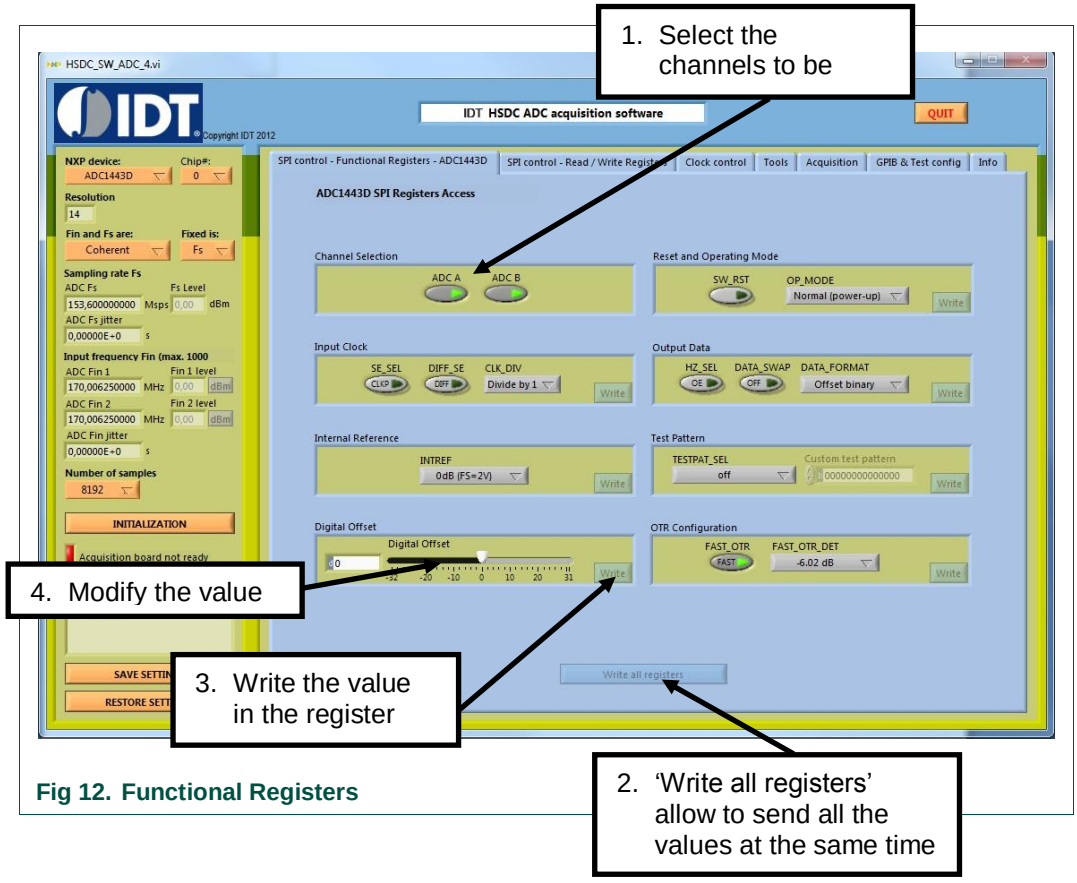


Fig 12. Functional Registers

5.5 Acquisition

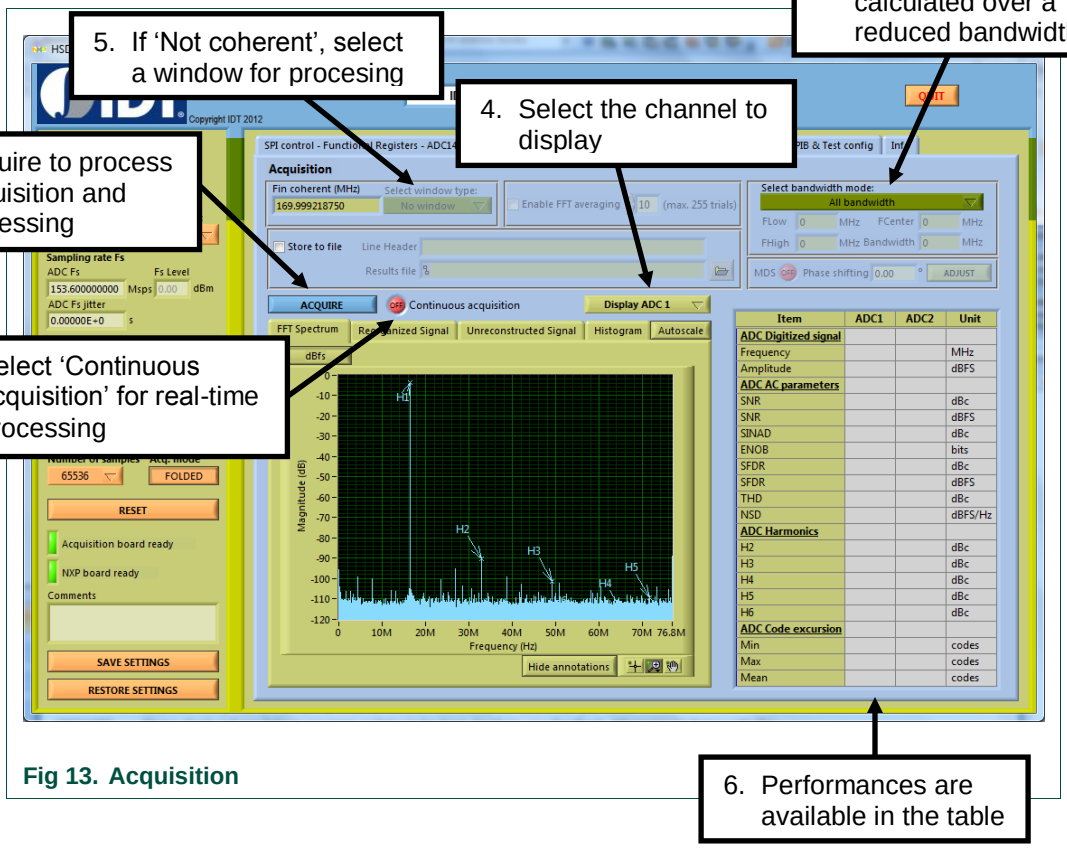


Fig 13. Acquisition

If you have a bad acquisition (especially when changing the frequencies), an FPGA hardware reset, pushing and releasing the PB3, is needed.