RC32312A

Evaluation Board Manual

This document describes the following topics about the RC32312A evaluation board:

- Basic hardware and GUI setup
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file
- Hardware modifications require for different conditions

Features

- Four differential clock inputs
- Twelve differential clock outputs
- On-board EEPROM stores startup-configuration data
- Selectable output buffer voltage
- XIN terminal can use laboratory signal generator or OCXO/TCXO/XO components and board
- Laboratory power supply connectors
- USB-C power supply
- Serial port for configuration and register read out

Computer Requirements

- USB 2.0 or USB 3.0 Interface
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space: minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)

Evaluation Kit Contents

- RC32312A evaluation board
- Evaluation board manual
- Configuration software (Installable plugin for Renesas IC Toolbox)
- Configuration example file for four built-in device settings
- Board schematic and BOM

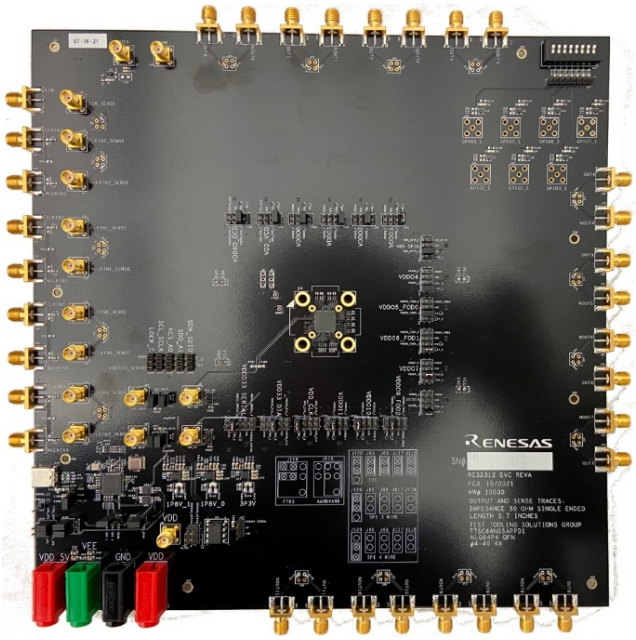


Figure 1. RC32312A Evaluation Board

Contents

Figures

1. Functional Description

The evaluation kit is used to demonstrate and evaluate the RC32312A, a fully integrated clock synthesizer/generator and clock jitter attenuator. The kit can evaluate major parameters including phase noise, spurious attenuation, clock frequency, output skew, phase alignment, device timing, and the signal waveform. The device on the board accepts any input frequency from 1kHz to 1GHz.

The RC32312A consists of a single APLL and DPLL design that allows for two separate frequency domains. The APLL can be used independently of the DPLL to generate synthesized clocks at the outputs that track the frequency of the input at the XIN pin. The DPLL can be used for jitter attenuation, clock filtering, and frequency translation while tracking clocks from the CLKIN pins. The DPLLs provide a programmable bandwidth and a DCO function for real-time frequency/phase adjustment.

1.1 Operational Characteristics

The board is equipped with on-board LDOs that require a 5V supply. If connecting to a high-speed USB interface, the evaluation board may be powered directly from the USB connection. The board is designed to operate over the industrial temperature range from -40 to 85°C, ambient temperature.

It is recommended to use proper grounding when operating the board to avoid ESD damage to the EVB.

1.2 Hardware Setup and Configuration

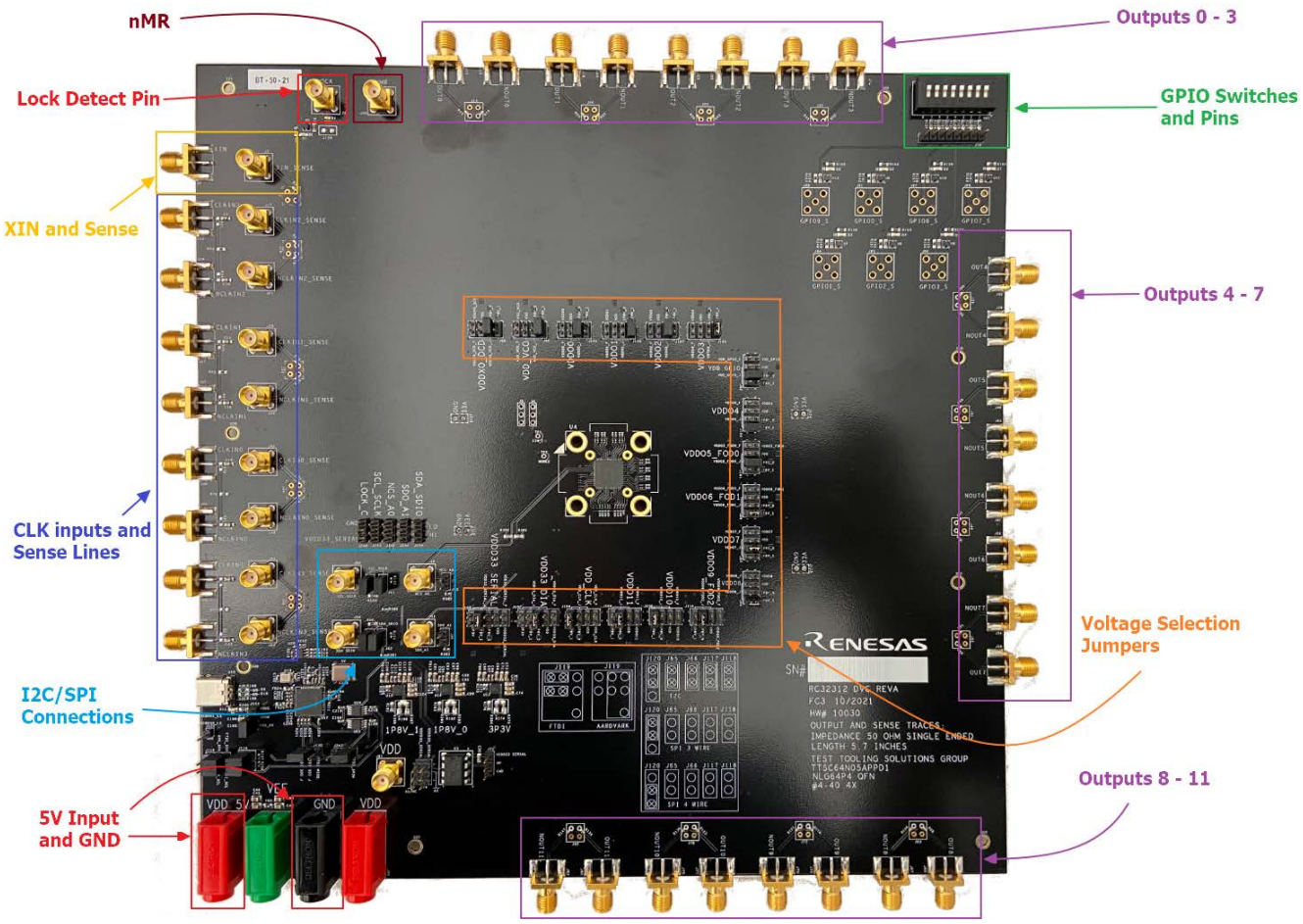


Figure 2. Evaluation Board Elements

Power Connection:

- Set the power supply voltage to 5V and the current limit to 2.5A
- +5V (J123) = +5V
- GND (J125) = GND

Expected Current Draw: ~ 0.58A

- After programming the device, depending on the configuration, ~0.6A to 1A during normal operation.

USB/I2C Connection

- Connect the USB port (U16) to PC through a USB cable

For proper functionality out of the box, the jumpers on the board should be placed to allow the correct voltages at each LDO and domain. The jumpers should be arranged as seen in Table 1.

Table 1. Default Jumper Configurations

Label/Function	Jumper	Default Orientation
Connect nCS_LS to IC from FTDI	J45	OFF
Connect MISO_LS to IC from FTDI	J46	OFF
Connect SCL_SCLK_LS to IC from FTDI	J61	ON
Connect SDA_SDIO_LS to IC from FTDI	J62	ON
I2C Pull-up to VDDD33_SERIAL	J65	ON
I2C Pull-up to VDDD33_SERIAL	J66	ON
EEPROM Write Protect	J71	OFF
EEPROM Address Select	J74	OFF
GPIO	J76	OFF
VDD_GPIO	J92	Either 1P8V_0 or 1P8V_1
VDDO8	J94	Either 1P8V_0 or 1P8V_1
VDD_VCO	J96	Either 1P8V_0 or 1P8V_1
VDDO7	J97	Either 1P8V_0 or 1P8V_1
VDD_XO_DCD	J98	Either 1P8V_0 or 1P8V_1
VDDO6_FOD1	J99	Either 1P8V_0 or 1P8V_1
VDDD33_SERIAL	J100	3P3V
VDDO5_FOD0	J101	Either 1P8V_0 or 1P8V_1
VDD33_DIA	J102	Either 1P8V_0 or 1P8V_1
VDDO4	J103	Either 1P8V_0 or 1P8V_1
VDD_CLK	J104	Either 1P8V_0 or 1P8V_1
VDDO3	J105	Either 1P8V_0 or 1P8V_1
VDDO11	J106	Either 1P8V_0 or 1P8V_1
VDDO2	J107	Either 1P8V_0 or 1P8V_1
VDDO10	J108	Either 1P8V_0 or 1P8V_1
VDDO1	J109	Either 1P8V_0 or 1P8V_1

Label/Function	Jumper	Default Orientation
VDDO9_FOD2	J110	Either 1P8V_0 or 1P8V_1
VDDO0	J111	Either 1P8V_0 or 1P8V_1
I2C Pull-up	J117	ON
I2C Pull-up	J118	ON
Bus Communication Selection	J119	Between FTDI_SDO and AVK_SDA and between FTDI_SCL and AVK_SCL
SDO and SDI Connection for I2C	J120	Between FTDI_SDO_J and FTDI_SDI_J
GND	J121	OFF
Enable I2C Pull-ups	J243	Between FTDI_3P3V and Center
SDA_SDIO	J244	OFF
SCL_SCLK	J245	OFF
SDO_A1	J246	OFF
NCS_A0	J247	OFF
LOCK_C	J248	OFF

1.3 GUI Setup and Configuration

1.3.1. Prepare the Software

1. Prior to execution of the GUI, the Renesas IC Toolbox (RICBox) software must be downloaded and installed. If Renesas IC Toolbox is already installed on this computer, then skip this step.
2. If Renesas IC Toolbox software is not yet installed, download and install the software from the webpage or install the one provided by Renesas support.
3. Double click the Renesas IC Toolbox software .exe file and install the one that corresponds to the version of Microsoft Windows currently being used.
   a. The filename with x64 corresponds to 64-bit Microsoft Windows.
   b. The filename with x86 corresponds to 32-bit Microsoft Windows.
4. Follow the on-screen instructions for Renesas IC Toolbox installation.
5. Download the RC32312A plugin file from the RC32312A webpage. This can also be provided from Renesas support.
6. Double click the RC32312A plugin .exe file and install the one that corresponds to the version of Windows currently being used.
7. Follow the on-screen instructions RC32312A plug-in installation.

1.3.2. Activating the GUI

After successfully installing the Renesas IC Toolbox (RICBox) software, activate the software from the Windows **Start** menu at the bottom left-corner of the screen.

1. Start > **RICBox**
2. Click Create new project

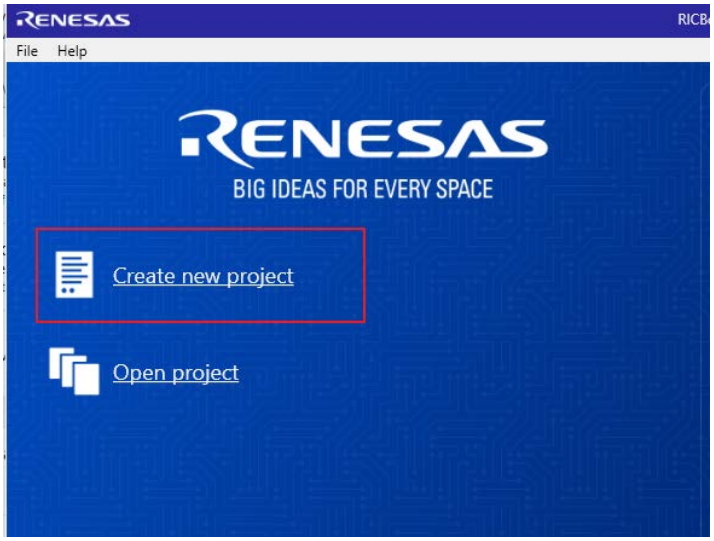


Figure 3. RICBox Create New Project Window

3. Use the "Select a Product Family" box to choose the FemtoClock3 devices.
4. Select the product variant being evaluated and click **OK**. In this example the RC32312A is used.

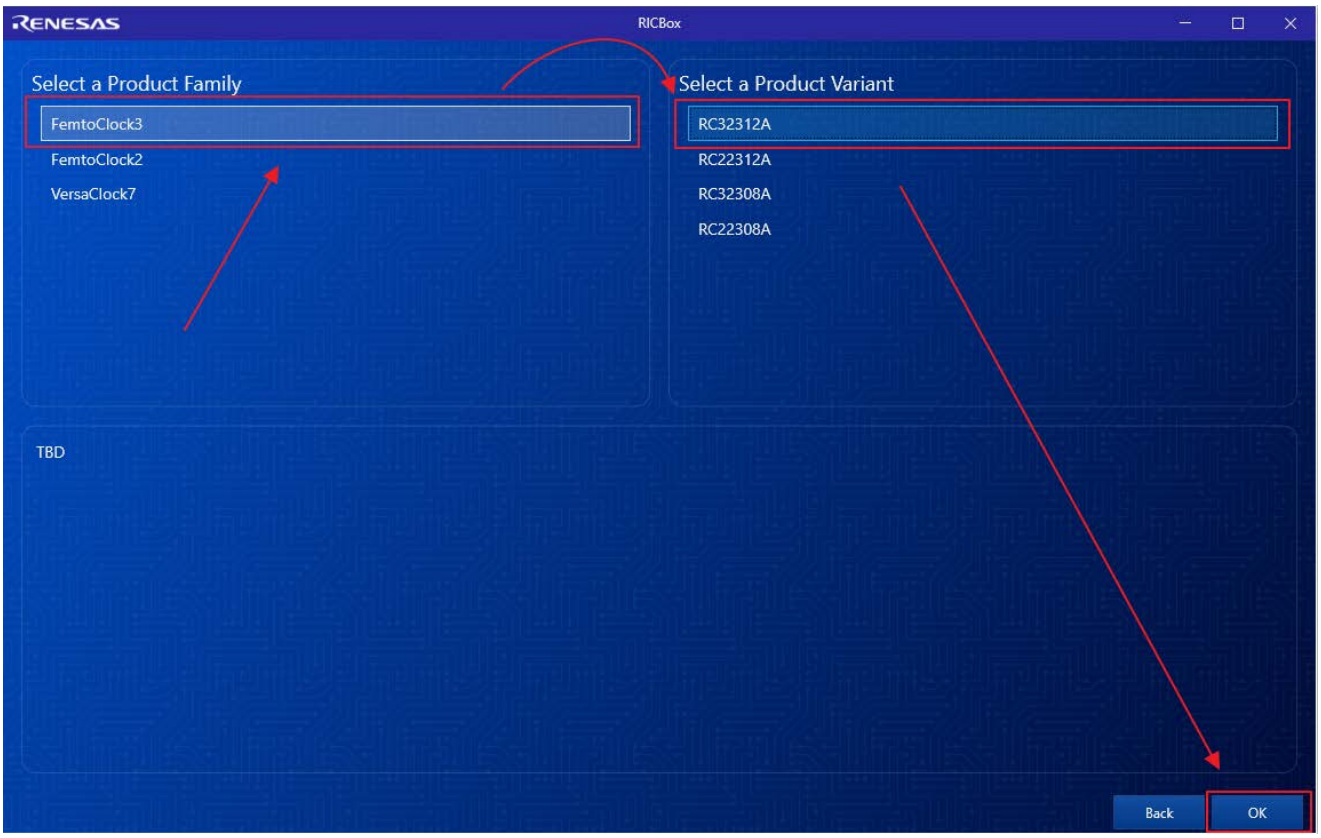


Figure 4. Product Family and Product Variant Window

5. Follow the on-screen wizard to setup the device for general evaluation starting from “Inputs”, then “DPLL”, and then “Outputs”.

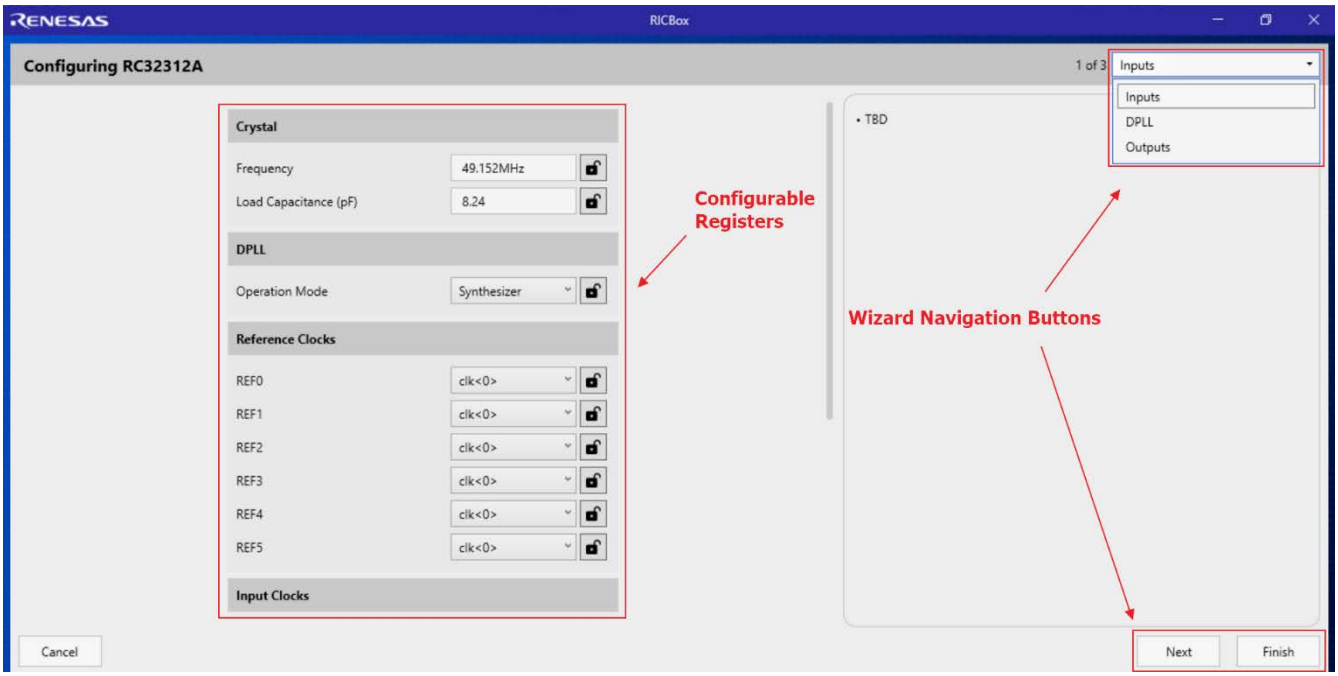


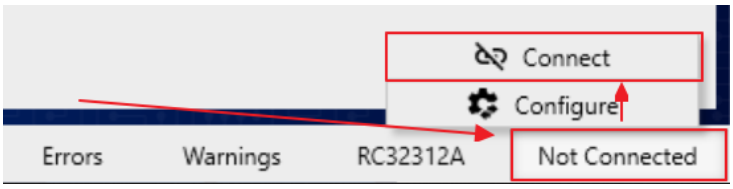
Figure 5. Configuration and Registers Window

6. After the settings are decided, click **Finish** to review the “Control Panel” page.
7. Use the side panel menu buttons to navigate through the GUI to all five separate pages.

Figure 6. Side Panel Menu Buttons

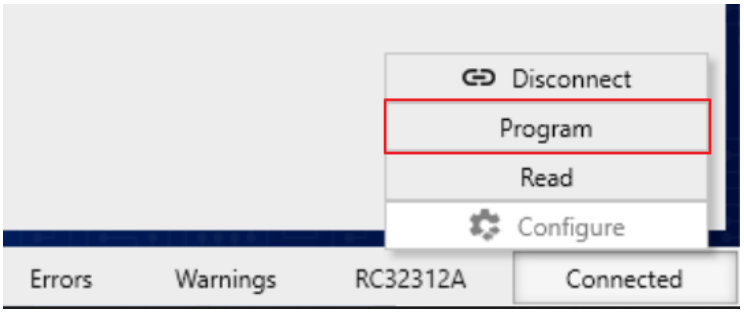
1.3.3. Configure the Evaluation Board

1. To establish communication between the EVB and the GUI, click the **Not Connected** button in the lower right corner. Then click **Connect**.



2. Once a connection is established to the EVB, the "Not Connected" button will change to say "Connected".

3. Click the **Program** button to write all the changed registers from the GUI to the on-board device. Any register changes after the “Program” button is clicked will occur in real-time and the device will update.



1.4 Hardware Modification Options

There are two options for providing an input signal to the device XIN (crystal oscillator input) pin:

- An external signal (J2 SMA connector) typically from a signal generator. This option is configured by default. See section 1.4.1.
- An on-board XTAL mount (U3). See section 1.4.2

The following sections describe how to configure the board for each option.

1.4.1. Overdrive the XIN with an External Signal

1. Populate C1 with 0.1µF capacitor to ensure that J2 has a connected path to the RC32312A device.
2. Depopulate C2 and C3 to ensure that excess trace is not used.
3. Place input clock signal at J2 and ensure that the signal is within specification for the XIN pin.

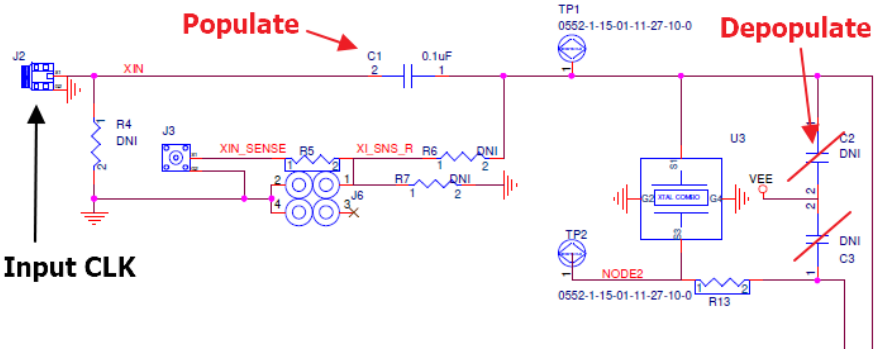


Figure 7. Overdrive the XIN with an External Signal Schematic

1.4.2. On-board XTAL Mount

1. Depopulate C1 to ensure there is no excess trace in the XIN pin.
2. Populate C2 and C3 to externally tune the input XTAL frequency.
3. Mount XTAL to U3 or use the through hole connectors on top of the EVB at TP1 and TP2.

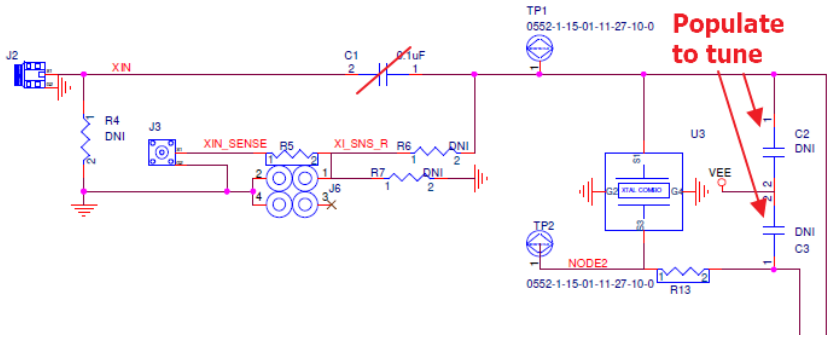


Figure 8. On-board XTAL Mount Schematic

2. Board Design

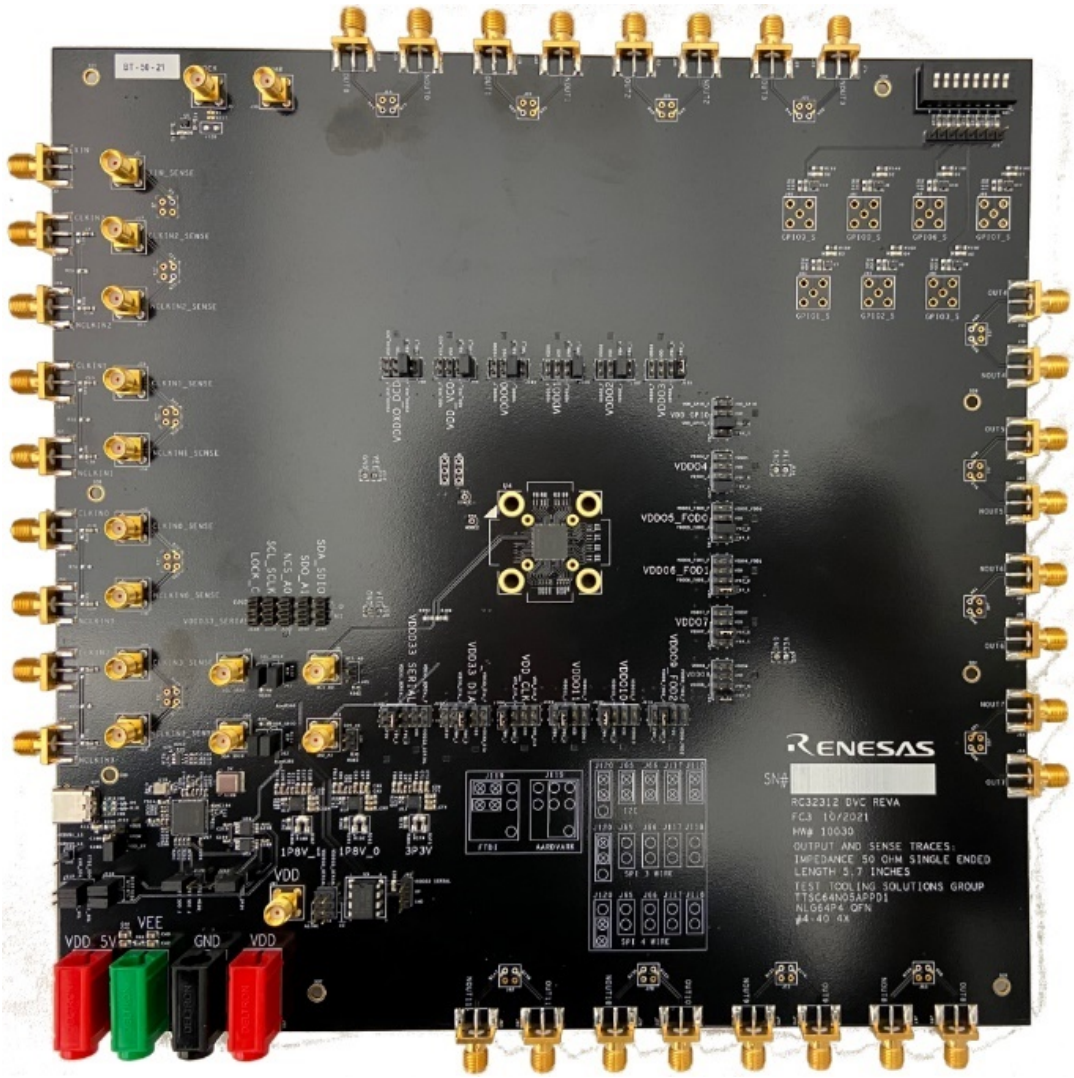


Figure 9. RC32312A Evaluation Board – Top View

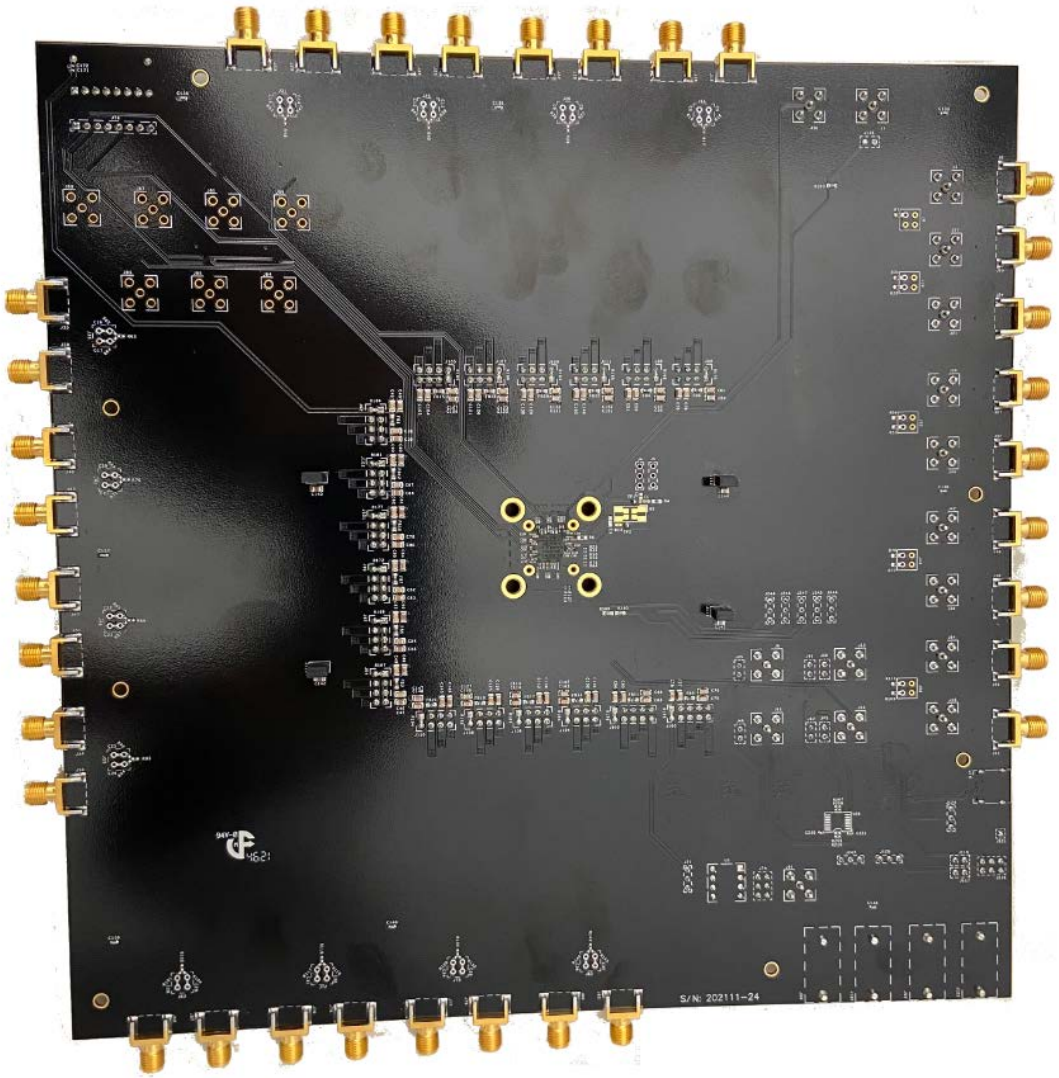


Figure 10. RC32312A Evaluation Board – Bottom View

2.1 Layout Guidelines

For more information, contact Renesas support.

2.2 Schematic Diagrams

The schematic diagrams are located at the end of this document.

2.3 Typical Phase Noise Plots

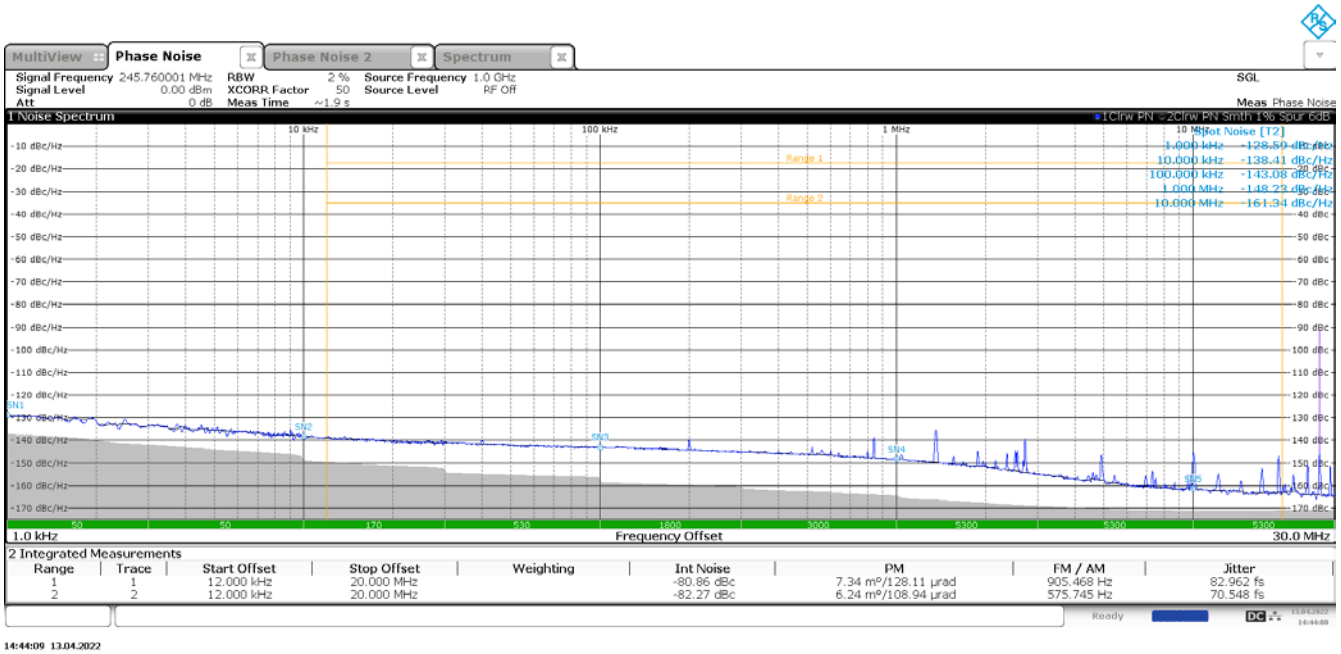


Figure 11. 245.76MHz Typical Phase Noise Synthesizer Mode

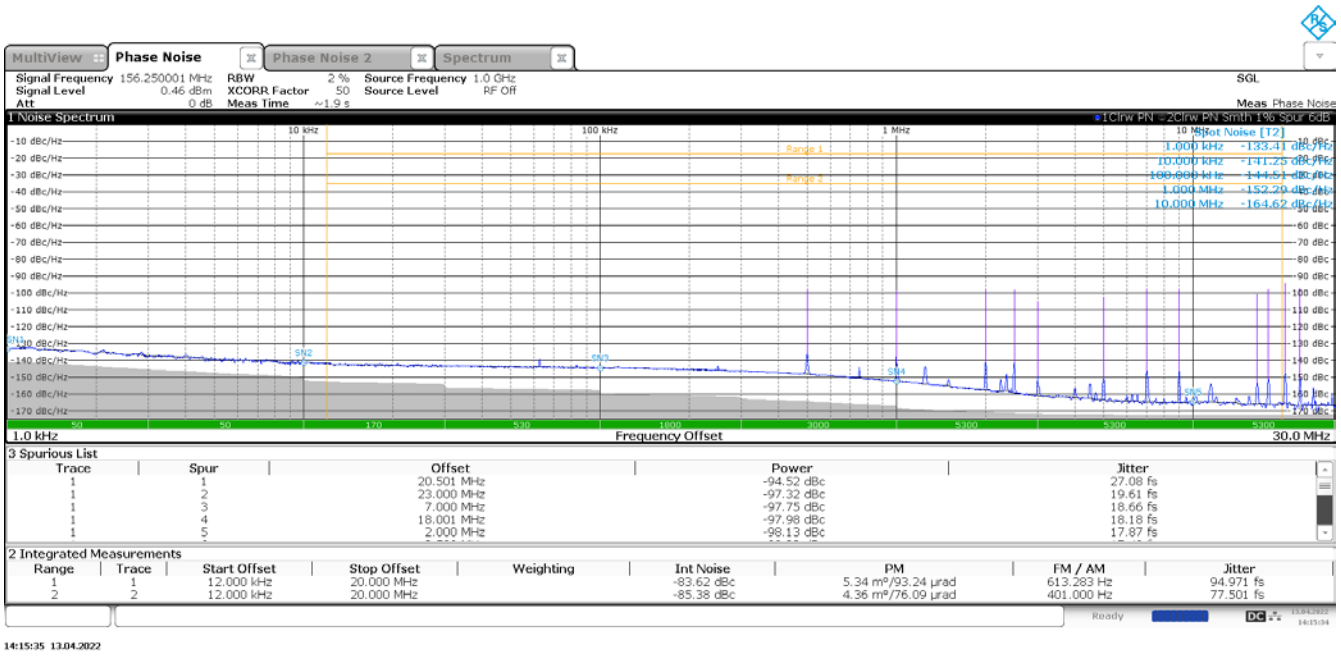


Figure 12. 156.25MHz Typical Phase Noise Synthesizer Mode

2.4 Bill of Materials

Table 2. Bill of Materials

Item	Qty	Reference	Part	Manufacturer Part Number
1	16	C1,C7,C10,C13,C18,C19,C24,C27,C30,C33,C71,C72,C96,C97,C117, C119	0.1µF	C0603C104K5R
2	39	C38,C41,C42,C45,C46,C49,C50,C53,C54,C57,C58,C61,C62,C65,C75, C78,C79,C82,C83,C86,C87,C90,C100,C103,C104,C107,C112,C114, C120,C123,C125,C128,C129,C132,C145,C148,C149,C152,C195	0.1µF	GRM21BR71E104K
3	43	C39,C40,C43,C44,C47,C48,C51,C52,C55,C56,C59,C60,C63,C64,C76, C77,C80,C81,C84,C85,C88,C89,C101,C102,C105,C106,C108,C113, C121,C122,C126,C127,C130,C131,C141,C142,C143,C144,C146,C147 ,C150,C151,C196	10µF	GRM21BC71E106K
4	6	C66,C68,C91,C93,C109,C115	10µF	GRM188D70J106MA73D
5	23	C67,C69,C92,C94,C110,C116,C189,C190,C193,C194,C198,C200,C20 2,C204,C206,C207,C208,C209,C210,C218,C219,C220,C221	0.1µF	GCM155R71E104KE02D
6	6	C70,C73,C95,C98,C111,C118	22µF	GRM188R60J226M
7	3	C74,C99,C124	1µF	GCM188R71E105KA64D
8	8	C133,C134,C135,C136,C137,C138,C139,C140	820pF	GRM1555C1E821J
9	2	J90,J123	Banana Red	571-0500
10	16	J92,J94,J96,J97,J98,J99,J101,J103,J104,J105,J106,J107,J108,J109, J110,J111	Headerstrip 2X4	10-89-7080
11	1	J93	Banana Green	571-0400
12	2	J100,J102	Headerstrip 2X5	10-89-7100
13	1	J121	Headerstrip 1X1	68000-401HLF
14	1	J125	Banana Black	571-0100
15	10	R2,R99,R100,R141,R149,R152,R155,R158,R161,R164	4.70k	CRCW06034K70FK
16	9	R3,R144,R150,R153,R156,R159,R162,R165,R200	1.50k	CRCW06031K50FK
17	24	R14,R20,R22,R32,R37,R42,R44,R54,R61,R65,R67,R73,R80,R89,R90, R96,R97,R108,R115,R120,R125,R135,R138,R146	0.00	ERJ-1GN0R00
18	7	R126,R127,R129,R131,R133,R134,R137	1.00k	CRCW06031K00FKTA
19	7	R171,R178,R186,R211,R212,R213,R214	10.0k	RC0402JR-0710KL
20	3	R174,R182,R188	25k	3214W-1-253E
21	3	R176,R183,R191	0.00	CRCW06030000Z0
22	2	R196,R197	4.70k	RC0402JR-074K7L
23	2	R198,R199	5.10k	CRCW04025K10FK
24	4	R201,R202,R203,R204	10.0	RC0402FR-0710RL
25	1	R215	12.0k	CRCW040212K0FK
26	1	R216	2.00k	CRCW04022K00FKED
27	5	R375,R385,R386,R387,R388	20.0k	CPF-A-0603B20KE
28	4	R380,R381,R382,R383	0.00	ERJ-2GE0R00

Item	Qty	Reference	Part	Manufacturer Part Number
29	1	R384	7.50k	CRCW06037K50FK
30	5	R389,R390,R391,R392,R393	10.0k	RC0603JR-0710KL
31	8	SO1,SO2,SO3,SO4,SO5,SO6,SO7,SO8	Standoff 25mm	25506
32	1	SW1	Slide 3Pos	KAT1108E
33	2	TP1,TP2	0552-1-15-01-11-27-10-0	0552-1-15-01-11-27-10-0
34	8	U1,U6,U7,U8,U9,U10,U11,U12	BSS138W	BSS138W
35	1	U5	AT24C04C	AT24C04C-PUM
36	3	U13,U14,U15	RAA214020	RAA214020
37	1	U16	USB Type C	12401598E4#2A
38	1	U17	FT232HQ	FT232HQ-REEL
39	1	U19	ABM8W-12.0000MHZ-6-B1U-T3	ABM8W-12.0000MHZ-6-B1U-T3
40	1	U20	93LC56BT-I/OT	93LC56BT-I/OT
41	2	U24,U25	PCA9517	PCA9517
42	1	U26	LSF0204	LSF0204PWR

3. Ordering Information

Part Number	Description
RC32312A-EVK	RC32312A Evaluation Board

4. Revision History

Revision	Date	Description
1.00	Apr 19, 2022	Initial release.

CONFIGURATION LATCHING

Renesas	1140 West Warner Rd. Tempe, AZ 85284
Title:	FC3_DVC_QFN64_REVA
Size: D	HW Number: HW10032
Engineer:	Andy
Date:	11/02/2021
Sheet:	3 of 5
Rev.	A

VDD_VCO	160mA
VDDXO_DCD	80mA
VDDD33_SERIAL	10mA
VDDD33_DIA	220mA
VDD_CLK	60mA
VDDO11	40mA
VDDO10	40mA
VDDO9_FOD2	110mA
VDDO8	40mA
VDDO7	40mA
VDDO6_FOD1	110mA
VDDO5_FOD0	110mA
VDDO4	40mA
VDDO3	40mA
VDDO2	40mA
VDDO1	40mA
VDDO0	40mA

if using POT, replace with 8.2K, remove 20k and 7.5k

if using POT, replace with 8.2K, remove 20k

if using POT, replace with 8.2K, remove 20k

Place these 10 uF caps near J112, J113, J114, J115, on the bottom of board

Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: FC3_DVC_QFN64_REVA

Size	HW Number:	Engineer:	Rev.
C	HW10032	Andy	A
	Date: 10/27/2021	Sheet: 4 of 5	

If Aardvark is being used, plug in the USB-C cable. FTDI_3P3V comes from FT232.

SPI only for FTDI.

If using bypass path, then ground EN pin.

FTDI AARDVARK

I2C

SPI 3 Wire

SPI 4 Wire

Turn 5V into a power plane

Turn FTDI_3P3V into a power plane

Place 0.1uF close to pin 40

Place 0.1uF close to pin 39

Place 0.1uF close to pin 3

Place 0.1uF close to pin 8

Place close to pin 37, 38

Place close to pin 12, 24, 46

Renesas 1140 West Warner Rd. Tempe, AZ 85284			
Title: FC3_DVC_QFN64_REVA			
Size: B	HW Number: HW10032	Engineer: Andy	Rev.: A
	Date: 11/10/2021	Sheet: 5 of 5	

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.