## Introduction

The evaluation board is designed to help the customer evaluate the 5P35023 device, the latest addition to the family of programmable devices in IDT's Timing portfolio. When the board is connected to a PC running IDT Timing Commander™ software through a USB, the device can be configured and programmed to generate different combinations of frequencies.

## Board Overview

Use Figure 1 and Table 1 to identify: USB connector and the input and output frequency SMA connectors.

Figure 1. EVK5P35023 Evaluation Board

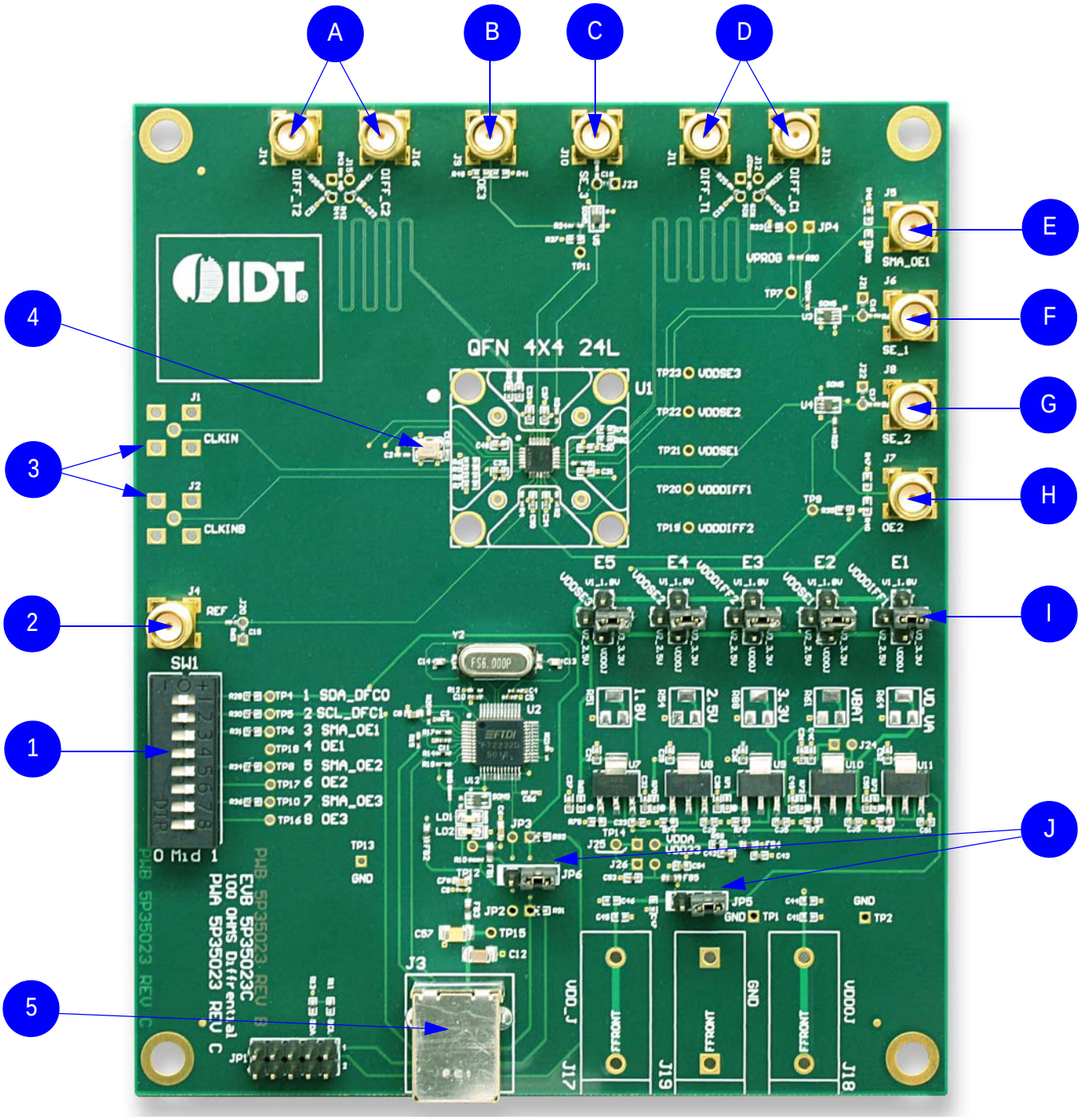


Table 1. Evaluation Board Labels and Functions

| Label Number | Name | On-board Connector Label | Function |
|---|---|---|---|
| 1 | DIP Switch | SW1 | This is used to set outputs enable/disable on the IC and switches DFC in different configurations. |
| 2 | Reference Output | REF | This is the reference or buffered output from the crystal. |
| 3 | Differential Clock Input | CLKIN/CLKINB | A differential clock can be connected as source for the device. |
| | Single-ended Clock Input | CLKINB | A Single-ended clock can be connected as source for the device using CLKINB only. |
| 4 | Crystal, 25MHz | | This crystal is used as a reference source for the clock signal. |
| 5 | USB Connector | J3 | Connect this USB to your PC to run IDT Timing Commander. |
| A | Differential Output #2 | DIFF_T2/C2 | This can be a differential pair, or two single-ended outputs. By default, it's an LPHCSL differential output. |
| B | Output-enable Connector | OE3 | This port can be used in Pro-active Power Saving (PPS) mode. |
| C | Single-ended Output | SE_3 | This is the single-ended output. By default it's an LVCMOS single-ended output. |
| D | Differential Output #1 | DIFF_T1/C1 | This can be a differential pair, or two single-ended outputs. By default, it's LPHCSL differential output. |
| E | Output-enable Connector | SMA_OE1 | This port can be used in Pro-active Power Saving (PPS) mode. |
| F | Single-ended Output | SE_1 | This is the single-ended output. By default it's an LVCMOS single-ended output. |
| G | Single-ended Output | SE_2 | This is the single-ended output. By default it's an LVCMOS single-ended output. |
| H | Output enable Connector | OE2 | This port can be used in Pro-active Power Saving (PPS) mode. |
| I | Output Voltage Selector | E1, E2, E3, E4, E5 | This is a four-way header used to select an output voltage. Connect center pin to GND, and then the respective voltage (3.3V as default). |
| J | Input Selector | JP5, JP6 | This is used to configure input from USB or external power supply. |

# Board Power Supply

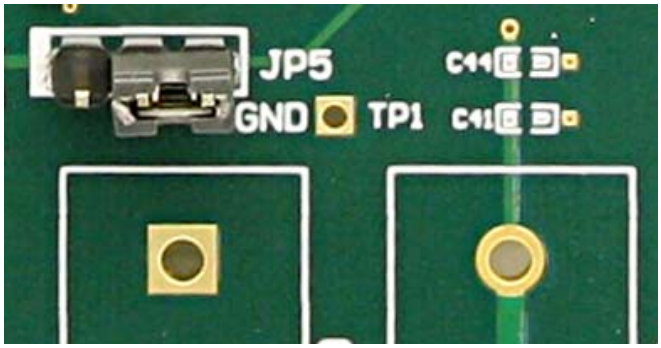
## Power Supply Options

The core voltage includes a digital voltage $V_{DD33}$ and an analog voltage $V_{DDA}$. Both core voltages can be powered by USB as default.

- USB Power Supply only – When the board is connected to a PC through a USB cable, on-board voltage regulators will generate a 3.3V for the device. In this case, place the jumper as shown in Figure 2. See the JP5 jumper position for the on-board voltage regulators in the following figure. USB power source is recommended because it's readily available right from your laptop.

Figure 2. JP5 Jumper Position (pins 1 & 2) for the On-Board Voltage Regulators

Jumping to the pin configuration as shown will select the power source from on-board voltage regulators powered by USB.



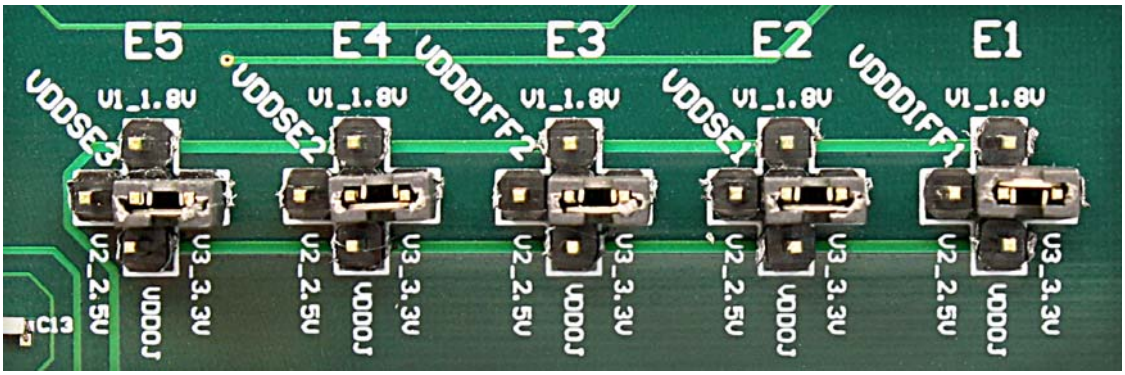

## Output Clock Voltages

Like $V_{DDA}$ and $V_{DD33}$ having two sources, each output voltage is also provided with two sources to choose from: bench power supply or powered from USB. The selection is made by a 4-way header as shown in Figure 3 below.

The jumper can be used to select a voltage for E1, E2, E3, E4, and E5 respectively. The on-board voltage regulators powered by USB are 1.8V, 2.5V and 3.3V; $V_{DDOJ}$ is from bench power supply connecting to JP17 and JP18

Note: Each output voltage can be individually selected. Use the label on the evaluation board: E1 for $V_{DDDIFF1}$, E2 for $V_{DDSE1}$, E3 for $V_{DDDIFF2}$, E4 for $V_{DDSE2}$ and E5 for $V_{DDSE3}$.

Figure 3. Jumper Configuration for On-board Voltage Regulators

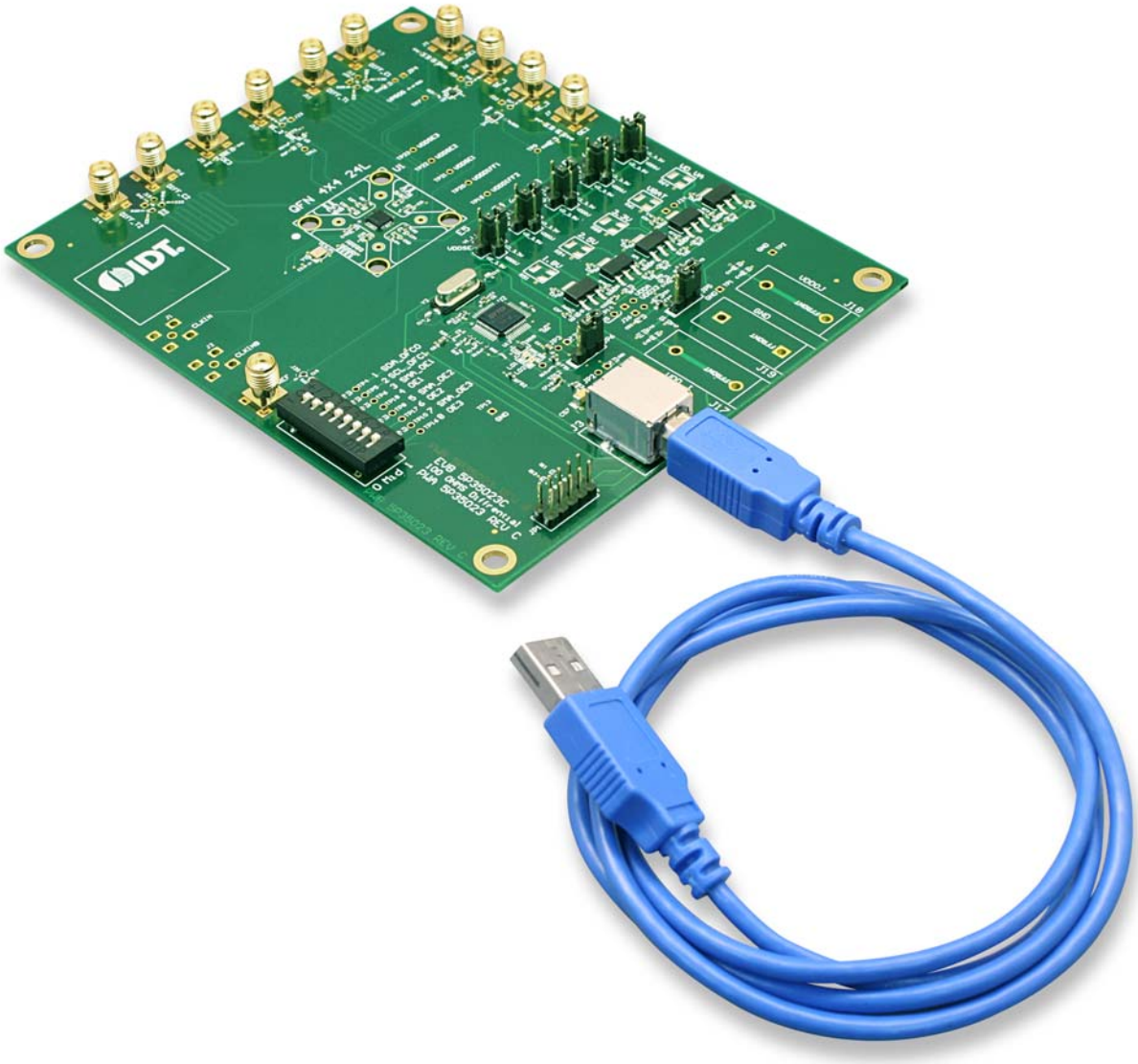



# Connecting the Board

The board is connected to a PC through a USB connector for configuring and programming the device, as shown in Figure 4 below. The USB interface will also provide +5V power supply to the board, from which on-board voltage regulators generate various voltages for the core as well as for each output.

Note: The USB port only supports USB 2.0; USB 3.0 is not supported at this time.

Figure 4. Connecting the Board with USB Port for Communications with Timing Commander Software



## On-board Crystal

A 25MHz crystal is installed on the board and is used as a source for reference frequency.

## Board Default Frequency Output

Table 2. Board Default Frequency Output

| Serial | Output | Output Frequency |
|---|---|---|
| 1 | SE_1 (Single-ended) | — |
| 2 | SE_2 (Single-ended) | 48MHz |
| 3 | SE_3 (Single-ended) | 60MHz |
| 4 | REF (Single-ended: Reference output) | 25MHz |
| 5 | DIFF_T1/C1 (Differential output) | 100MHz |
| 6 | DIFF_T2/C2 (Differential output) | 100MHz |

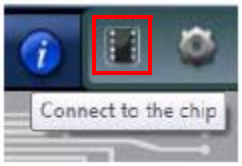
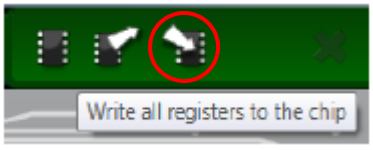
## DIP Switch (SW1)

Table 3. DIP Switch (SW1)

| Serial | DIP Switch Pin Number | DIP Switch Pin Name | State | Mode |
|---|---|---|---|---|
| A | 1 | SDA_DFCO | Floating/Tri-state | — |
| B | 2 | SCL_DFC1 | Floating/Tri-state | Software $I^2C$ |
| C | 3, 5, 7 | SMA_OE1, SMA_OE2, SMA_OE3 | High or 1 | — |
| D | 4, 6, 8 | OE1, OE2, OE3 | High or 1 | — |

## Configuration and Setup from $I^2C$ Port

Table 4. Configuration and Setup from I2C Port

| Step Number | Step Description | Comments |
|---|---|---|
| 1 | Set SCL_OFC1 Pin (DIP switch pin 2). | High or 1. The default setting from the board is pull-high internally. |
| 2 | Launch 5P35023 Timing Commander software. | Refer to 5P35023 Timing Commander User Guide, Timing Commander software. |
| 3 | Follow the “Getting Started Steps” in Timing Commander software. | An $I^2C$ connection is established between GUI software and VersaClock 3S device. |
| 4 | Using the Timing Commander GUI, start a new settings file, or open a pre-optimized file. | Configure the Timing Commander software for the required sets of outputs. |
| 5 | Connect J3 to a USB Port using the supplied $I^2C$ cable. | An $I^2C$ connection is established between GUI software and VersaClock 3S chip. |
| 6 | Connect to the EVB by clicking on the microchip icon located at the right of the Timing Commander. |  |
| 7 | Once configured, new options will be available on a green background indicating that the EVB has successfully connected with the board. |  |
| 8 | Write the setting to the device by clicking on the write all registers to the chip option. |  |
| 9 | All intended outputs should be available for measurement. | — |

# Evaluation Board Schematics

Evaluation board schematics are shown on the following pages.

Figure 5. Evaluation Board Schematic (1)

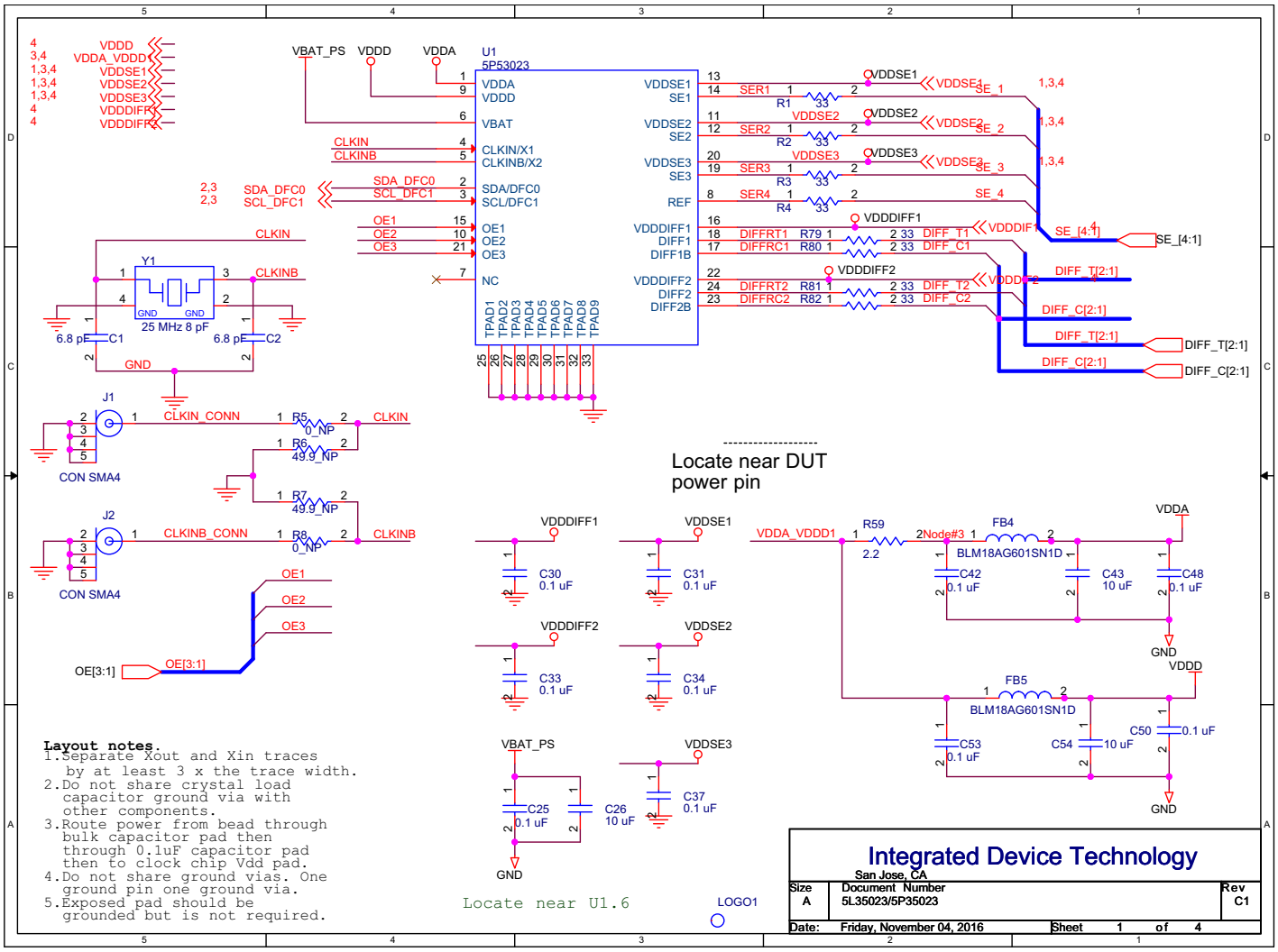


Figure 6. Evaluation Board Schematic (2)

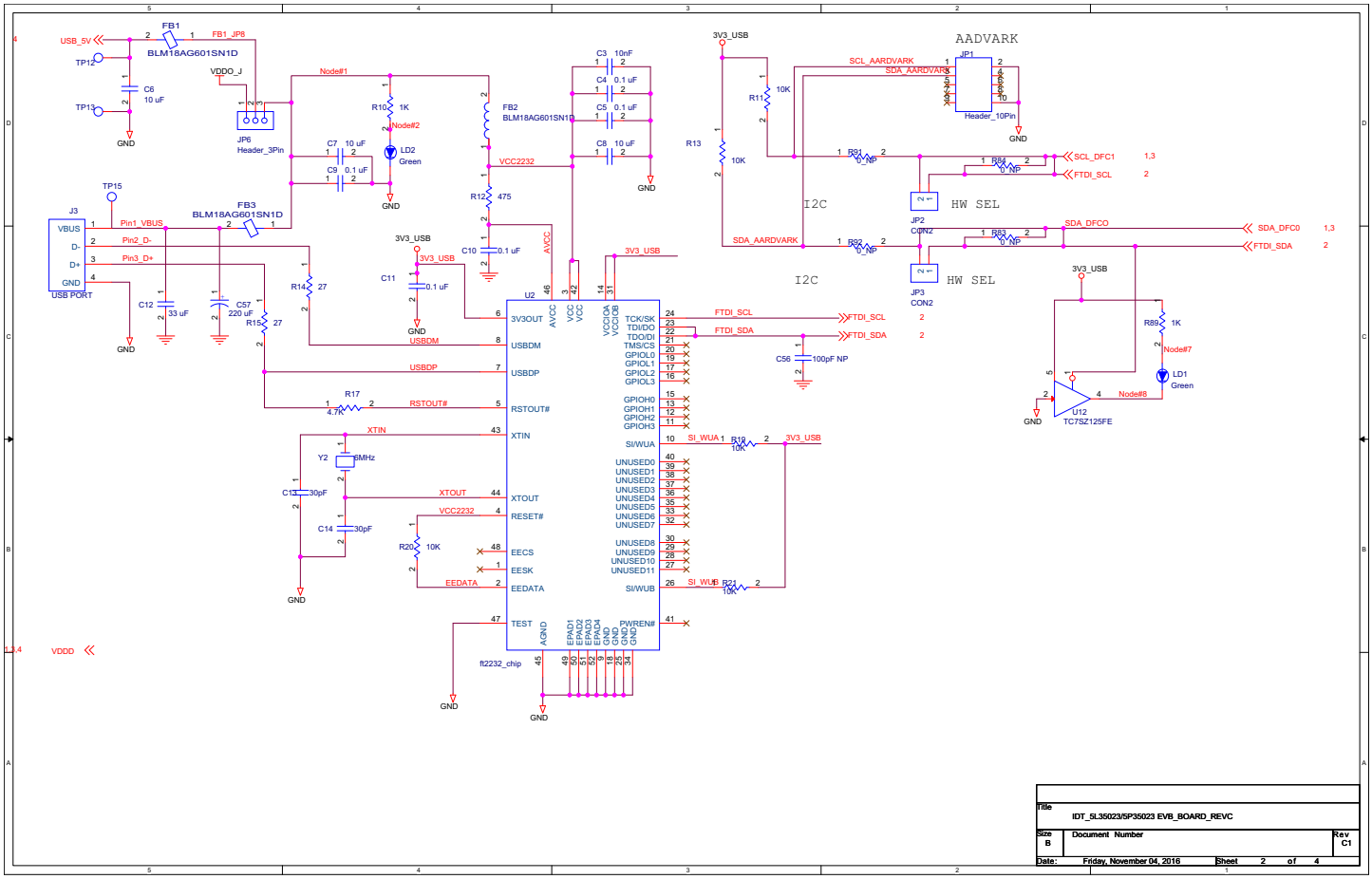


Figure 7. Evaluation Board Schematic (3)

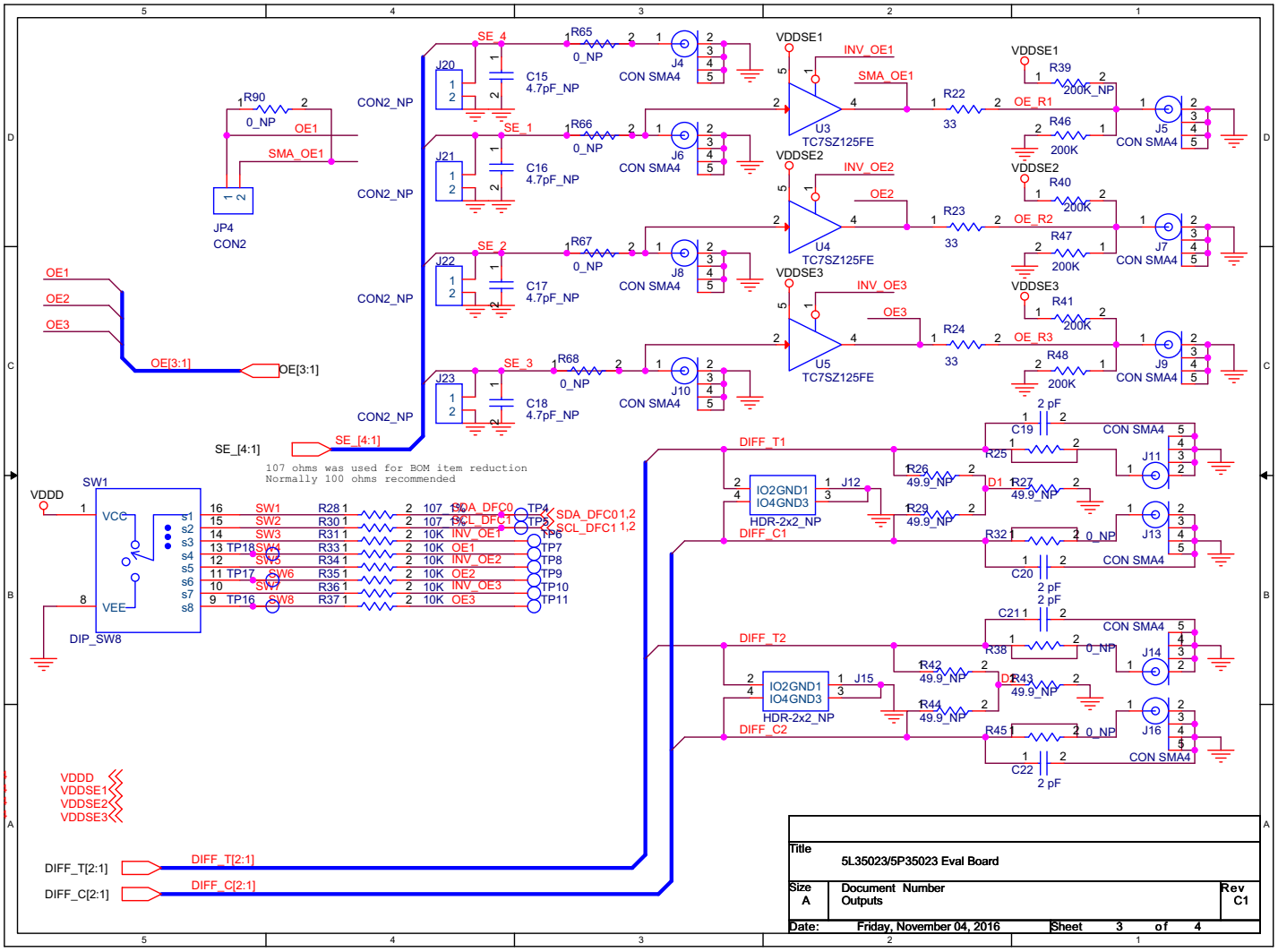
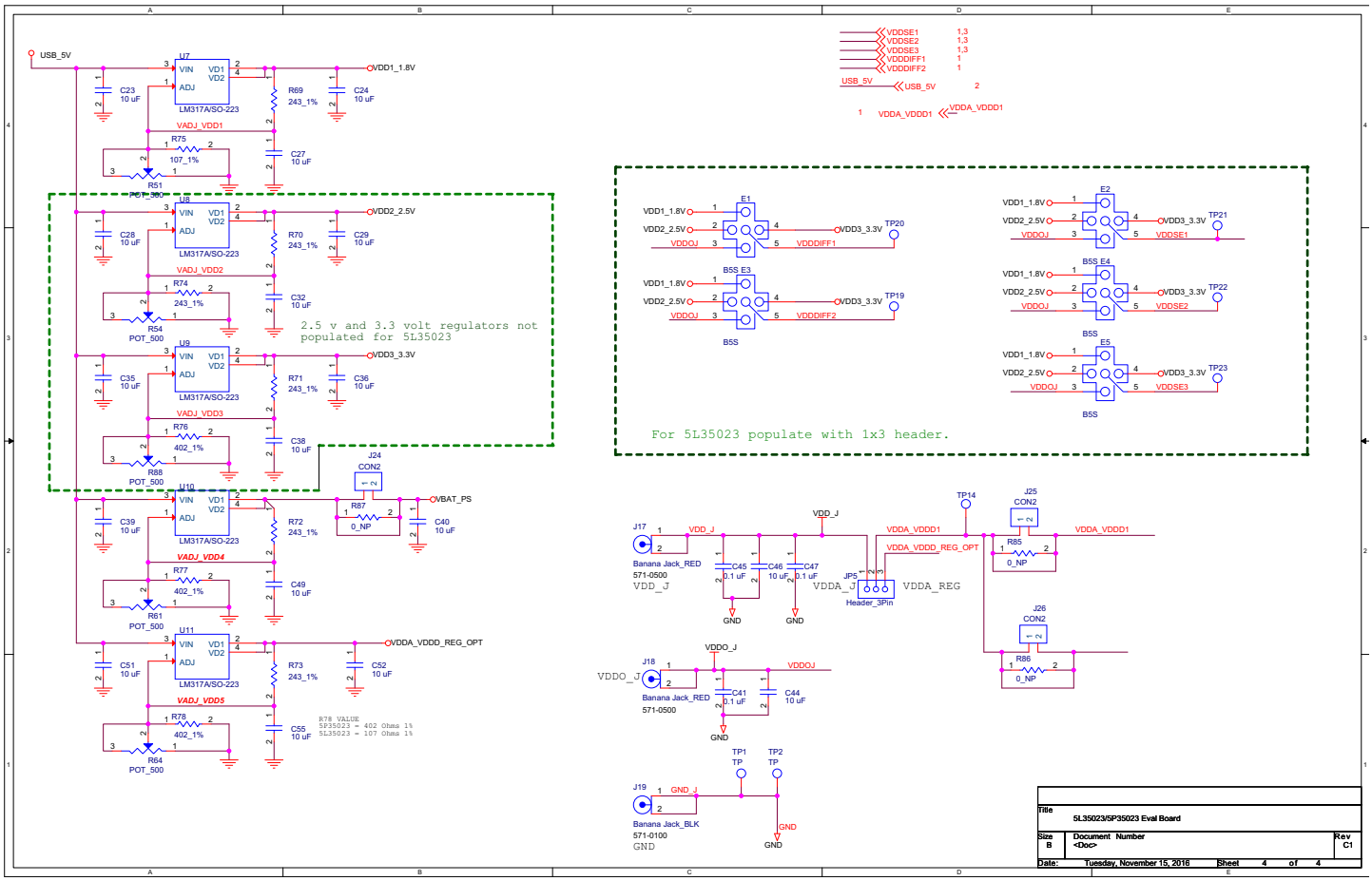


Figure 8. Evaluation Board Schematic (4)

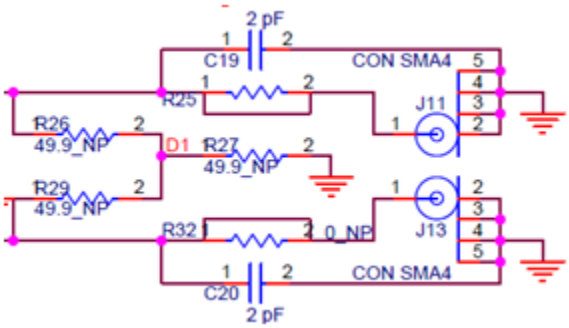


# Signal Termination Options

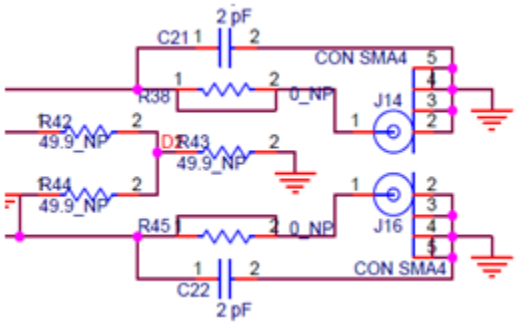
Termination options for differential output 1–2 in the evaluation board are displayed in Figure 9. The termination circuits are designed to optionally terminate the output clocks in LVPECL, LVDS, LVCMOS and HCSL signal types by populating (or not-populating) some resistors. DC or AC coupling of these outputs are also supported.

Table 5 and Table 6 tabulates component installations to support LVPECL, LPHCSL, LVCMOS and LVDS signal types for output 1–2, respectively. Note that by doing so, the output signals will be measured and terminated by an oscilloscope with a 50Ω internal termination.

Figure 9. Output Termination Options




DIFF_T1/C1




DIFF_T2/C2

Table 5. Termination Options for Differential Output 1 (DIFF_T1/C1)

| Signal Type | Series Resistors: R79, R80 | Series Capacitors: C19, C20 | Resistor Network | | |
|---|---|---|---|---|---|
| | | | R26, R29 | R27 | R25, R32 |
| **LPHCSL | 33Ω | 2pF | Not installed | Not installed | Not installed |

Table 6. Termination Options for Differential Output 2 (DIFF_T2/C2)

| Signal Type | Series Resistors: R81, R82 | Series Capacitors: C21, C22 | Resistor Network | | |
|---|---|---|---|---|---|
| | | | R42, R44 | R43 | R38, R45 |
| **LPHCSL | 33Ω | 2pF | Not installed | Not installed | Not installed |

As noted, 4-resistor network is not installed in Table 5 and Table 6 because oscilloscope with internal 50Ω termination is utilized for signal termination and measurement. If an AC-coupled, stand-alone LVPECL output is needed (without oscilloscope connections), the 4-resistor network needs to be installed accordingly.

Table 7. Termination for Single-ended Output 1 (SE_1)

| Signal Type | Series Resistors: R1 | Series Capacitors: C16 |
|---|---|---|
| *LVCMOS | 33Ω | Not installed |

Table 8. Termination for Single-ended Output 2 (SE_2)

| Signal Type | Series Resistor: R2 | Series Capacitors: C17 |
|---|---|---|
| *LVCMOS | 33Ω | Not installed |

Table 9. Termination for Single-ended Output 3 (SE_3)

| Signal Type | Series Resistor: R3 | Series Capacitors: C18 |
|---|---|---|
| *LVCMOS | 33Ω | Not installed |

Table 10. Termination for Single-ended REF Output (REF)

| Signal Type | Series Resistor: R4 | Series Capacitors: C15 |
|---|---|---|
| *LVCMOS | 33Ω | Not installed |

Table 11. Termination for Differential and Single-ended Clock Input (CLKIN\CLKINB)

| Signal Type | Series Resistor: R8 | Series Resistor: R15 |
|---|---|---|
| Differential Clock Input | Not installed | Not installed |
| Single-ended Clock Input | Not installed | Not installed |

Note: **The differential output is applicable to LPHCSL which is the default configuration of the board.
*The single-ended output is applicable to LVCMOS which is the default configuration of the board.
Contact IDT if user wants to change termination configuration to support other output signal types.

# Ordering Information

Table 12. Orderable Part Number

| Part Number | Description |
|---|---|
| EVK5P35023 | Evaluation board with all differential outputs terminated as LPHCSL; single-ended terminated as LVCMOS. |

# Revision History

Table 13. Revision History

| Revision Date | Description of Change |
|---|---|
| June 8, 2017 | ▪ Updated user manual to new format.<br>▪ Updated all images and made several textual changes throughout.<br>▪ Updated Evaluation Board Schematics drawings. |
| May 27, 2016 | Initial release. |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.