

ISL73006SLHEV1Z

The ISL73006SLHEV1Z evaluation board (Figure 3) features the ISL73006SLH buck regulator. This IC is a small foot print radiation hardened POL designed for critical low power applications.

The ISL73006SLH is operational over 3V to 18V integrating both high-side and low-side power FETs and switches at a native 500kHz frequency. The ISL73006SLH uses constant-frequency peak current mode control architecture for fast loop transient response. The ISL73006SLH can use either its internal compensation or an external Type II compensation to stabilize the loop as determined by specific design and performance requirements.

By integrating both P-channel and N-channel power devices and with the option of internal compensation, a minimum of external components are required, thereby reducing the BOM count and complexity of the design.

The ISL73006SLHEV1Z evaluation board and this accompanying manual provide a quick and easy method to evaluate the ISL73006SLH part in both an internal or an external compensation configuration.

See the *ISL73006SLH datasheet* for information about the operation, function, and performance of the device.

**Features**

- Optimized for 12V to 3.3V conversion
- Jumper configurable to either the internal or external slope and compensation configuration
- 1A output current
- On board transient generator

**Specifications**

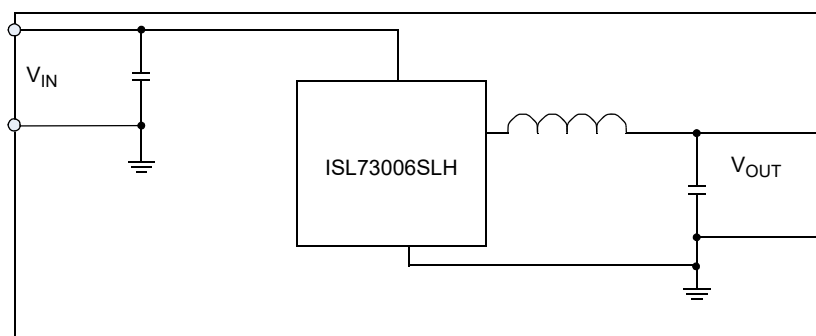
The ISL73006SLHEV1Z evaluation board is configurable by jumpers for either external or internal configuration of compensation or slope.

The board allows for other conditions to be evaluated with user-modification of components and connections.

The electrical ratings of the ISL73006SLHEV1Z evaluation board are shown in Table 1.

**Table 1. Electrical Ratings**

Parameter	Rating
PVIN Supply Voltage	6V - 18V
DC Output Voltage	3.3V
Operating Frequency	500kHz
Output Current	1A
Temperature	-55°C to +125°C



**Figure 1. Block Diagram**

## Contents

<b>1. Functional Description</b>	<b>3</b>
1.1 Operational Characteristics	3
1.2 Setup and Configuration	3
<b>2. Board Design</b>	<b>4</b>
2.1 Basic Layout	5
2.2 Layout Guidelines	5
2.3 Schematic Diagrams	5
2.4 Bill of Materials	6
2.5 Board Layout	7
<b>3. Typical Performance Graphs</b>	<b>8</b>
<b>4. Ordering Information</b>	<b>10</b>
<b>5. Revision History</b>	<b>10</b>

# 1. Functional Description

The ISL73006SLHEV1Z evaluation board is configured by default for 12V to 3.3V conversion with a 1A maximum output current and contains the ISL73006SLH voltage regulator IC. Any external configurations for control loop and slope compensations can be chosen by jumpers JP5 and JP3, respectively. [Figure 1](#) shows the ISL73006SLHEV1Z evaluation board block diagram. [Figure 3](#) shows the ISL73006SLHEV1Z board image.

The ISL73006SLHEV1Z evaluation board provides test point access to critical pins of the IC device and convenient pads for connecting test equipment. For more information, see the schematic ([Figure 5](#)), PCB layers ([Figure 7](#) through [Figure 12](#)), and [Bill of Materials](#). [Figure 13](#) through [Figure 22](#) show the performance data using the ISL73006SLHEV1Z and basic lab equipment.

## 1.1 Operational Characteristics

The ISL73006SLHEV1Z only requires a single voltage supply > 6V connected to the PVIN pad to operate, outputting 3.3V on the VOUT pad with a 1A output current capability. Configured for a nominal PVIN voltage of 12V, the input operating voltage at which the IC turns on is set by the resistor divider ( $R_1$  and  $R_2$ ) on the ENABLE pin.

*Note:* Do not exceed 5V on the ENABLE pin.

## 1.2 Setup and Configuration

The following equipment is recommended for testing the board:

- 12V power supply
- 100MHz oscilloscope

Complete the following steps to configure and use the board:

1. Configure the board as shown in [Figure 2](#).
2. Connect and turn on a 12V power supply to the PVIN pad.
3. Use the oscilloscope to look at VIN and VOUT waveforms and observe the behavior of the LX phase node located on pin 10 of the IC package. Proper probe grounding must be practiced when observing clean waveforms.
4. Output current loading can be externally added at the VOUT and GND pads for loaded output evaluations. A DVM(s) can monitor the input and output voltages and currents.

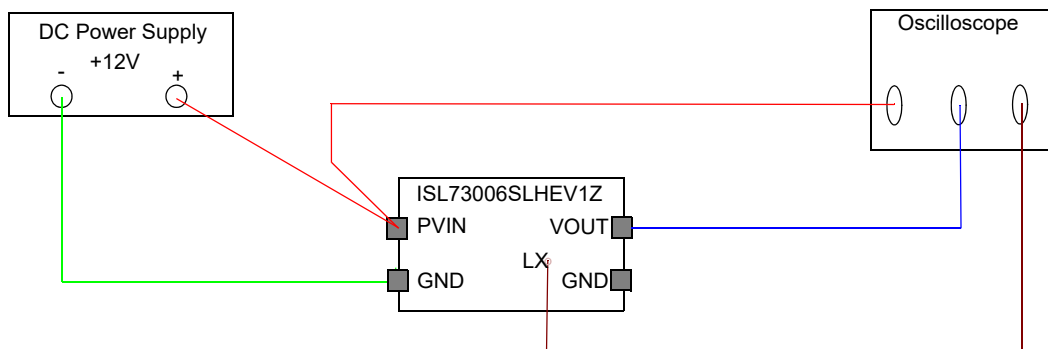


Figure 2. ISL73006SLH Basic Evaluation Test Setup Block Diagram

## 2. Board Design

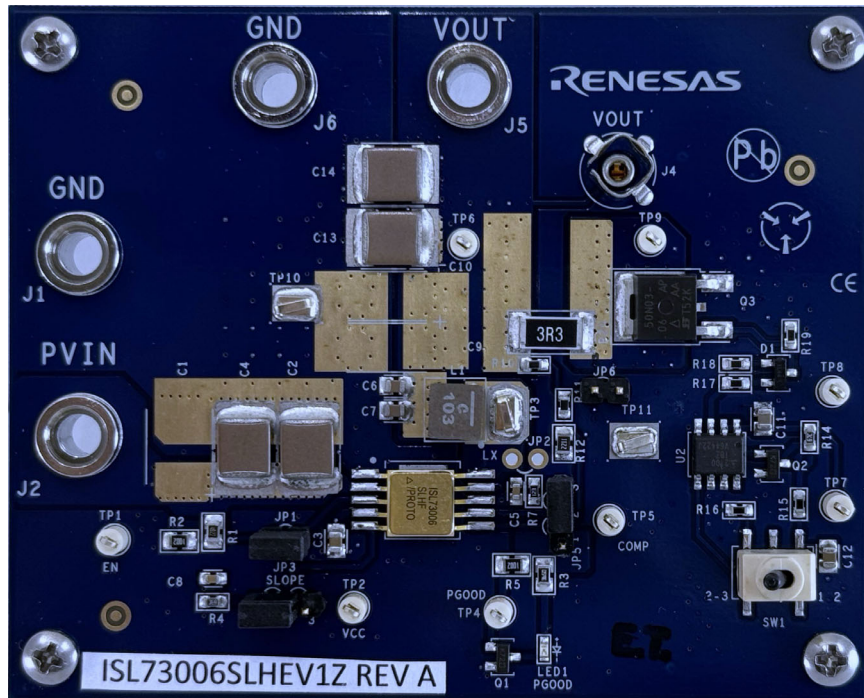


Figure 3. Evaluation Board (Top)

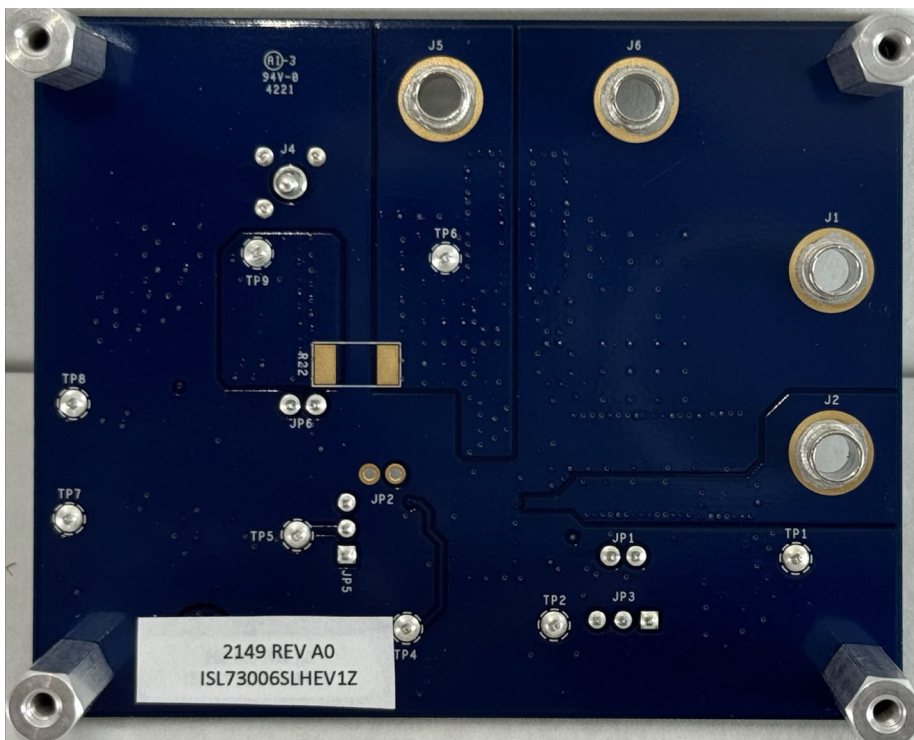


Figure 4. Evaluation Board (Bottom)

## 2.1 Basic Layout

The ISL73006SLH is located in the lower center of the board and is labeled U1. Connect the input power across the PVIN and GND jacks. The output voltage appears across the VOUT and GND jacks.  $C_{IN}$  is provided by  $C_2$  and  $C_4$ . The output LC filter is comprised of the  $L_{OUT}$ ,  $L_1$ , and  $C_{OUT}$  is provided by  $C_{13}$  and  $C_{14}$ . JP1 sets the EN threshold to enable the IC when PVIN is ~6V; otherwise, ENABLE can be accessed by TP1. The transient generator circuit is towards the right of the board. Consult the schematic in (Figure 5) for details.

## 2.2 Layout Guidelines

PCB design is critical to reducing parasitic inductances, with critical components being closely placed next to the IC. The critical components are the loop compensation RC, the slope resistor, and the low ESR ceramic input capacitors. Avoid placing traces or components under the LX shapes to avoid noise coupling from the switching node.

## 2.3 Schematic Diagrams

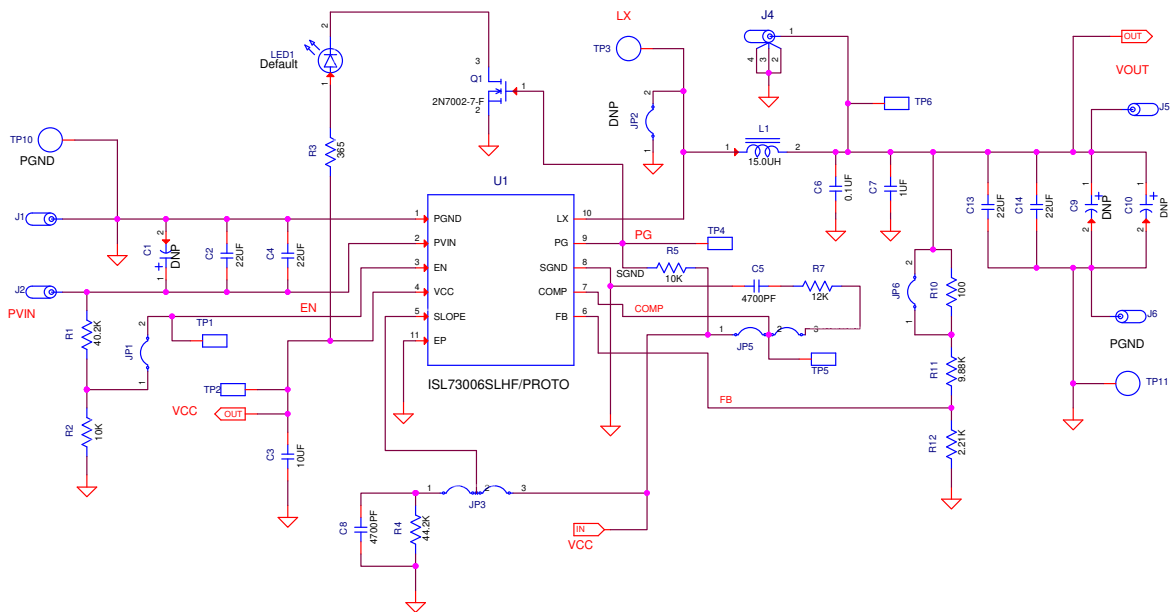


Figure 5. ISL73006SLHEV1Z Schematic

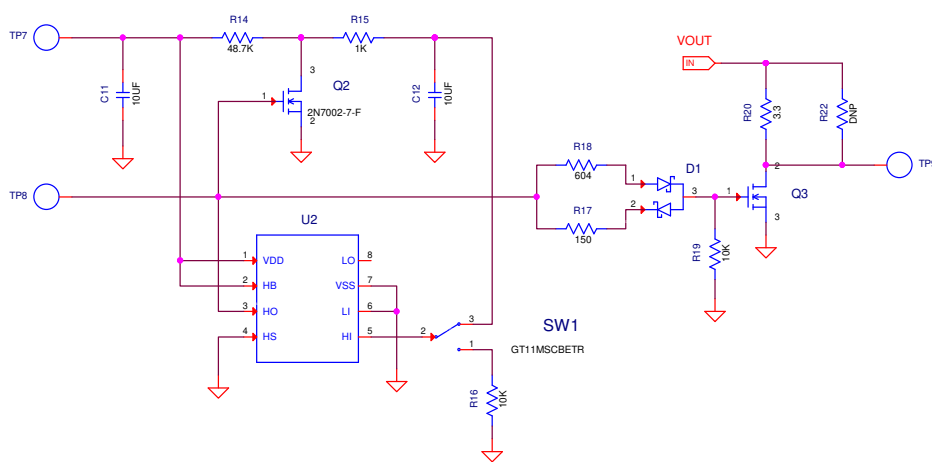


Figure 6. Transient Generator Schematic

## 2.4 Bill of Materials

Reference Designator	Description	Manufacturer	Manufacturer Part
U1	IC-RAD HARD 1A POL REGULATOR	Renesas Electronics	ISL73006SLHF/PROTO
L1	COIL-PWR INDUCT, SMD, 5.4×5.2mm, 15μH.20%, 3.7A, 76.6mohm, ROHS	Coilcraft	XEL5050-153MEC
C2, C4, C13, C14	22μF, Multilayer Cap	Various	Generic
C3	10μF, Multilayer Cap	Various	Generic
C5	4700pF, Multilayer Cap	Various	Generic
C6	0.1μF, Multilayer Cap	Various	Generic
C7	1μF, Multilayer Cap	Various	Generic
C8	0.001μF, Multilayer Cap	Various	Generic
R1	40.1kΩ, Thick Film Chip Resistor	Various	Generic
R2, R5	10kΩ, Thick Film Chip Resistor	Various	Generic
R3	365Ω, Thick Film Chip Resistor	Various	Generic
R4	44.2kΩ, Thick Film Chip Resistor	Various	Generic
R7	12kΩ, Thick Film Chip Resistor	Various	Generic
R10	100Ω, Thick Film Chip Resistor	Various	Generic
R11	9.88kΩ, Thin Film Chip Resistor	Various	Generic
R12	2.21kΩ, Thick Film Chip Resistor	Various	Generic
JP1	Two Pin Jumper	Generic	JUMPER2_100
JP3, JP5	Three Pin Jumper	Generic	JUMPER-3-100
JP2, JP6	Two Point Differential Test Points	Generic	JUMPER2_100
Q1	N-Channel EMF Effect Transistor (Pb-FREE)	Generic	2N7002-7-F
LED1	AllnGaP Green LED	LITEON	LTST-C190KGKT
<b>Transient Generator Components</b>			
U2	100V/2A Peak High Freq Half Bridge Driver (Pb-FREE)	Renesas	HIP2100IBZ
Q2	N-Channel EMF Effect Transistor (Pb-FREE)	FAIRCHILD	2N7002-7-F
Q3	N-Channel 30V (D-S) MOSFET (RoHS compliant)	VISHAY	SUD50N03-06AP-E3
C11, C12	10μF Ceramic Chip Capacitor	Samsung	CL21B106KOQNNNE
R14	48.7kΩ Thick Film Chip Resistor	Various	Generic
R15	1kΩ Thick Film Chip Resistor	Various	Generic
R16, R19	10kΩ Thick Film Chip Resistor	Various	Generic
R17	150Ω Thick Film Chip Resistor	Various	Generic



Reference Designator	Description	Manufacturer	Manufacturer Part
R18	604Ω Thick Film Chip Resistor	Various	Generic
R20-R22	3.3Ω Thick Film Chip Resistor	Various	Generic
D1	30V 200mA SCHOTTKY BARRIER DIODE	DIODES	BAT54S
SW1	SPDT On-None-On (2 Switch Positions) SM Ultraminiature Toggle Switch	C&K	GT11MSCBETR

## 2.5 Board Layout

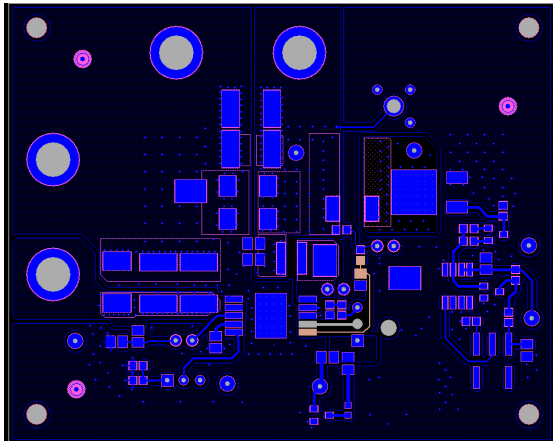


Figure 7. Top Layer

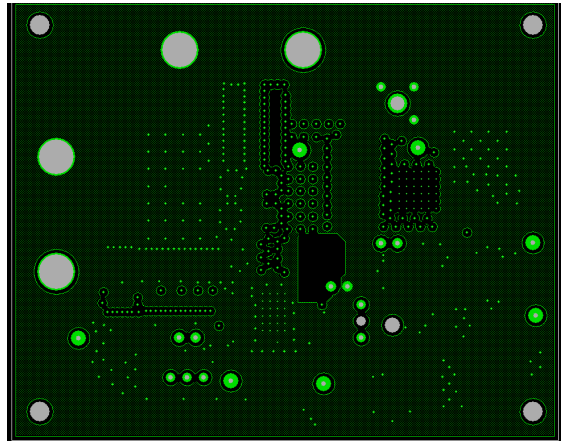


Figure 8. Layer 2

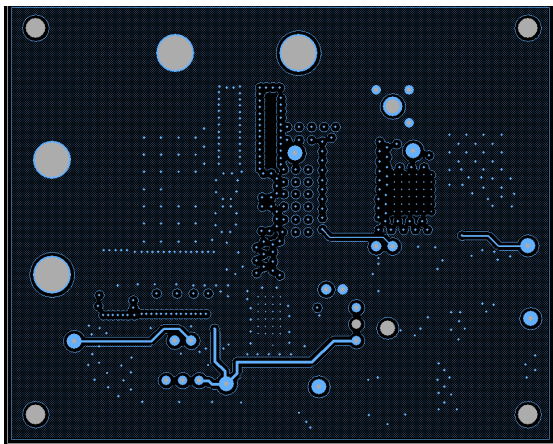


Figure 9. Layer 3

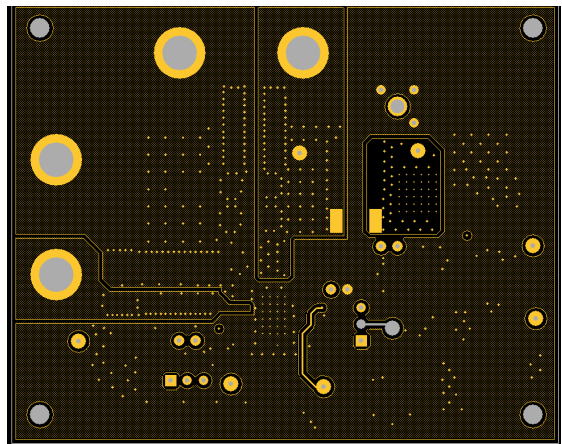


Figure 10. Bottom Layer

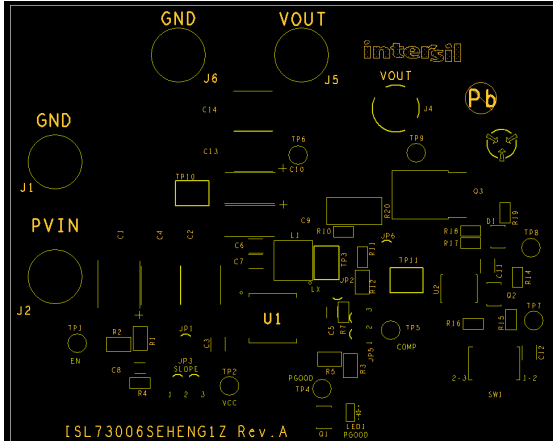


Figure 11. Top Silk Layer

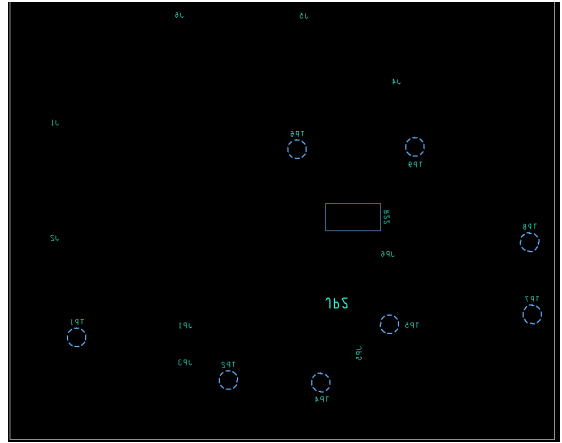


Figure 12. Bottom Silk Layer

### 3. Typical Performance Graphs

Unless otherwise noted,  $P_{VIN} = 12V$ ;  $V_{OUT} = 3.3V$ ,  $f_{SW} = 500kHz$ ,  $T_A = \text{Room Ambient}$

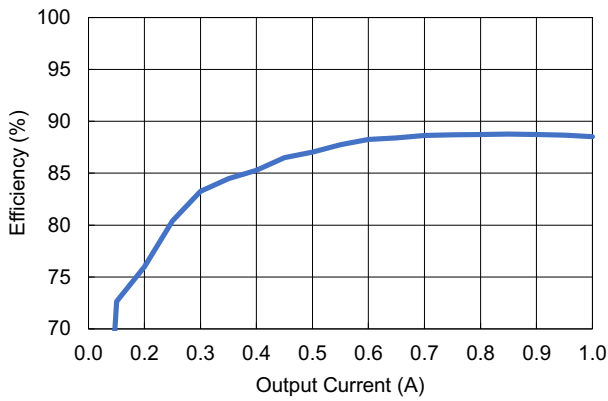


Figure 13. Efficiency

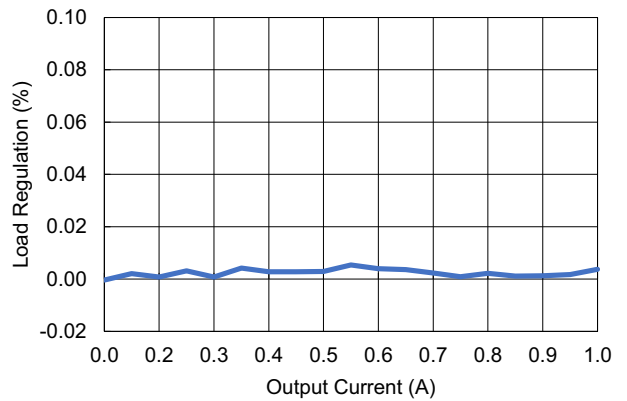


Figure 14. Load Regulation Internal and External Comp

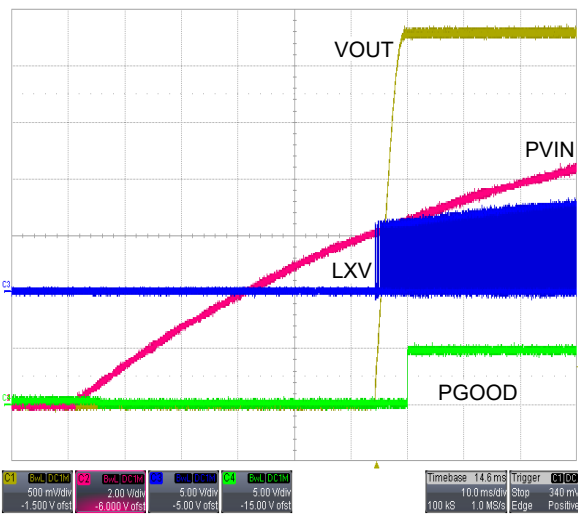


Figure 15. Turn-On by PVIN, 3Ω Load

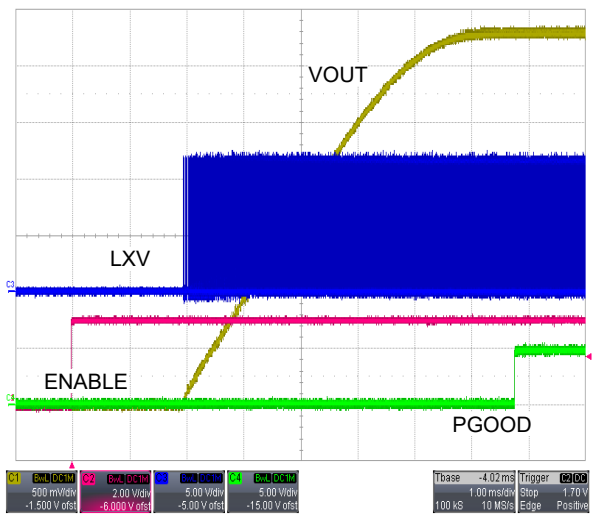


Figure 16. Enabled Turn-On, 3Ω Load



Unless otherwise noted,  $P_{VIN} = 12V$ ;  $V_{OUT} = 3.3V$ ,  $f_{SW} = 500kHz$ ,  $T_A = \text{Room Ambient}$  (Cont.)

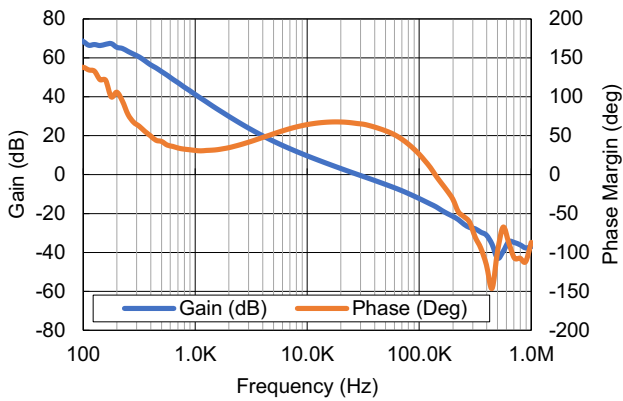


Figure 17. Ext Comp Gain/Phase Bode Plot,  $I_{OUT} = 0.5A$

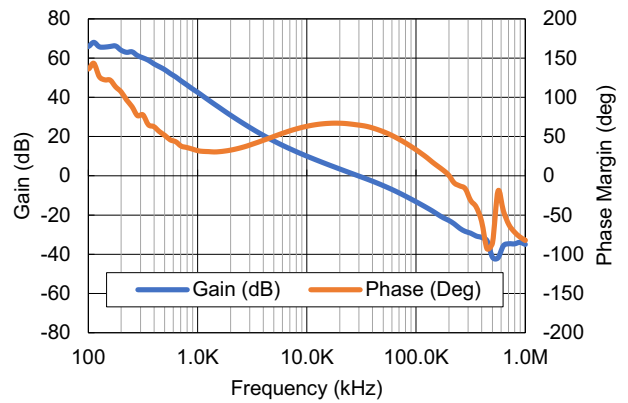


Figure 18. Int Comp Gain/Phase Bode Plot,  $I_{OUT} = 0.5A$

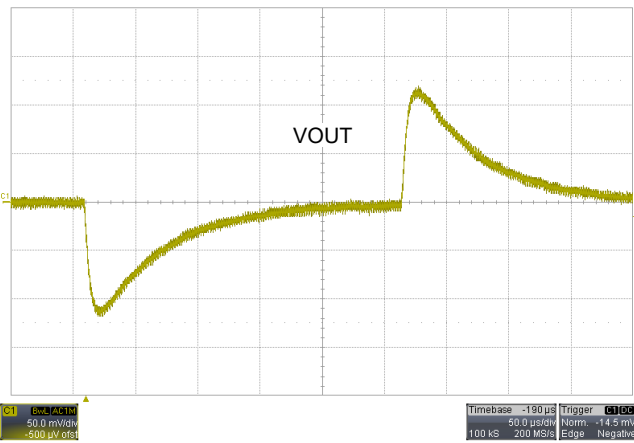


Figure 19. 1A Load Transient (External Compensation)

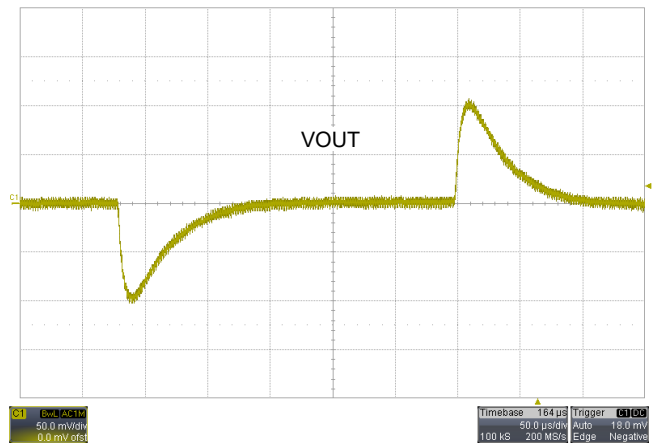


Figure 20. 1A Load Transient (Internal Compensation)

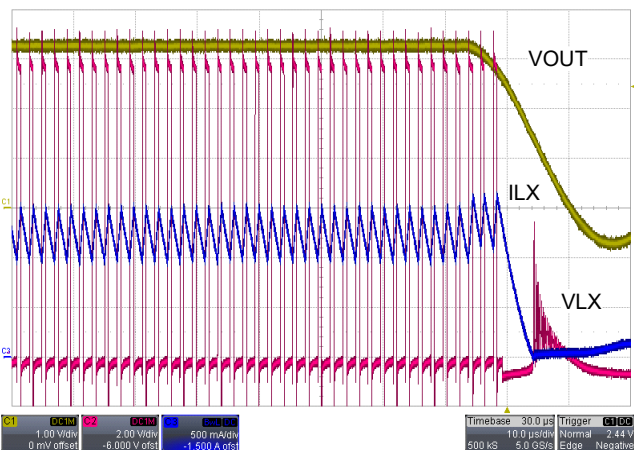


Figure 21. Positive Overcurrent Protection

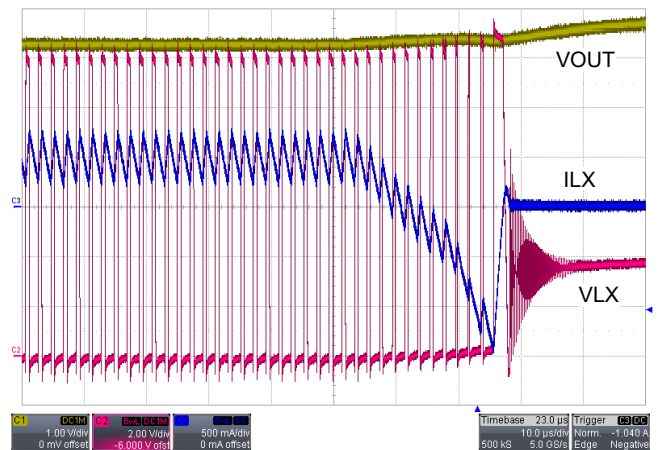


Figure 22. Negative Overcurrent Protection

## 4. Ordering Information

Part Number	Description
ISL73006SLHEV1Z	Radiation Hardened ISL73006SLH buck regulator Evaluation board for $12V_{IN}$ to $3.3V_{OUT}$ , includes feature configuration jumpers for loop and slope compensation, test points, and transient load generator

## 5. Revision History

Revision	Date	Description
1.00	Jan 16, 2024	Initial release

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).