

ISL8112EVAL1Z

Evaluation Board Setup Procedure

AN1539

Rev 0.00

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The ISL8112 is a dual-output Synchronous Buck controller with 2A integrated driver. It features high light load efficiency which is especially preferred in systems concerned with high efficiency in wide load range, like the battery powered system. ISL8112 includes two constant on-time PWM controllers. Both outputs can operate in an output fixed mode or an adjustable mode. In fixed mode, one output can be 5V or 3.3V and the other 1.5V or 1.05V. In adjustable mode, one output can range from 0.7V to 5.5V, and the other from 0V to 2.5V (sensing output voltage directly) or up to 5V (using resistor divider voltage for voltage sensing). This device also features a linear regulator providing 3.3V/5V, or adjustable from 0.7V to 4.5V via LDOREF. The linear regulator provides up to 100mA output current with automatic linear-regulator bootstrapping to the BYP input. When in switchover, the LDO output can source up to 200mA. ISL8112 includes on-board power-up sequencing, the power-good (PGOOD_) outputs, digital soft-start, and internal soft-stop output discharge that prevents negative voltages on shutdown.

ISL8112 is implemented with constant on-time PWM control scheme which need no sense resistors and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The unique ultrasonic pulse-skipping mode maintains the switching frequency above 25kHz, eliminating undesired audible noises in low frequency operation at light load. Other features include pulse skipping which maximizes efficiency in light-load applications, and fixed-frequency PWM mode which reduces RF interference in sensitive applications.

Recommended Equipment

- 0V to 25V power supply with at least 20A source current capability, battery, or notebook AC adapter.
- Two electronic loads capable of sinking current up to 15A.
- Dummy loads for the LDO's.
- Digital multimeters (DMMs).
- 100MHz quad-trace oscilloscope.
- Signal generator.

Quick Start

1. Ensure that the circuit is correctly connected to the supply and loads prior to applying any power.
2. Verify that position 2's are ON for SW1, SW2, SW3, SW4, and SW5. Make sure that no other position of each switch is ON at the same time.
3. Turn on the input power supply.
4. Verify the output voltages are correct.
5. Verify the LDOs output voltages are correct.

Evaluating the Other Output Voltage

The ISL8112EVAL1Z board outputs are preset to 5V/7A, 3.3V/7A and 5V/200mA on LDO. The V_{OUT1} can also be adjusted between 0.7V to 5.5V by changing the value of R_9 and R_{10} or R_{11} and R_{12} given by Equation 1:

$$R_{12} = \frac{R_{11}}{(V_{OUT}/V_{FB}) - 1} \quad (\text{EQ. 1})$$

where $V_{FB} = 0.7V$

- The V_{OUT2} can track OUT2REF at 1:1 ratio with input voltage range from 0.7V to 2.5V. Likewise, the LDO output can also track LDOREF at 1:2 with voltage range from 0.35V to 2.25V.

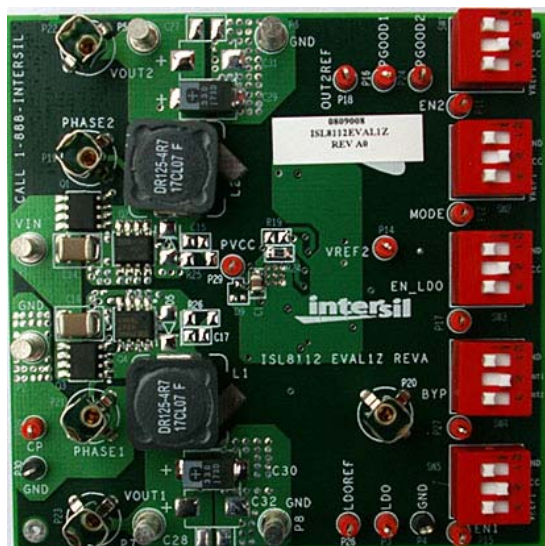


FIGURE 1. TOP VIEW

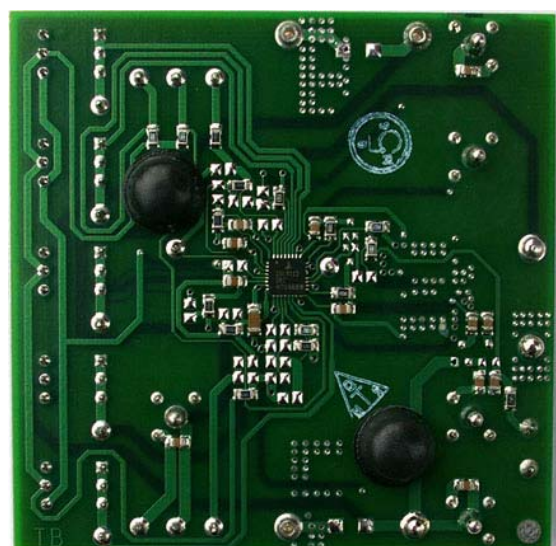


FIGURE 2. BOTTOM VIEW

ISL8112EVAL1Z Board Schematic

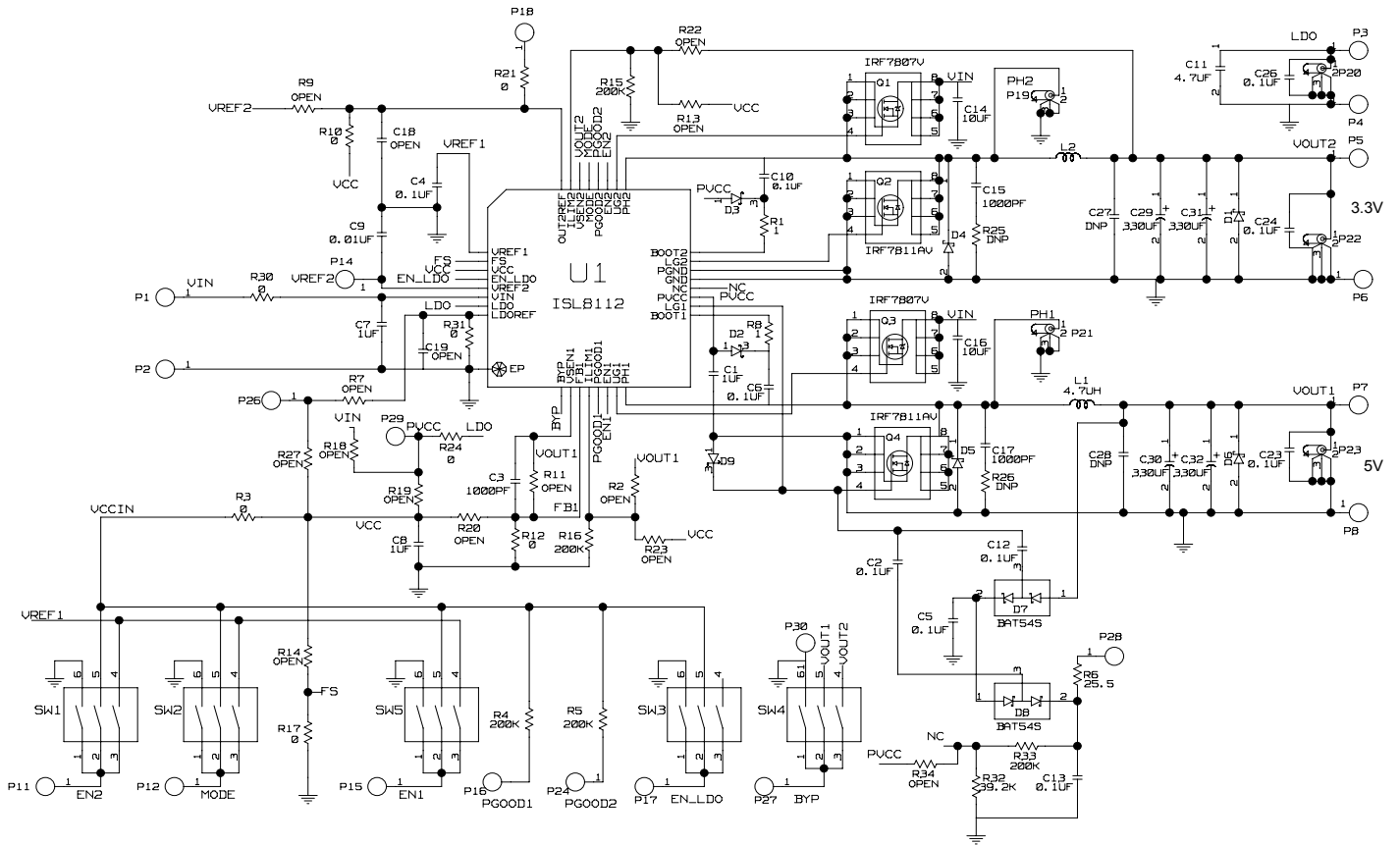


FIGURE 3. ISL8112EVAL1Z REV A BOARD SCHEMATIC

TABLE 1.

SW1	EN2	V _{OUT2} OUTPUT CONTROL
1	Connect to GND.	V _{OUT2} output shutdown.
2	Connect to VCC.	V _{OUT2} output active.
3	Connect to VREF1.	V _{OUT2} sequence to V _{OUT1} output.

NOTE: Only toggle one position at a time.

TABLE 2.

SW2	MODE	OPERATING MODE
1	Connect to GND.	Normal operation mode, allow automatic PWM/PFM switchover for pulse-skipping at light load.
2	Connect to VCC.	Low noise, fixed-frequency PWM mode.
3	Connect to VREF1.	Ultrasonic pulse-skipping mode (20kHz min.)

NOTE: Only toggle one position at a time.

TABLE 3.

SW3	EN_LDO	LDO CONTROL
1	Connect to GND.	LDO output shutdown.
2	Connect to VCC.	LDO output active.
3	N/C	No Connect.

NOTE: Only toggle one position at a time.

TABLE 4.

SW4	BYP	OPERATING MODE
1	Connect to GND.	Set BYP to 0V. No LDO switchover.
2	Connect to V _{OUT1} .	SET BYP to V _{OUT1} .
3	Connect to V _{OUT2} .	SET BYP to V _{OUT2} .

NOTE: Only toggle one position at a time.

TABLE 5.

SW5	EN1	V _{OUT1} OUTPUT CONTROL
1	Connect to GND.	V _{OUT1} output shutdown.
2	Connect to VCC.	V _{OUT1} output active.
3	Connect to VREF1.	V _{OUT1} sequence to V _{OUT2} output.

NOTE: Only toggle one position at a time.

Components List

REF DES	PART NUMBER	QTY	MANUFACTURER	DESCRIPTION
C1, C7, C8	08053D105KAT2A	3	AVX	1 μ F, 25V, X7R, 0805
C11	H1065-00475-10V10	1	GENERIC	4.7 μ F, 10V X5R 1206
C14, C16	TMK432BJ106KM	2	TAIYO-YUDEN	10 μ F, 25V X5R 1210
C2, C4, C5, C6, C10, C12, C13, C23, C24, C26	H1046-00104-50V10	10	GENERIC	0.1 μ F, 50V, X7R, 0805
C27, C28	OPEN	0	-	-
C29, C30	6TPD330M	2	POSCAP SANYO	330 μ F, 6.3V, POS CAP 9m Ω , D size
C3, C9, C15, C17, C18, C19	OPEN	0	-	-
C31, C32	OPEN	0	POSCAP	-
D1, D4-D6	OPEN	0	DIODES-INC	-
D2, D3	OPEN	0	ON-SEMI	-
D7, D8	OPEN	0	DIODES	-
D9	OPEN	0	ON-SEMI	0.3A, 30V, Schottky SOT23
L1, L2	DR125-4R7-R	2	COOPER/COILTRONICS	4.7 μ H, 10.5m Ω , 12.5x12.5mm Shielded
P1, P2, P5-P8	1514-2	6	KEYSTONE	Test Point Turret 0.150 Pad 0.100 Thole
P19-P23	131-4353-00	5	TEKTRONIX	Scope Probe Test Point PCB Mount
P3, P11, P12, P14-P18, P24, P26-P29	5000	13	KEYSTONE	Miniature Red Test Point 0.100 Pad 0.040 Thole
P4, P30	5001	2	KEYSTONE	Miniature Black Test Point 0.100 Pad 0.040 Thole

Components List (Continued)

REF DES	PART NUMBER	QTY	MANUFACTURER	DESCRIPTION
Q1	IRF7821	1	IR	30V 13.6A HEXFET Power MOSFET
Q2	IRF7832	1	IR	30V 20A HEXFET Power MOSFET
Q3	IRF7807V	1	IR	30V 8.3A N-Channel Power MOSFET
Q4	IRF7811AV	1	IR	30V 10.8A N-Channel Power MOSFET
R1, R8	H2512-01R00-1/10W	2	GENERIC	1Ω, 1%, 0805
R15	H2512-01503-1/10W1	1	GENERIC	150kΩ, 1%, 0805
R2, R7, R9, R11, R13, R14, R18, R19, R20, R22, R23, R27, R34	OPEN	0	-	-
R25, R26	OPEN	0	-	-
R3, R10, R12, R17, R21, R24, R30, R31	H2512-00R00-1/10W	8	GENERIC	0Ω, 1%, 0805
R32	H2512-03922-1/10W1	1	GENERIC	39.2kΩ, 1%, 0805
R4, R5, R16, R33	H2512-02003-1/10W1	4	GENERIC	200kΩ, 1%, 0805
R6	H2512-025R5-1/10W1	1	GENERIC	25.5Ω, 1%, 0805
SW1-SW5	78B03S	5	GRAYHILL	Dip Switch SPST (Raised Slide)
U1	ISL8112IRZ	1	INTERSIL	High-Efficiency, Quad Output Controller

Layout

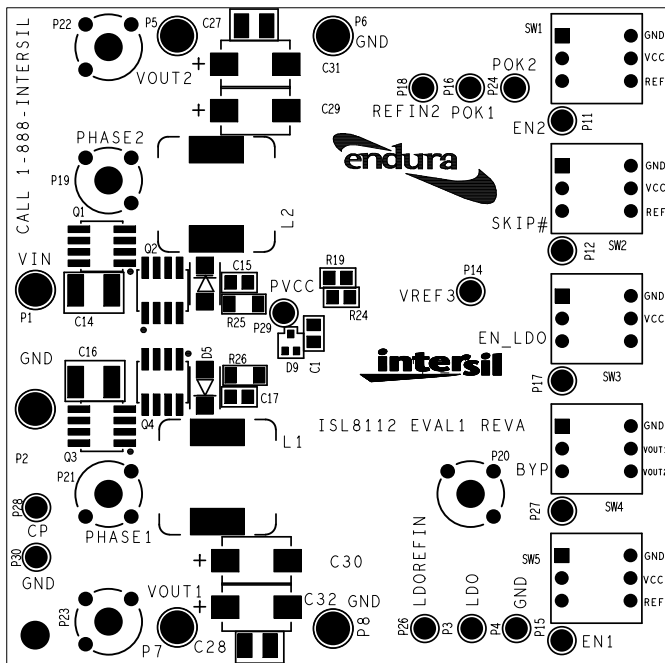


FIGURE 4. TOP COMPONENTS

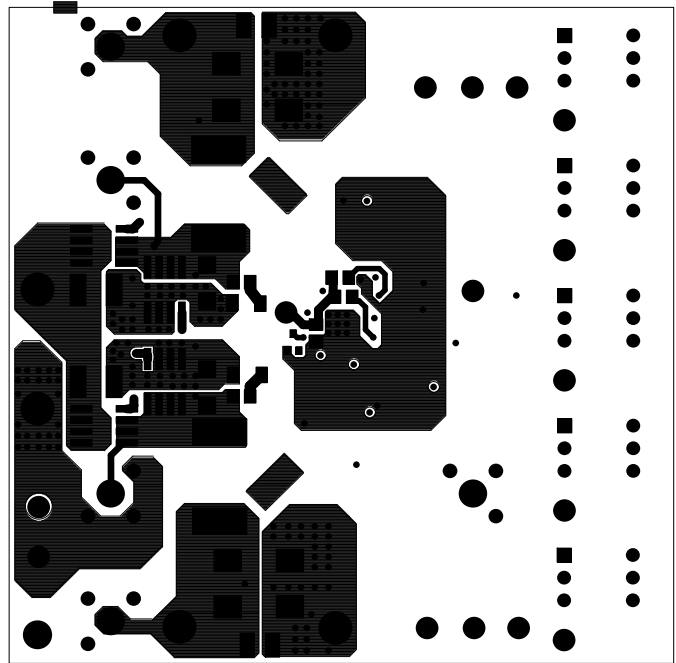


FIGURE 5. TOP ETCH

Layout (Continued)

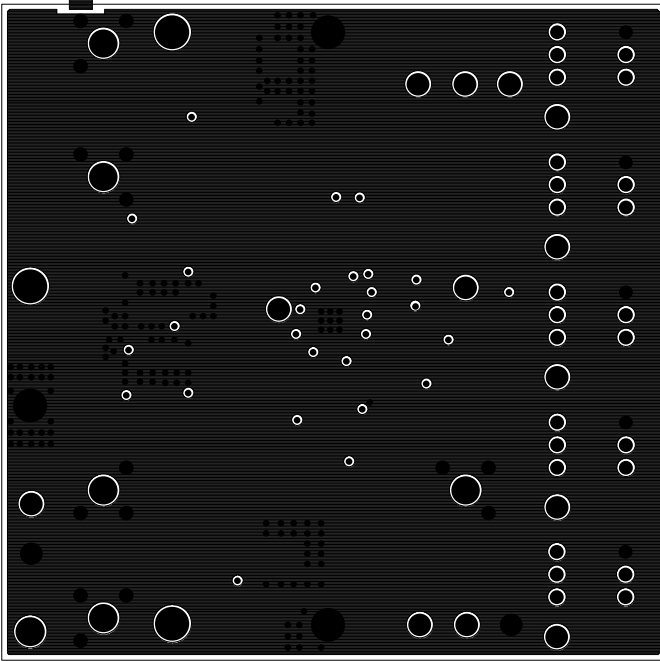


FIGURE 6. 2nd LAYER

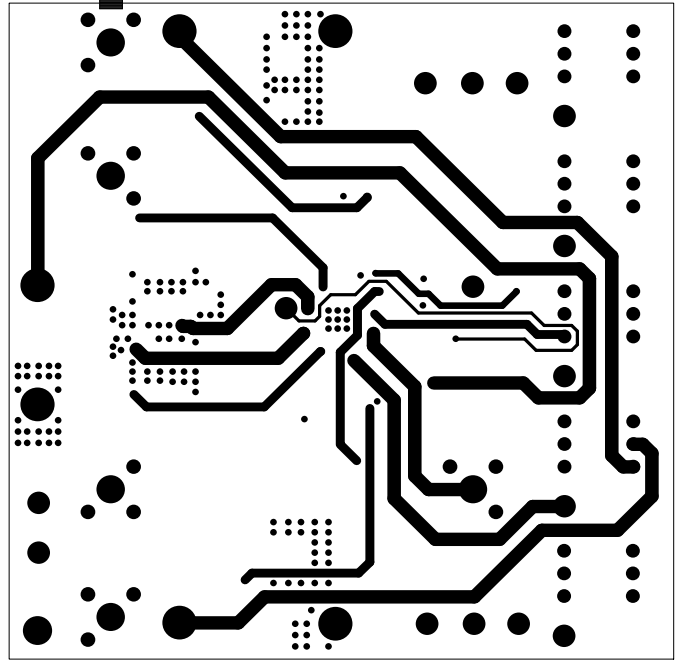


FIGURE 7. 3rd LAYER

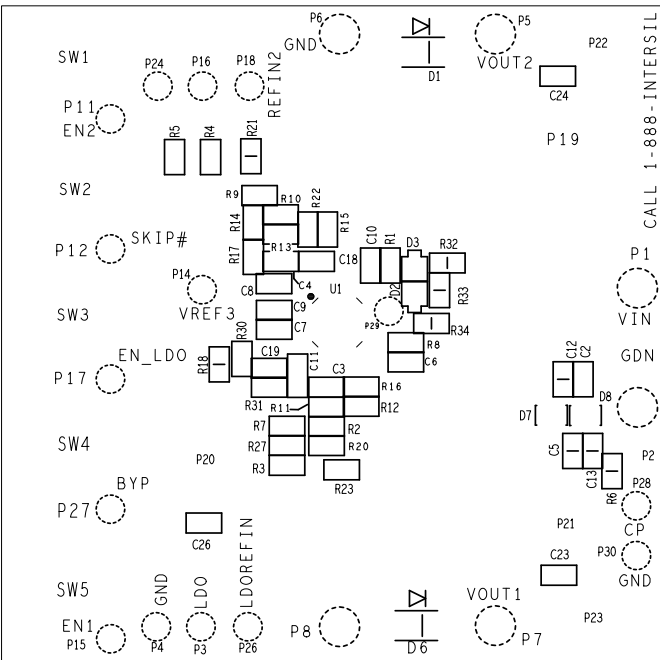


FIGURE 8. BOTTOM COMPONENTS (MIRRORED)

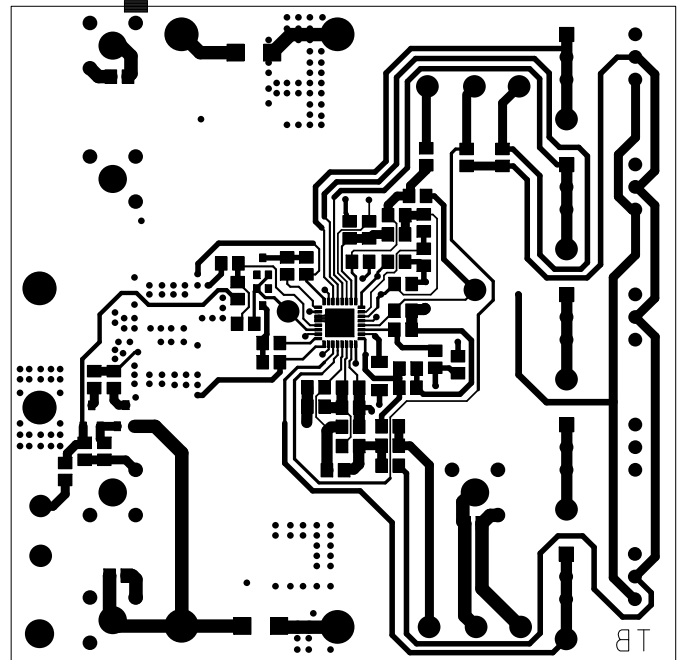


FIGURE 9. BOTTOM ETCH

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