ISL8200AMEVAL2PHZ Evaluation Board User's Guide

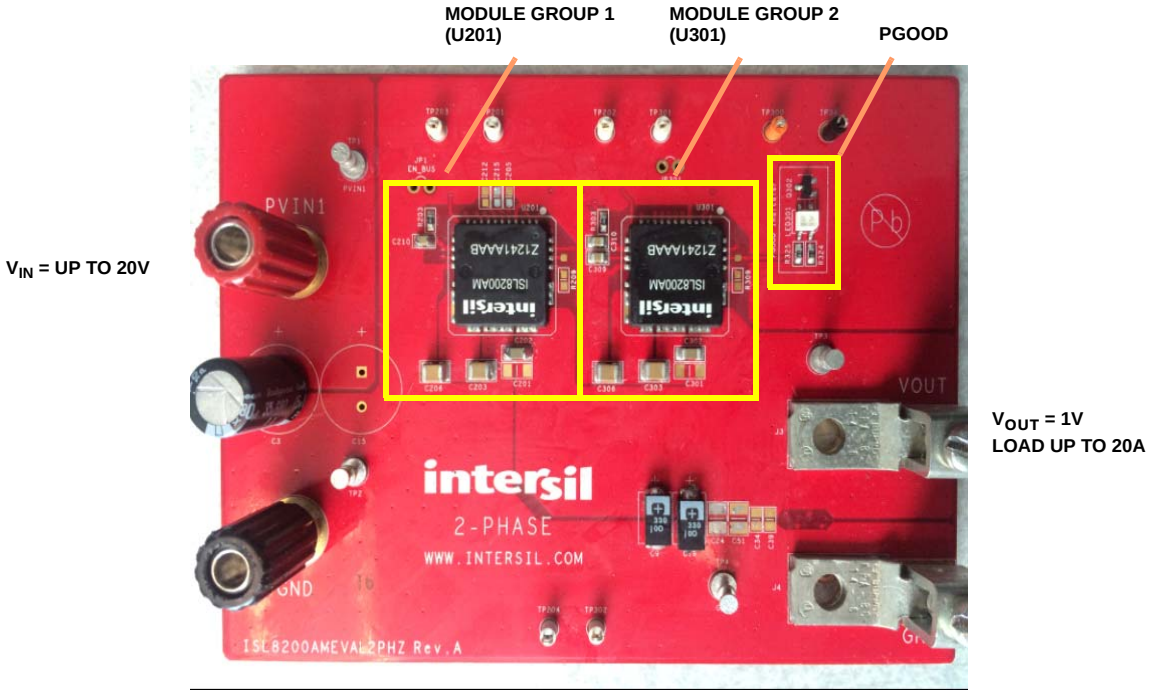

FIGURE 1. ISL8200AMEVAL2PHZ EVALUATION BOARD

ISL8200AMEVAL2PHZ Evaluation Board

The ISL8200AM is a complete 10A step-down current shareable switch mode power module in a low profile package. It can be used in a standalone single-phase operation as well as current shared applications where multiple modules are connected in parallel.

The ISL8200AMEVAL2PHZ evaluation board is used to demonstrate performance of the ISL8200AM 2-phase current shared application. The input voltage range can be up to 20V, and the output voltage is 1V and 20A maximum load. The output voltage can support a range up to 6V with the proper output capacitor rating.

TABLE 1. EVALUATION BOARD ELECTRICAL SPECIFICATIONS

DESCRIPTION	MIN	TYP	MAX	UNIT
Input Voltage	5		20	V
Output Voltage	0.6	1	6	V
Output Current		20		A
Switching Frequency	700	800	1500	kHz
Efficiency, V_{IN} = 8V, V_{OUT} = 5V, F_{SW} = 900kHz, I_{OUT} = 10A		94.1		%

TABLE 2. RECOMMENDED COMPONENT SELECTION FOR QUICK EVALUATION

V_{OUT} (V)	I_{OUT} (A)	C_{213}/C_{313} (pF)	F_{SW} (kHz)	R_{FSYNC} (kΩ)
1	20	OPEN	800	59
2.5	20	OPEN	850	55
3.3	20	680/680	1050	45
5	20	680/680	1150	41

Recommended Equipment

- 0V to 20V power supply with at least 15A source current capability
- One Electronic Load capable of sinking current up to 20A
- Digital multi-meters (DMMs)
- 100MHz quad-trace oscilloscope
- Signal generator (for synchronization demonstration)

Circuits Description

PVIN1 and GND banana plugs are the input power terminals.

Two input electrolytic capacitor footprints are provided to handle the input current ripple.

Two SANYO POSCAP 2TPF330M6 (330µF, ESR 6mΩ) are used as output E-caps for each channel. Also, capacitor footprints are available for the user to evaluate different output capacitors.

J_3, J_4 are output lugs for load connections.

TP301 is the clock output. The default phase shift of the CLKOUT signal from module 1 (U201) causes the second to switch with a phase shift of 180°, which can be observed by the relative phase between PHASE2 and PHASE3 signals as shown in Figures 37 and 38.

R_{203}, R_{303} and C_{210}, C_{310} are small added filters for the VIN pins.

Quick Start

1. Ensure that the circuit is correctly connected to the supply (PVIN1 and GND banana plugs) and load (J_3 and J_4) prior to applying any power.
2. Adjust the input supply to be 5V. Turn on the input power supply.
3. Verify the two outputs' voltages are correct. If the PGOOD is set high, LED301 will be green. If the PGOOD is set low, LED301 will be red. TP300 is the test post to monitor PGOOD.

Evaluating Other Output Voltages

The ISL8200AMEVAL2PHZ kit outputs are preset to 1.0V/20A. V_{OUT} can also be adjusted between 0.6V to 6V by changing the value of R_{221} and R_{321} simultaneously as given by Equation 1.

$$R_{221} = \frac{(V_{OUT} - V_{REF})}{(V_{REF})} ROS \quad \text{where } V_{REF} = 0.6V,\ ROS = 2.2k \text{ internal} \qquad \text{(EQ. 1)}$$

The output capacitors must be changed to support the corresponding output voltage. The onboard output capacitors are rated at 6.3V max.

For different output voltage, adjust F_{SW} according to Figure 2. The frequency selection resistor (R_{FSYNC}) can be estimated by Equation 2.

$$R_{FSYNC}[k\Omega] = 4.671 \times 10^{4} \cdot Fsw[kHz]^{-1.04} \qquad \text{(EQ. 2)}$$

Where $R_{FSYNC} = R_{223}//59k$, 59k is the internal resistor.

For high output applications, the feedback gain is reduced, so the 0dB cross-over frequency is pushed closer to the LC resonance frequency. Please add a zero in the loop to have better stability. We recommend using 680pF capacitors at C_{213} and C_{313} to boost the phase margin.

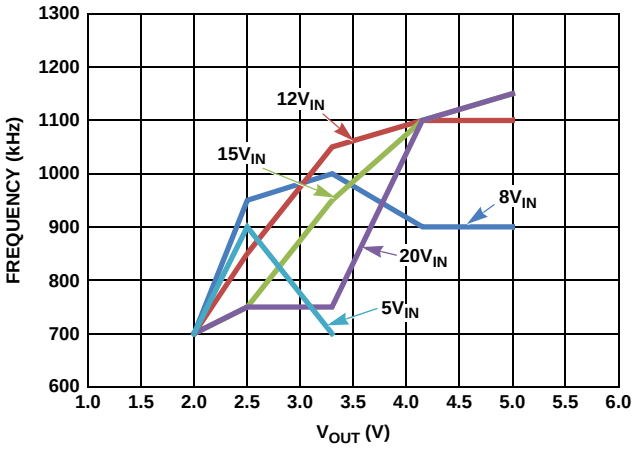

FIGURE 2. OPTIMUM FREQUENCY vs V_{OUT}

Programming the Input Voltage UVLO and its Hysteresis

By programming the voltage divider at the EN pin connected to the input rail, the input UVLO and its hysteresis can be programmed. The ISL8200AMEVAL2PHZ has R_1 = 8.25k and R_2 = 2.05k; the IC will be disabled when the input voltage drops below 4.5V and will restart after V_{IN} recovers to be above 4.0V.

The UVLO equations are re-stated in the following, where R_{UP} and R_{DOWN} are the upper and lower resistors of the voltage divider at EN pin, V_{HYS} is the desired UVLO hysteresis and V_{FTH} is the desired UVLO falling threshold.

$$R_{UP} = \frac{V_{HYS}}{I_{HYS}} \quad \text{where } I_{HYS} = N \times 30\mu A,\ N = \text{number of phases (= 2)} \qquad \text{(EQ. 3)}$$

$$R_{DOWN} = \frac{R_{UP} \cdot V_{ENREF}}{V_{FTH} - V_{ENREF}} \quad \text{where } V_{ENREF} = 0.6V \qquad \text{(EQ. 4)}$$

For 12V applications, if it is desired to have the IC disabled when the input voltage drops below 9V and restart when V_{IN} recovers above 10.6V, then R_1 = 16.5k and R_2 = 2.6k.

Efficiency Measurement

Figures 12 through 27 show the efficiency measurement for the ISL8200AMEVAL2PHZ Evaluation Board. The voltage and current meter can be used to measure input/output voltage and current. In order to obtain an accurate measurement and prevent the voltage drop of PCB or wire trace, the voltage meter must be close to the input/output terminals. For simplicity, the measuring point for the input voltage meter is at the TP1 terminal, and the measuring point for the output voltage meter is at the TP3 terminal.

The efficiency equation is shown in Equation 5:

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{IN}} = \frac{(V_{OUT} \bullet I_{OUT})}{(V_{IN} \bullet I_{IN})} \quad \text{(EQ. 5)}$$

Output Ripple/Noise Measurement

Simple steps should be taken to ensure that there is minimum pickup noise due to high frequency events, which can be magnified by the large ground loop formed by the oscilloscope-probe ground. This means that even a few inches of ground wire on the oscilloscope probe may result in hundreds of millivolts of noise spikes when improperly routed or terminated. This effect can be overcome by using the short loop measurement method to minimize the measurement loop area for reducing the pickup noise. The short loop measurement method is shown in Figure 3. For ISL8200AMEVAL2PHZ evaluation board, the output ripple/noise measurement point is located at the C_{202}/C_{302} terminal.

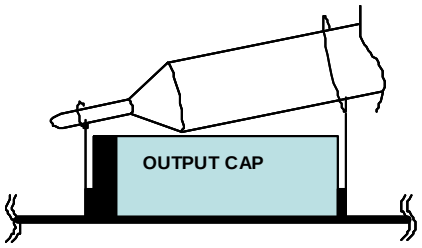

FIGURE 3. OUTPUT RIPPLE/NOISE MEASUREMENT

ISL8200AMEVAL2PHZ Schematic

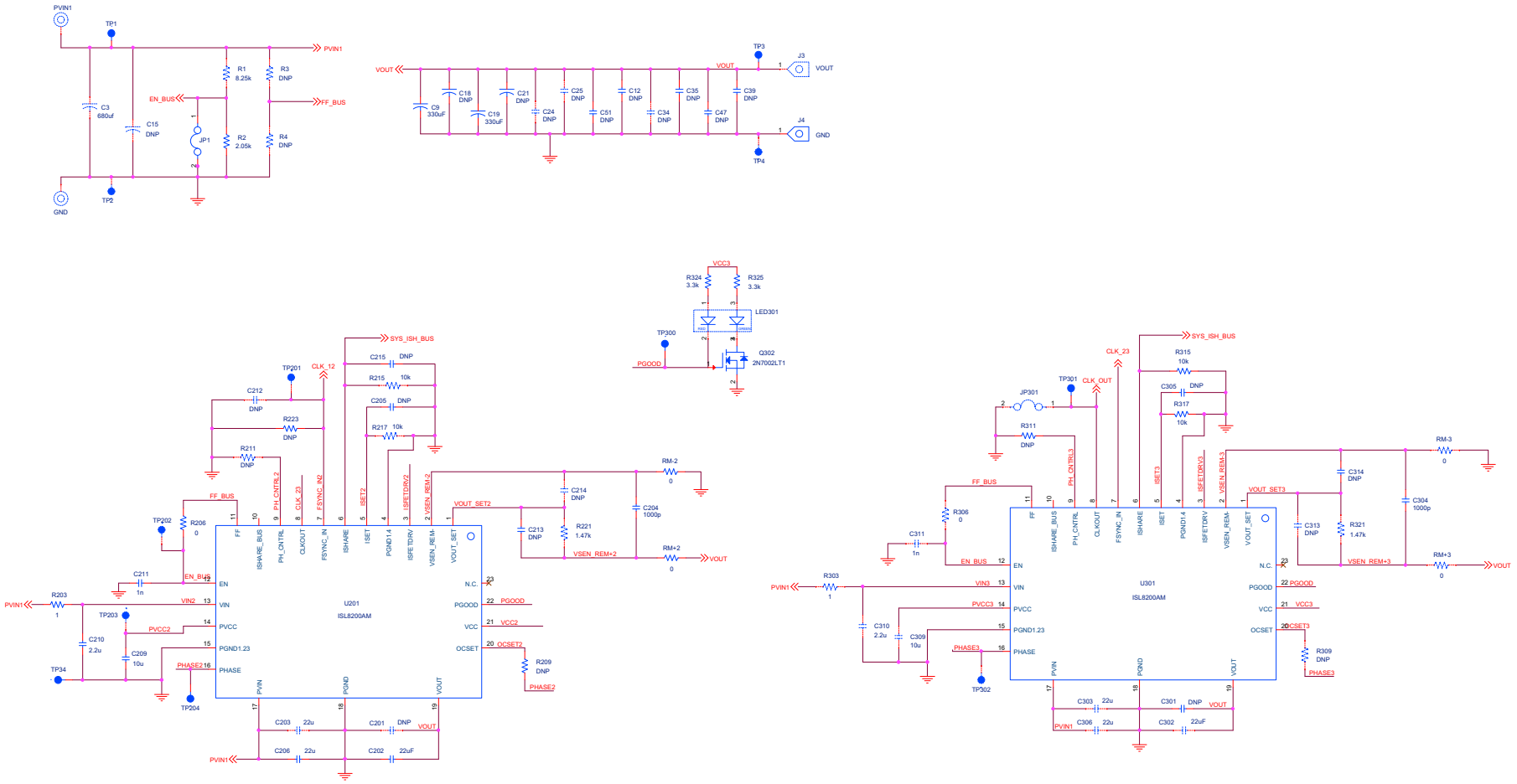

FIGURE 4.

ISL8200AMEVAL2PHZ Bill of Materials

CH2	CH3	COMMON	COMPONENTS VALUE	PART NUMBER	PART DESCRIPTION	COMMENTS
U201	U301			ISL8200AM		Module
R206	R306		0		RES, SMD, 0603, 0Ω, 1/16W, TF, ROHS	FF-EN Connection
R203	R303		1		RES, SMD, 0603, 1Ω, 1/10W, 1%, TF, ROHS	PVIN-VIN
R215	R315		10k		RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	RISHARE
R217	R317		10k		RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	RISET
R221	R321		1.47k		RES, SMD, 0603, 1.47k, 1/10W, 1%, TF, ROHS	RFB_TOP
RM+2, RM-2	RM+3, RM-3		0		RES, SMD, 0603, 0Ω, 1/16W, TF, ROHS	REM_SENS+/-
		R1	8.25k		RES, SMD, 0603, 8.25kΩ, 1/10W, 1%, TF, ROHS	EN-Top
		R2	2.05k		RES, SMD, 0603, 2.05k, 1/10W, 1%, TF, ROHS	EN-Bottom
C211	C311		1nF		CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	CEN-Bottom
C209	C309		10µF		CAP, SMD, 0805, 10µF, 16V, 10%, X5R, ROHS	PVCC_cap
C210	C310		2.2µF		CAP, SMD, 0805, 2.2µF, 25V, 10%, X5R, ROHS	VIN_cap
C204	C304		1000p		CAP, SMD, 0603, 1000pF, 50V, 5%, COG, ROHS	SENS_FILTER
		C3	680µF		CAP, ALUMINUM, RADIAL, 680µF, 35V	Cin_elec_common
C203, C206	C303, C306		22µF		CAP, SMD, 1210, 22µF, 25V, 20%, X5R, ROHS	Cin_Ceremic_1
C202	C302		22µF		CAP, SMD, 1206, 22µF, 16V, 10%, X5R, ROHS	
		C9, C19	330µF	6TPF330M6L	POSCAP 6.3V 9mΩ	Cout_Bulk1
PGOOD and Additional Placeholder						
		Q302		2N7002	TRANSISTOR, N-CHANNEL, SOT-23, 60V, 115mA, ROHS	PGOOD_NFET
		LED301		SSL-LXA3025IGC-TR	LED, SMD, 3x2.5mm, 4P, RED/GREEN, 2V, ROHS	PGOOD_LED
		R324, R325	3.3k		RES, SMD, 0603, 3.32k, 1/10W, 1%, TF, ROHS	PGOOD_RES
		C12, C18, C21, C24, C25, C34, C35, C39, C47, C51	DNP			Cout
		C212	DNP			FSYNC_IN2_cap
		R223	DNP			FSYNC_IN2_resistor
C205	C305		DNP			ISET_cap
		C215	DNP			ISHARE_cap
R209	R309		DNP			
		C15	DNP			Cin_elec_common

ISL8200AMEVAL2PHZ Bill of Materials (Continued)

CH2	CH3	COMMON	COMPONENTS VALUE	PART NUMBER	PART DESCRIPTION	COMMENTS
		R3, R4	DNP			FF-Top, FF-Bottom
R211	R311		DNP			PH_CNTRL
C213	C313		DNP			CFB_TOP
C214	C314		DNP			CFB_BOTTOM
C201	C301		DNP			
Connectors and Test Points						
TP201				5002	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	CLK_12 test point
	TP301			5002	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	CLK_23 test point
		TP202		5002	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	EN_BUS test point
		TP203		5002	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	PVCC_test point
TP204	TP304			5002	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	PHASE test point
		TP300		5003	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	PGOOD test point
		TP1, TP2, TP3, TP4		1514-2	CONN-TURRET, TERMINAL POST, TH, ROHS	PVIN1, GND, VOUT, GND Turret Posts
		J3, J4		KPA8CTP	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SC	Lug
		PVIN1		111-0702-001	CONN-BINDING POST, INSUL-RED, THMBNUT-GND, ROHS	Binding Post RED
		GND		111-0703-001	CONN-BINDING POST, INSUL-BLK, THMBNUT-GND, ROHS	Binding Post BLACK
		JP1, JP301	DNP			

ISL8200AMEVAL2PHZ Board Layout

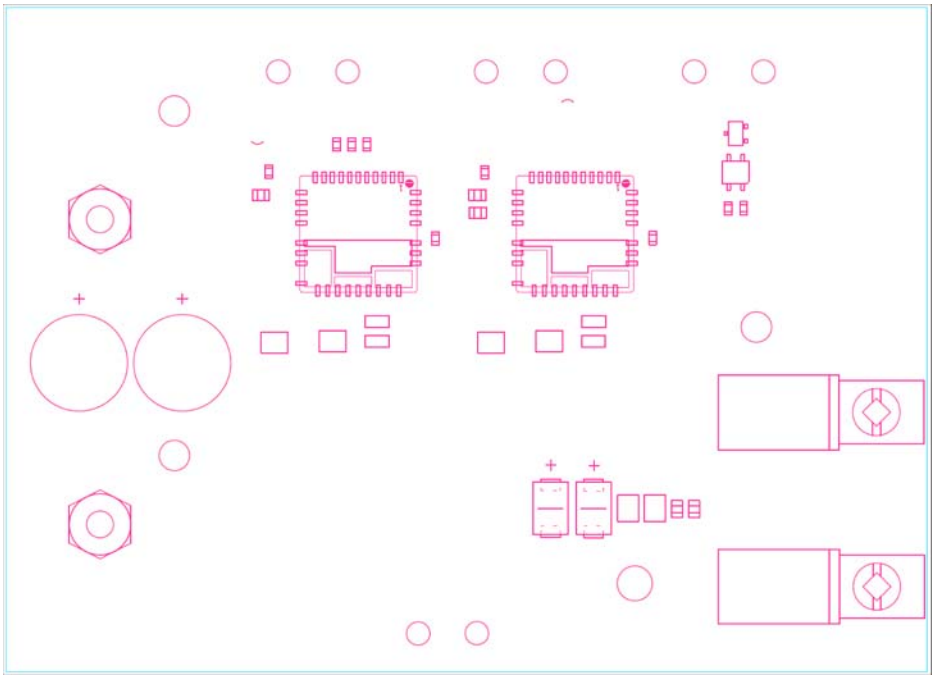

FIGURE 5. ASSEMBLY TOP

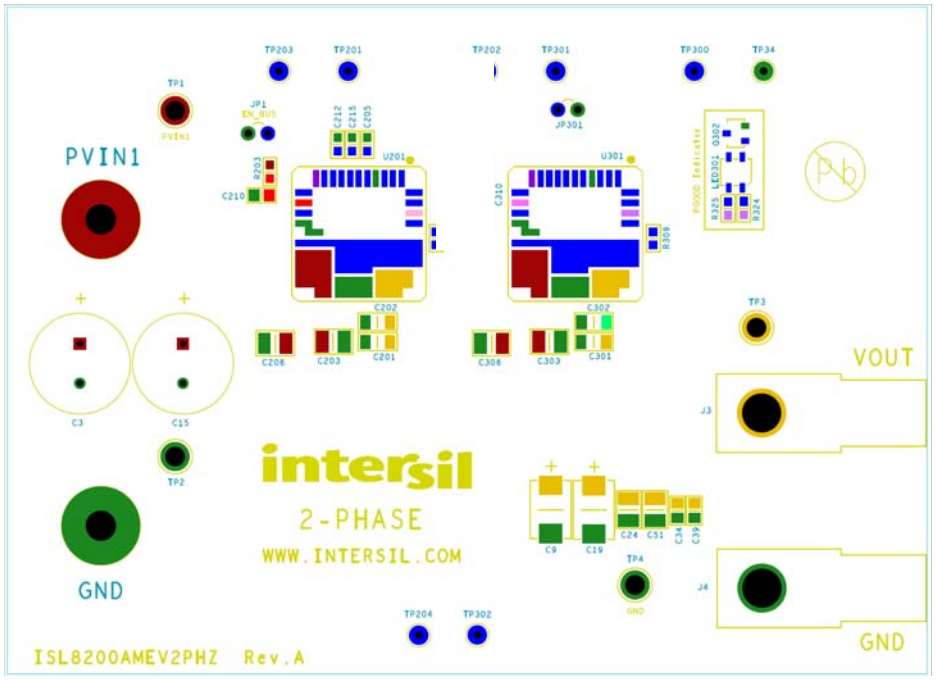

FIGURE 6. TOP SILK

ISL8200AMEVAL2PHZ Board Layout (Continued)

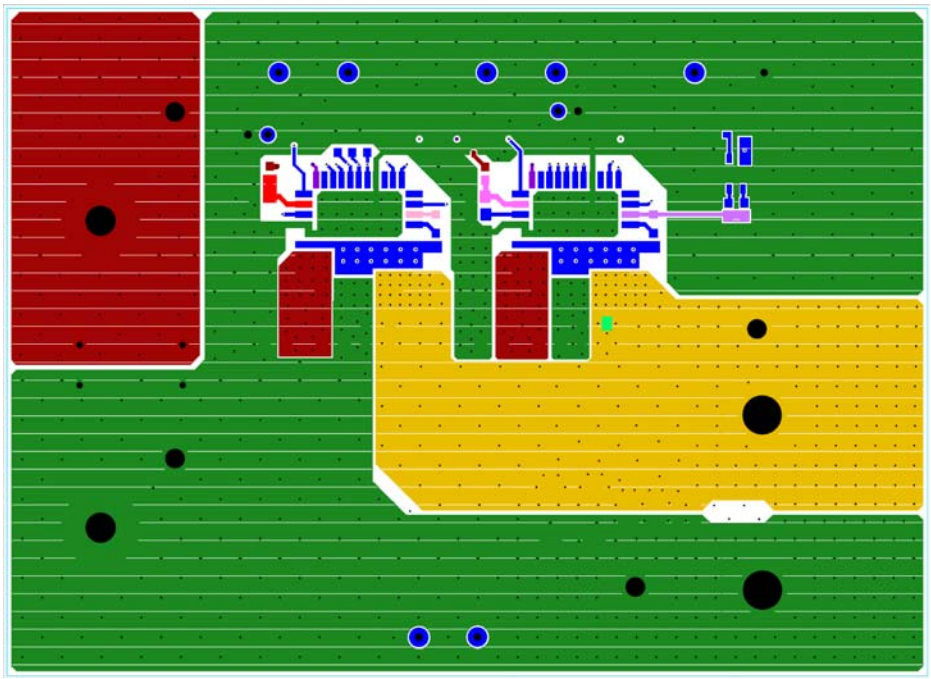

FIGURE 7. COMPONENT SIDE - TOP

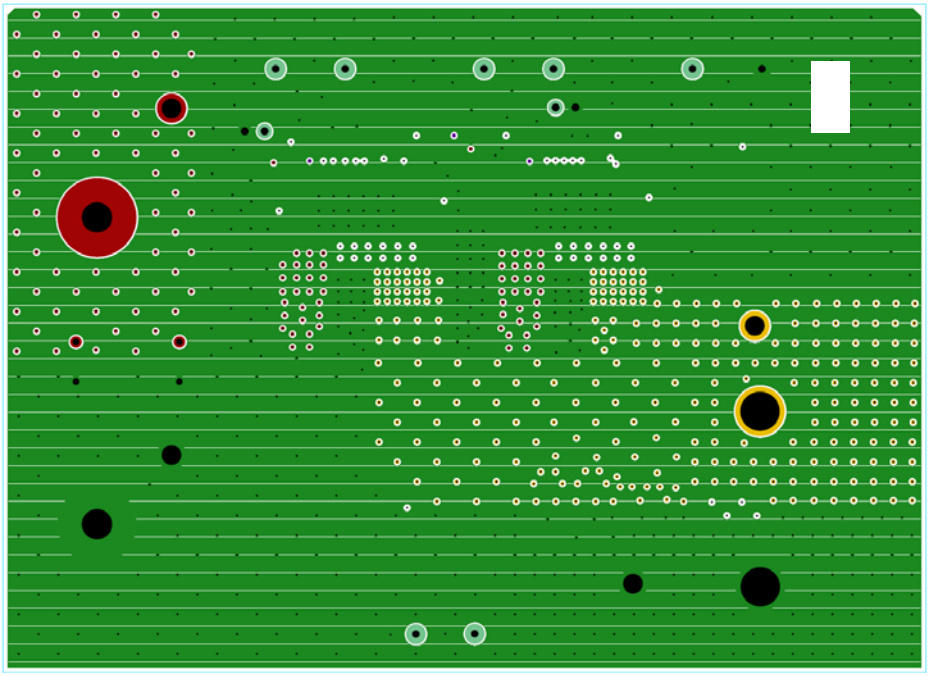

FIGURE 8. LAYER 2

ISL8200AMEVAL2PHZ Board Layout (Continued)

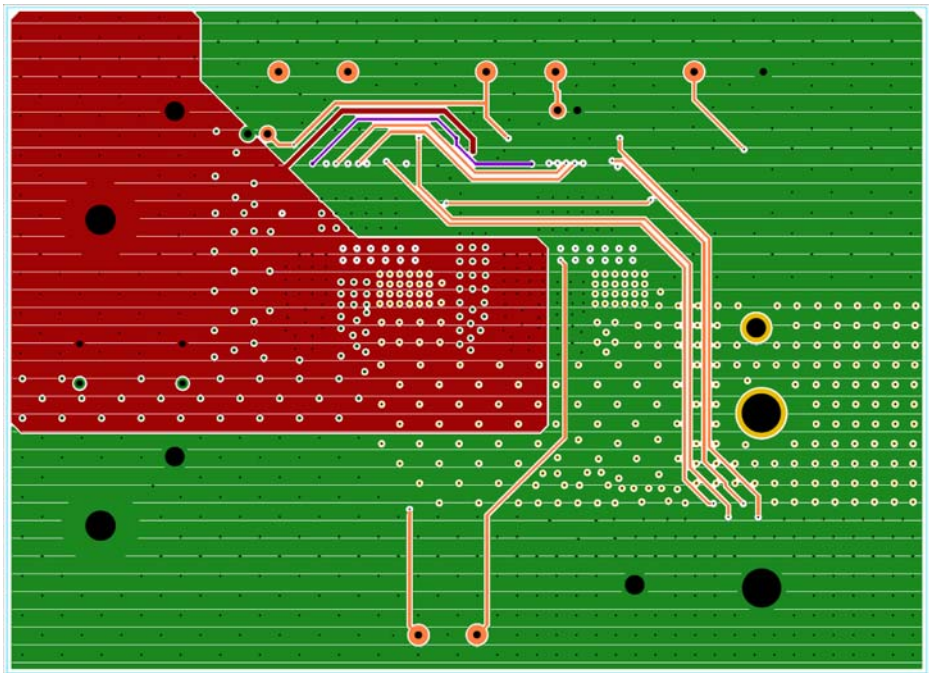

FIGURE 9. LAYER 3

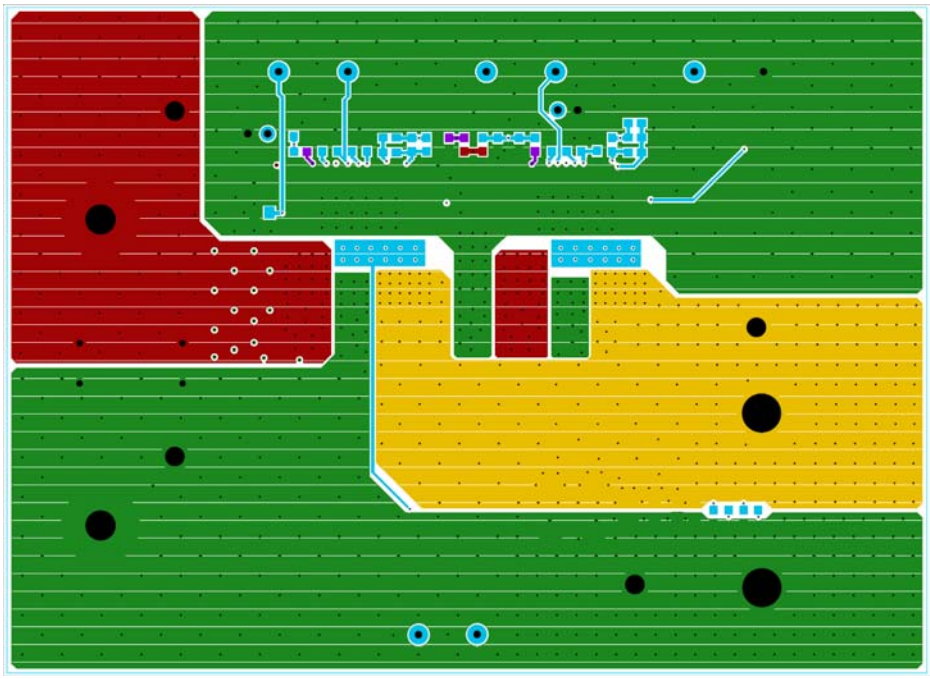

FIGURE 10. BOTTOM LAYER

ISL8200AMEVAL2PHZ Board Layout (Continued)

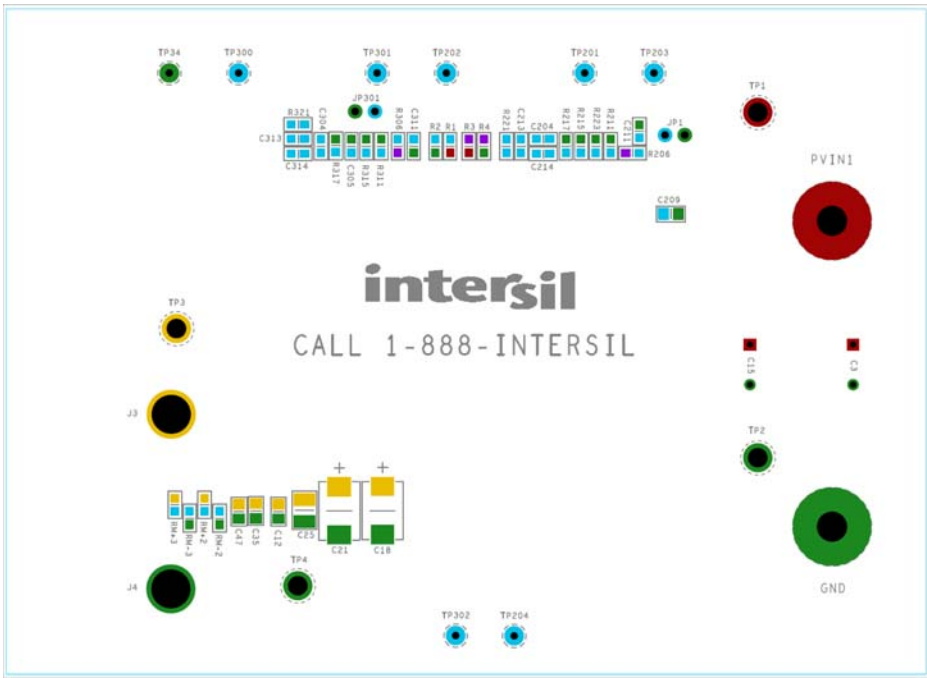

FIGURE 11. SILKSCREEN BOTTOM (MIRRORED)

Test Data for ISL8200AMEVAL2PHZ

Efficiency

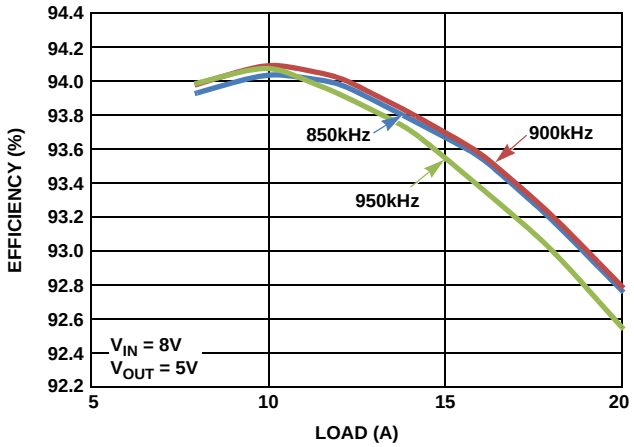

FIGURE 12. EFFICIENCY (V_{IN} = 8V, V_{OUT} = 5V)

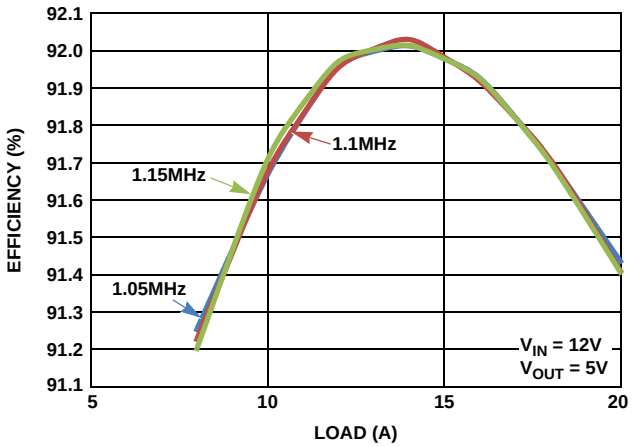

FIGURE 13. EFFICIENCY (V_{IN} = 12V, V_{OUT} = 5V)

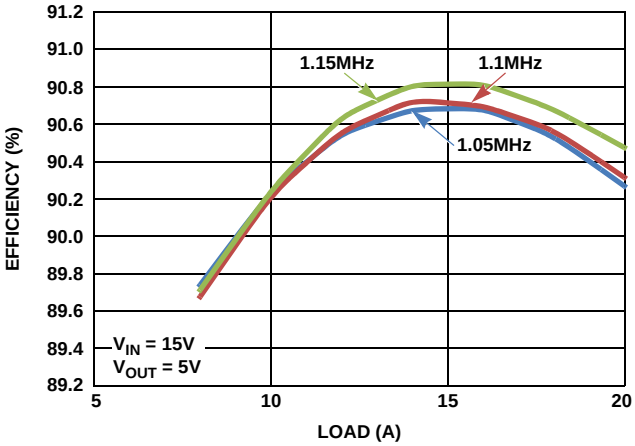

FIGURE 14. EFFICIENCY (V_{IN} = 15V, V_{OUT} = 5V)

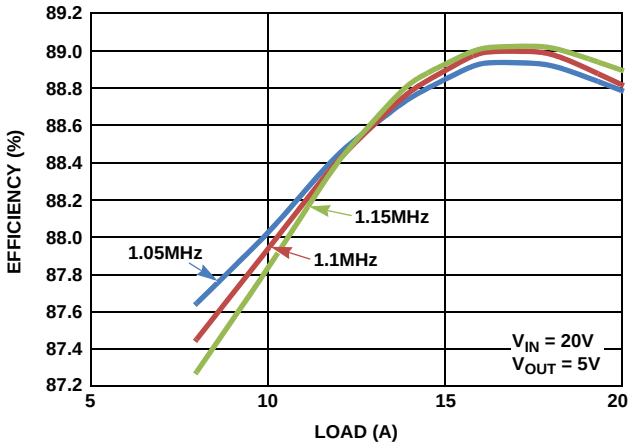

FIGURE 15. EFFICIENCY (V_{IN} = 20V, V_{OUT} = 5V)

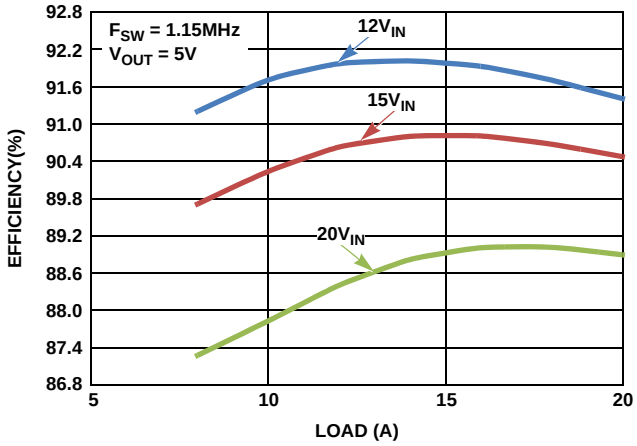

FIGURE 16. EFFICIENCY (F_{SW} = 1.15MHz, V_{OUT} = 5V)

Test Data for ISL8200AMEVAL2PHZ (Continued)

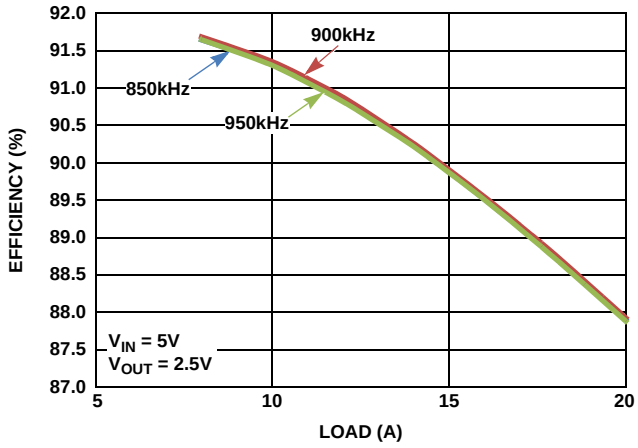

FIGURE 17. EFFICIENCY (V_{IN} = 5V, V_{OUT} = 2.5V)

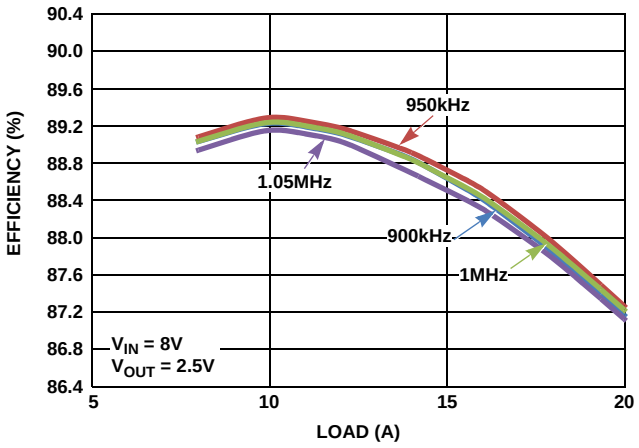

FIGURE 18. (V_{IN} = 8V, V_{OUT} = 2.5V)

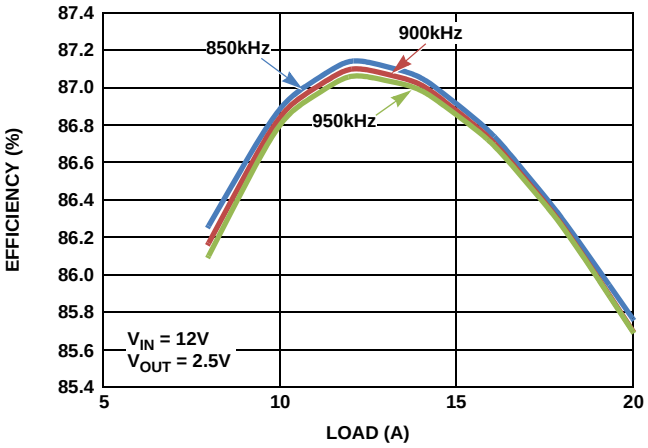

FIGURE 19. EFFICIENCY (V_{IN} = 12V, V_{OUT} = 2.5V)

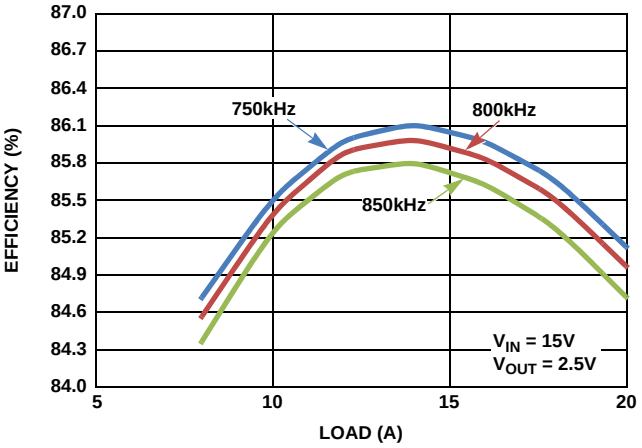

FIGURE 20. EFFICIENCY (V_{IN} = 15V, V_{OUT} = 2.5V)

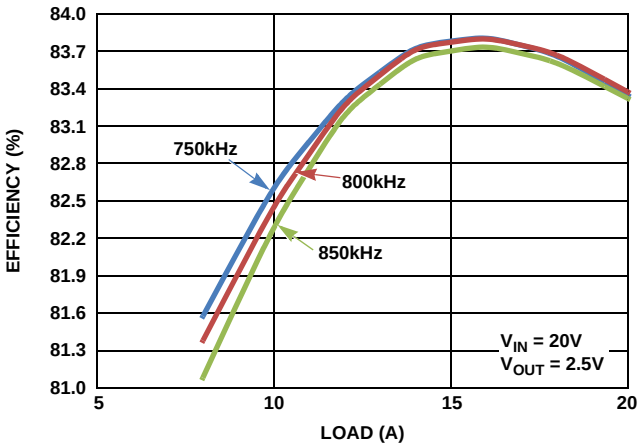

FIGURE 21. EFFICIENCY (V_{IN} = 20V, V_{OUT} = 2.5V)

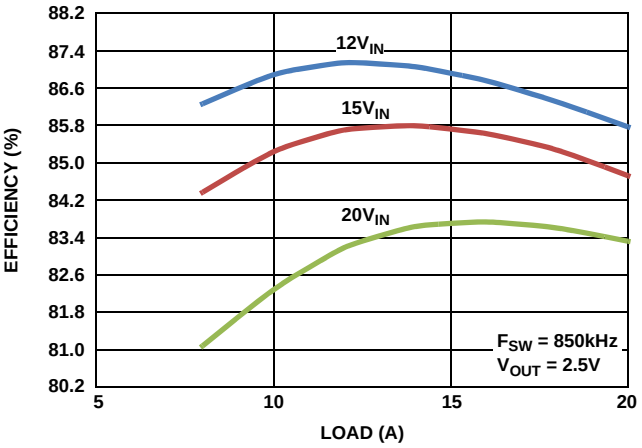

FIGURE 22. EFFICIENCY (F_{SW} = 850kHz, V_{OUT} = 2.5V)

Test Data for ISL8200AMEVAL2PHZ (Continued)

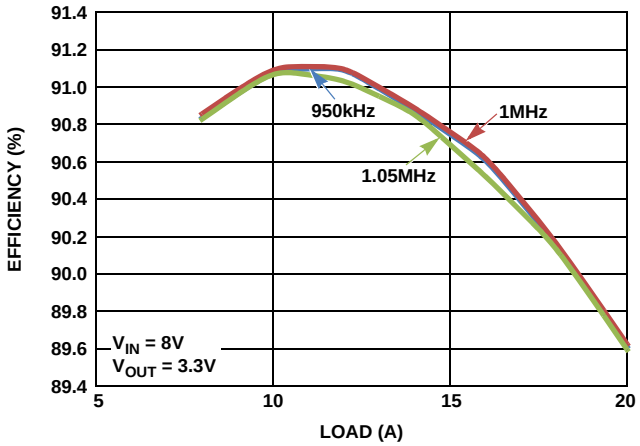

FIGURE 23. EFFICIENCY (V_{IN} = 8V, V_{OUT} = 3.3V)

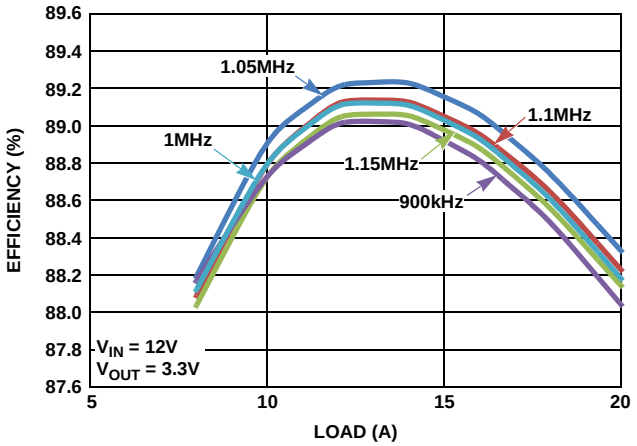

FIGURE 24. EFFICIENCY (V_{IN} = 12V, V_{OUT} = 3.3V)

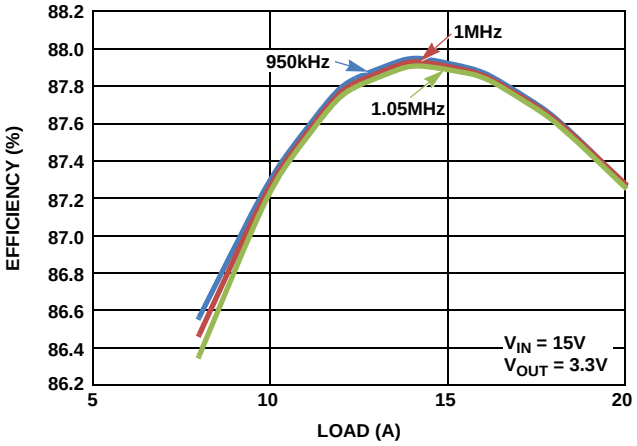

FIGURE 25. EFFICIENCY (V_{IN} = 15V, V_{OUT} = 3.3V)

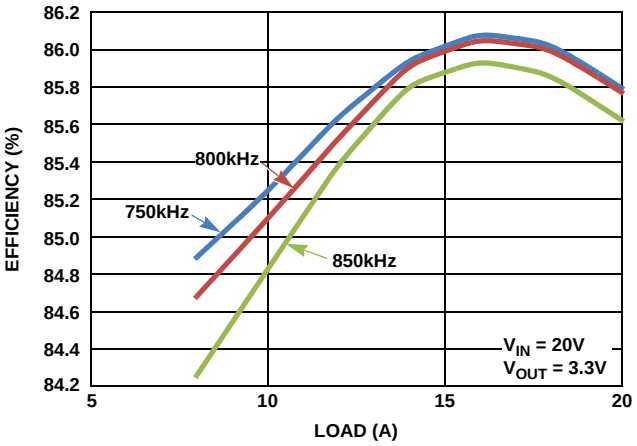

FIGURE 26. EFFICIENCY (V_{IN} = 20V, V_{OUT} = 3.3V)

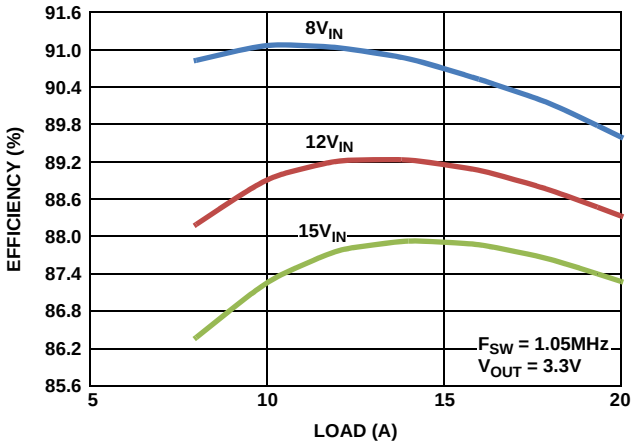

FIGURE 27. EFFICIENCY (F_{SW} = 1.05MHz, V_{OUT} = 3.3V)

Test Data for ISL8200AMEVAL2PHZ (Continued)

Load Regulation

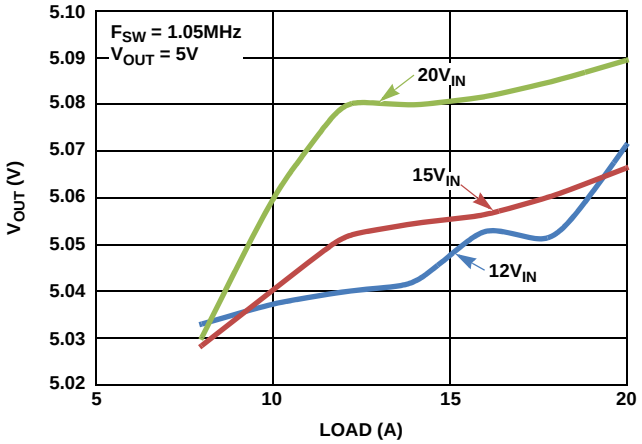

FIGURE 28. LOAD REGULATION (F_{SW} = 1.05MHz, V_{OUT} = 5V)

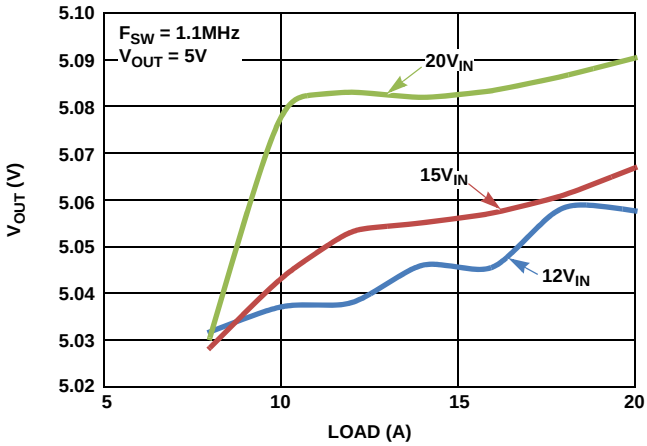

FIGURE 29. LOAD REGULATION (F_{SW} = 1.1MHz, V_{OUT} = 5V)

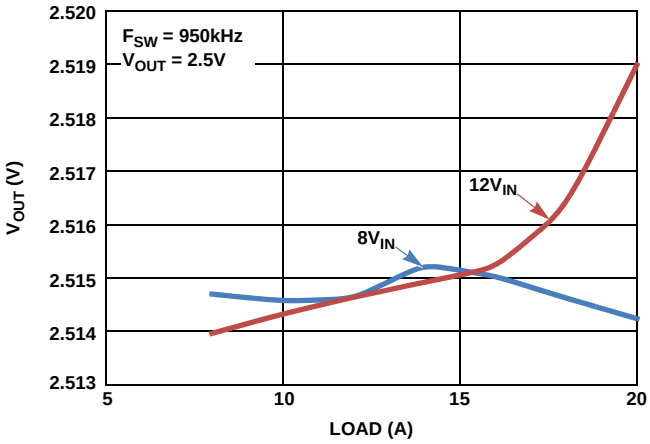

FIGURE 30. LOAD REGULATION (F_{SW} = 950kHz, V_{OUT} = 2.5V)

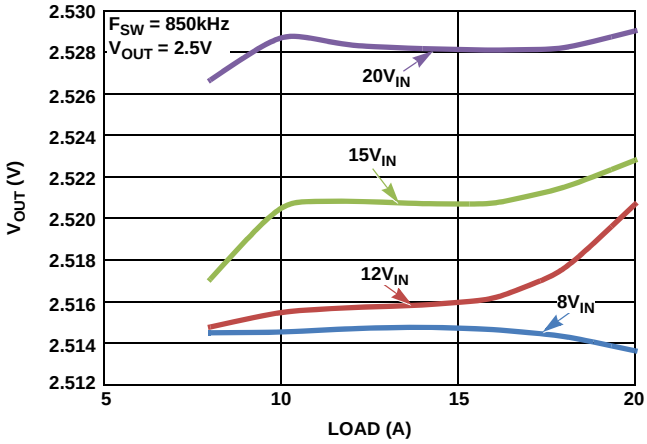

FIGURE 31. LOAD REGULATION (F_{SW} = 850kHz, V_{OUT} = 2.5V)

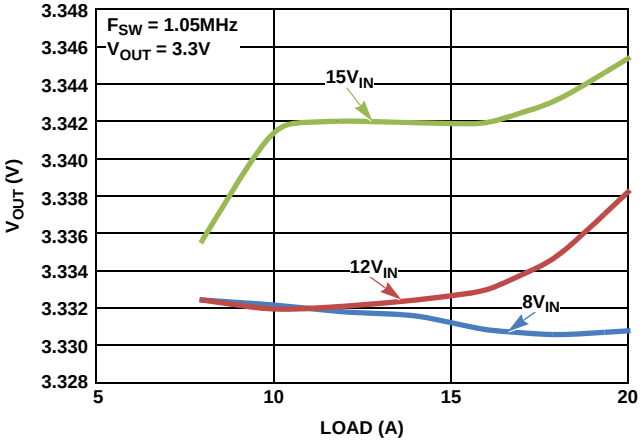

FIGURE 32. LOAD REGULATION (F_{SW} = 1.05MHz, V_{OUT} = 3.3V)

Test Data for ISL8200AMEVAL2PHZ (Continued)

1V Waveforms

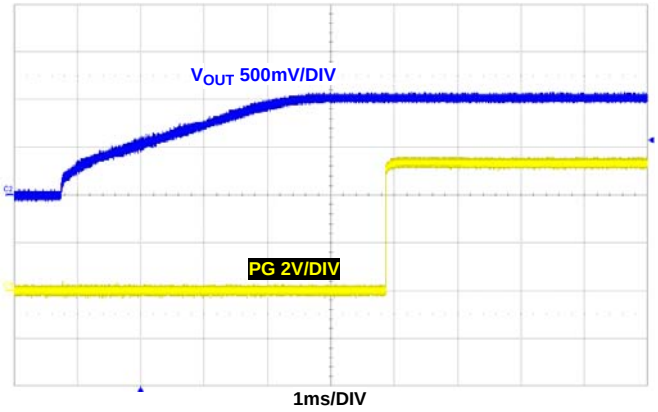

FIGURE 33. START-UP AT NO LOAD, V_{IN} = 12V, V_{OUT} = 1V

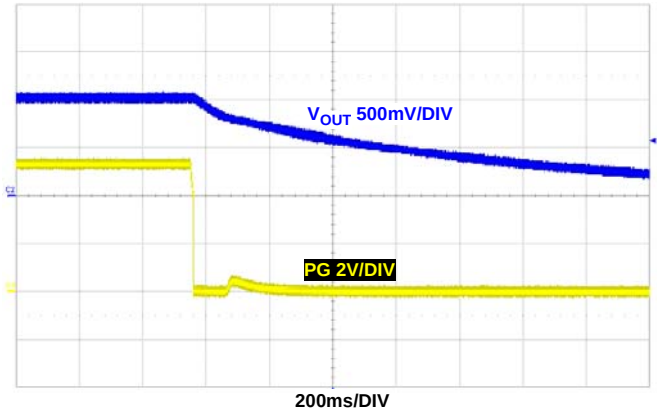

FIGURE 34. SHUTDOWN AT NO LOAD

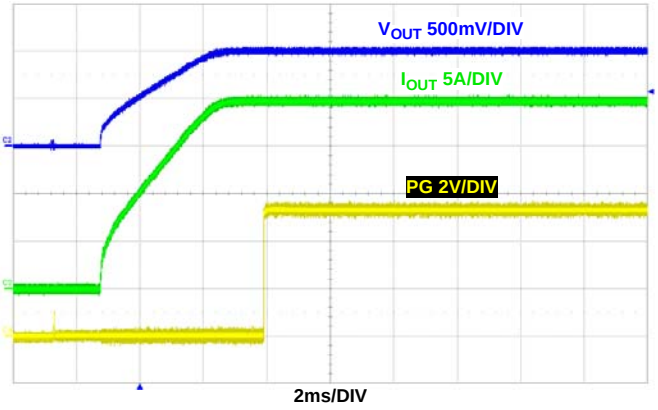

FIGURE 35. START-UP AT 20A LOAD

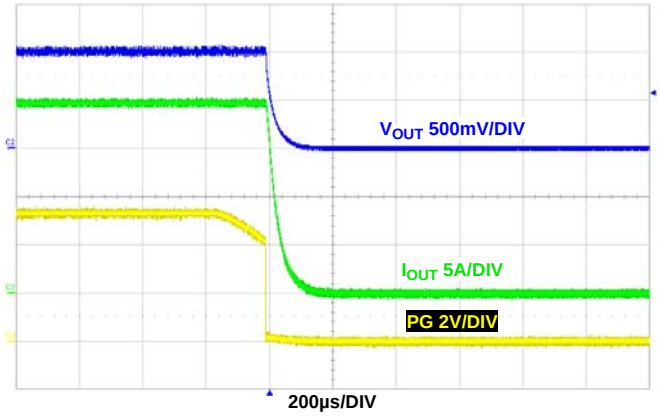

FIGURE 36. SHUTDOWN AT NO LOAD

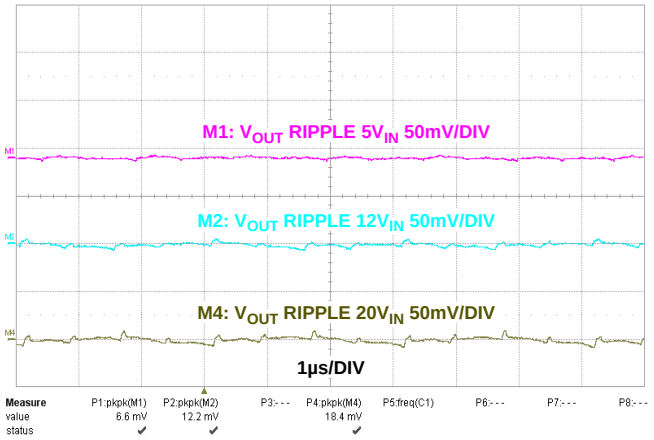

FIGURE 37. STEADY STATE NO LOAD

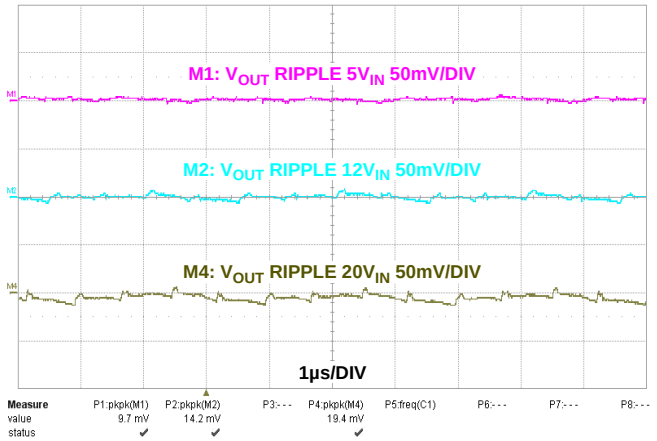

FIGURE 38. STEADY STATE AT FULL LOAD

Test Data for ISL8200AMEVAL2PHZ (Continued)

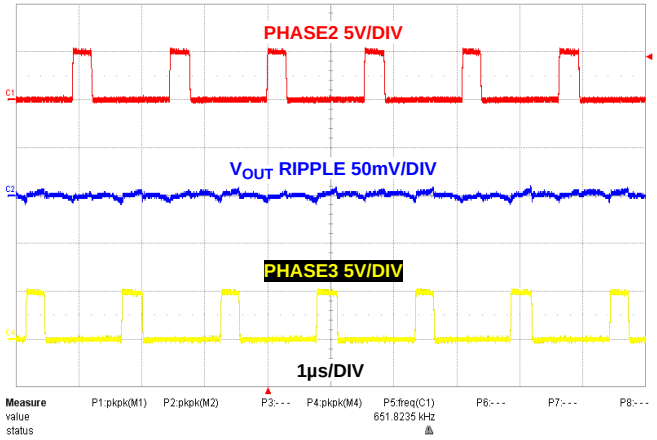

FIGURE 39. STEADY STATE AT NO LOAD, V_{IN} = 5V

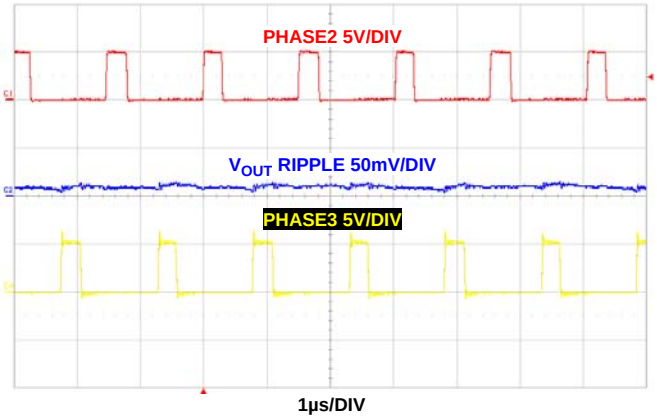

FIGURE 40. STEADY STATE AT 20A LOAD, V_{IN} = 5V

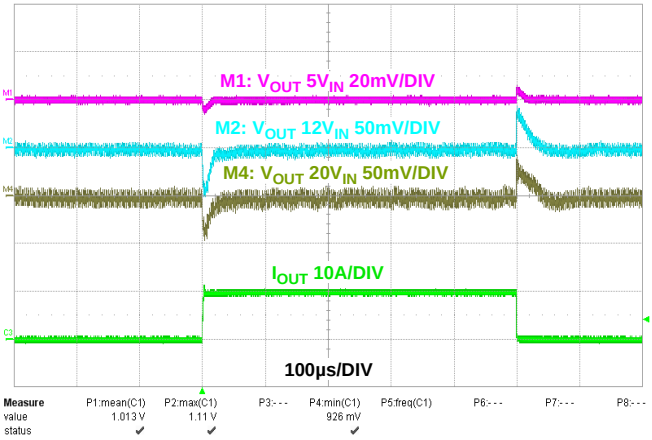

FIGURE 41. LOAD TRANSIENT

5V Waveforms

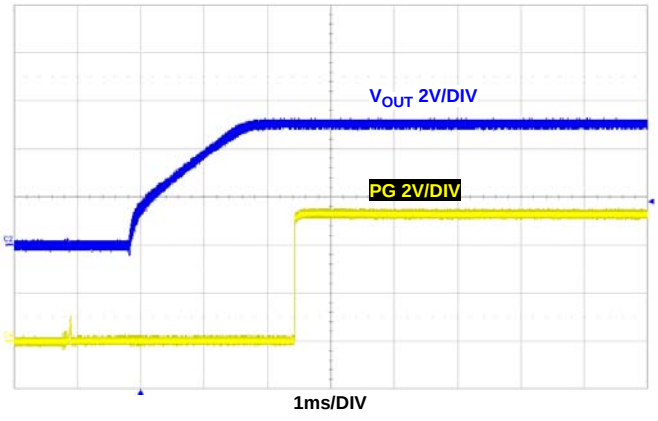

FIGURE 42. START-UP AT NO LOAD, V_{IN} = 12V, V_{OUT} = 5V

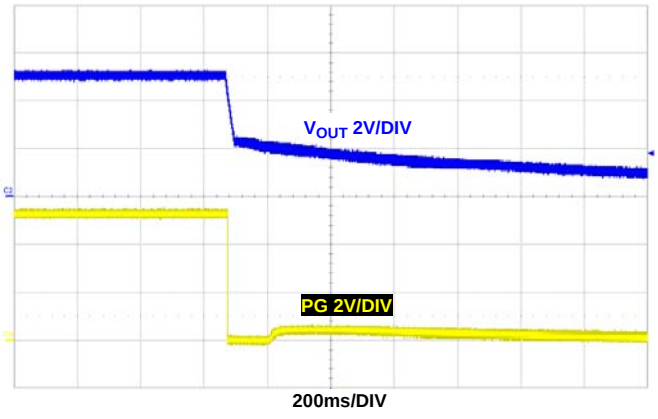

FIGURE 43. SHUTDOWN AT NO LOAD, V_{IN} = 12V, V_{OUT} = 5V

Test Data for ISL8200AMEVAL2PHZ (Continued)

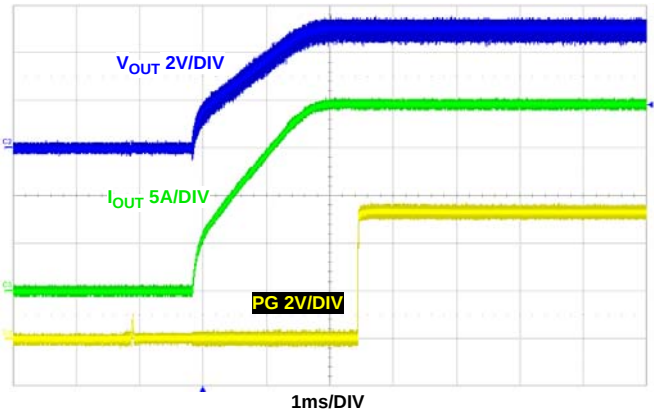

FIGURE 44. START-UP AT 20A LOAD, V_{IN} = 12V, V_{OUT} = 5V

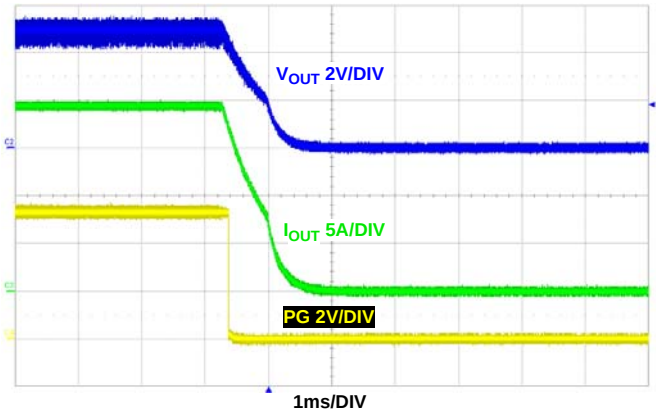

FIGURE 45. SHUTDOWN AT 20A LOAD, V_{IN} = 12V, V_{OUT} = 5V

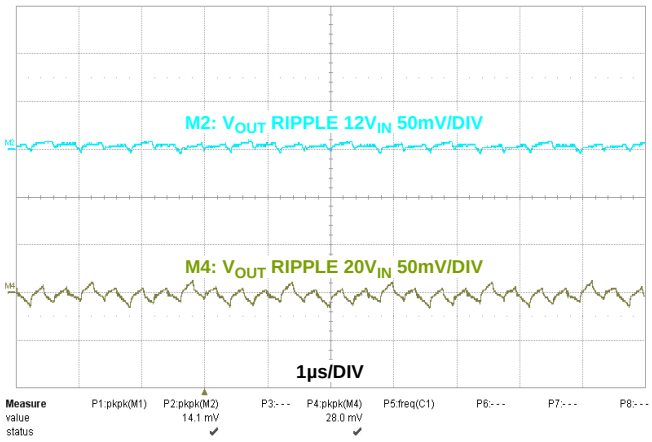

FIGURE 46. STEADY STATE NO LOAD, $5V_{OUT}$

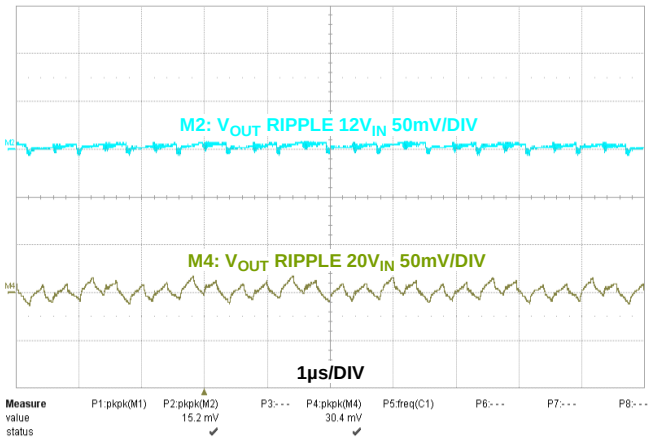

FIGURE 47. STEADY STATE AT FULL LOAD, $5V_{OUT}$

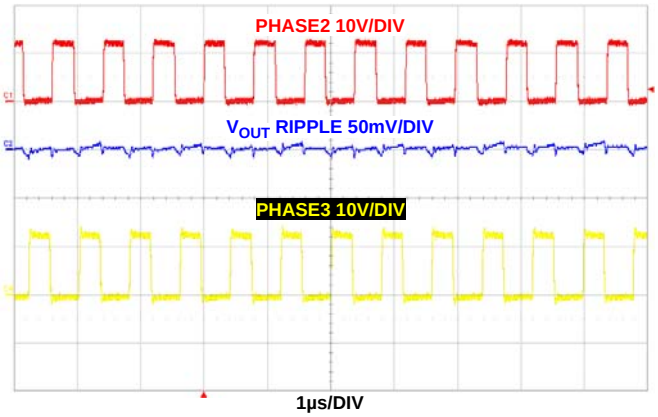

FIGURE 48. STEADY STATE AT NO LOAD, $12V_{IN}$, $5V_{OUT}$

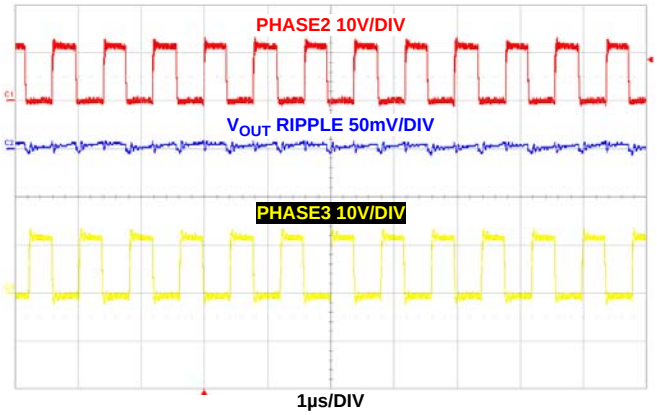

FIGURE 49. STEADY STATE AT FULL LOAD, $12V_{IN}$, $5V_{OUT}$