ISL97694AIRT-EVZ Evaluation Board User Guide

The ISL97694A is Intersil's highly integrated 6-channel LED driver for display backlighting. This part maximizes battery life by featuring only 1mA quiescent current and by operating down to 2.4V input voltage, with no need for higher voltage supplies. The ISL97694A provides 8-, 10- or 12-bit PWM dimming with adjustable dimming frequency up to 30kHz, 7.5kHz, or 1.875kHz, respectively, controlled with I^2C or PWM input.

Start Guide for I^2C Interface

If using the I^2C interface, please follow these instructions and see Figures 1, 2 and 7:

1. Please download from http://www.intersil.com/en/products/audiovideo/display-ics/led-backlight-drivers/ISL97694A.html and install interface software onto the computer from the Intersil web site.
2. Run the I^2C interface software. On Windows operating systems, this is usually found through the Start menu under Intersil → ISL97694A HID → ISL97694A Evaluation Software.
3. Once the application window (see Figure 1) appears, click the green "Connect" button then click the "Read All" button beside it. The control fields should be updated with values read from the ISL97694A unit. If an error occurs, confirm the setup and click "Read All" again.
4. From the power supply, connect the positive terminal from the power supply to the VIN and the negative terminal of the power supply to PGND on the eval board. A voltmeter can be used to sense the voltage at the pin VIN on the eval board in Figure 2.
5. The switch on the evaluation board allows the user to enable or disable the part. To enable the ISL97694A, move the SW_EN switch to "H" and to disable it, move it to the "L" position.
6. Once the power supplies are hooked up to the ISL97694A eval board and the USB cable is connected to the I^2C interface board, turn on the power supply.
7. Go to "ISL97694A Evaluation Software", click on "READ ALL REGISTERS". The brightness bits (BRT11 to BRT0) are all green and have "1" as the default value in the box. The brightness control registers are 0x00 for 8-bit and 0x02 for 12-bit resolution. The default brightness resolution is 8-bit. All of the bits in the Device Control register 0x01 should be low as default.
8. Since the brightness is set to 8 bits by default, the register "BRT_LSB @ reg addr 0x02" does not affect the brightness when the 8-bit option is being used.
9. To turn on the LEDs, select "BL_CTL" to "1" under the register "DEVCTL @ reg addr 0x01" and select "WRITE" on the right hand side. To enable phase shift, select "PS_EN" to "1". (The "PS_EN" is the "Phase Shift" option for the ISL97694A.)
10. To control the LED current, a potentiometer is placed between ISET and GND. Please see ISL97694A datasheet on how to set the LED string current.
11. To reduce the brightness, select the bit code under "BRT_MSB @ reg addr 0x00" and click "WRITE".
12. To enable more brightness bits, select "EN10BIT" or "EN12BIT" under the register "DEVCTL @ reg addr 0x01". If "EN10BIT" is selected, "BRT3" and "BRT2" under the register "BRT_LSB @ reg addr 0x02" is included in the brightness control. If "EN12BIT" is selected, "BRT3", "BRT2", "BRT1" and "BRT0" under the register "BRT_LSB @ reg addr 0x02" is included in the brightness control.
13. To adjust the dimming frequency to the LED strings, a 2kΩ resistor in series with the potentiometer FPWM_R is placed on the ISL97694AIRT-EVZ evaluation board. Adjust the potentiometer for desirable dimming frequency. Please refer to Equations 1, 2 and 3 for 8-bit, 10-bit and 12-bit dimming frequency (f_{PWM}) setting. ISL97694A is defaulted to 8-Bit for PWM Max Dimming Frequency. Please see Table 1 in the ISL97694A datasheet.

$$R_{FPWM} = \frac{58.1 \times 10^6}{f_{PWM}} \quad \text{(EQ. 1)}$$

$$R_{FPWM} = \frac{14.5 \times 10^6}{f_{PWM}} \quad \text{(EQ. 2)}$$

$$R_{FPWM} = \frac{3.63 \times 10^6}{f_{PWM}} \quad \text{(EQ. 3)}$$

14. To adjust switching frequency of the boost, a 27kΩ resistor in series with potentiometer FSW_R is placed on the eval board. Please adjust the switching frequency with potentiometer to optimize the inductor ripple current and the efficiency in each load condition.

References

ISL97694A Datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL97694AIRT-EVZ	ISL97694AIRT-EVZ Evaluation Board

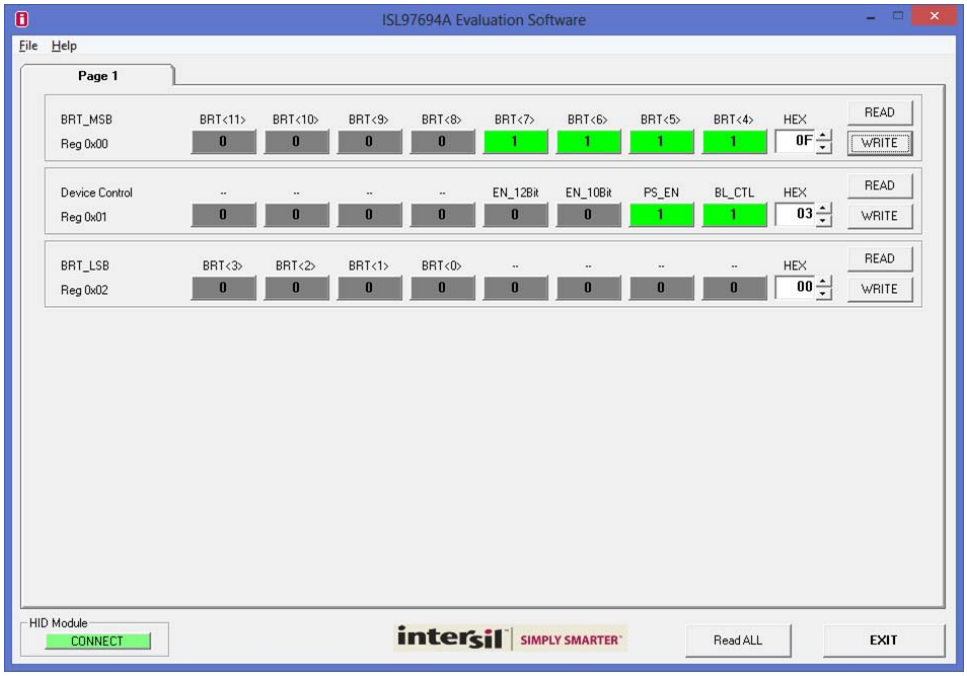

FIGURE 1. ISL97694AIRT-EVZ INTERFACE SOFTWARE

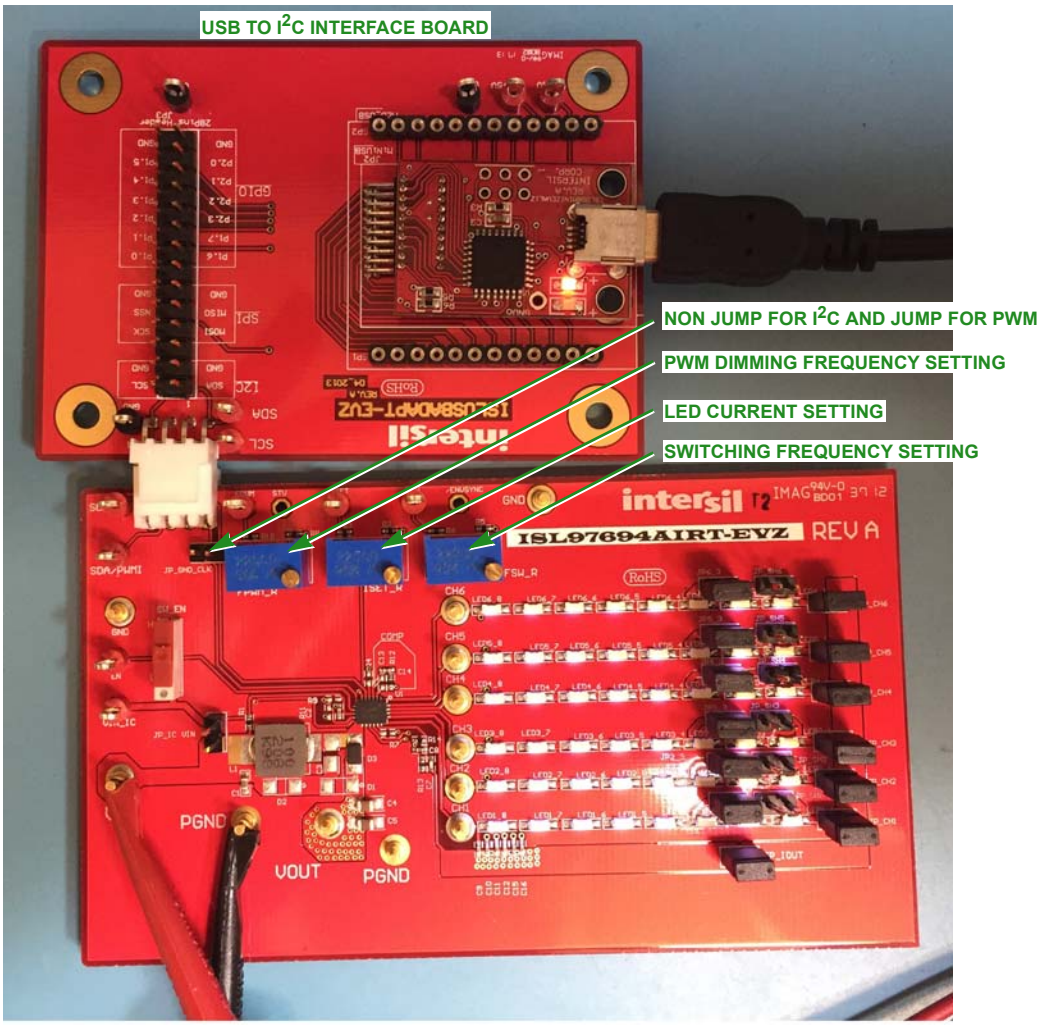

FIGURE 2. PICTURE OF ISL97694AIRT-EVZ EVALUATION BOARD. PICTURE OF ISL97694AIRT-EVZ AND ISLUSBADAPT-EVZ

Start Guide for PWM Interface

The ISL97694A supports the PWM interface and these instructions should be followed for setup:

1. From the power supply, connect the positive terminal from the power supply to the VIN and the negative terminal of the power supply to PGND on the eval board. A voltmeter can be used to sense the voltage at the pin VIN on the evaluation board in Figure 2.
2. In order to select the PWM interface option, please Jump JP_GND_CLK pin to be GND. The PWM signal should be applied to the SDA/PWMI pin for brightness control. When using the PWMI pin to dim, there are two options on how the LEDs are dimmed:
   - Encoded PWM dimming: The incoming PWM provides only dimming duty cycle information and the frequency is not directly applied to the LED strings. Phase shift is enabled with this option. To adjust the dimming frequency, use a potentiometer FPWM_R. Please refer to the ISL97694A datasheet for more details on phase shift.
   - Direct PWM dimming: The second option is to apply a direct PWM signal to the SDA/PWMI pin so the LEDs follow the PWMI frequency and pulse width input signal from a function generator. To do this, connect the FPWM pin to the VIN pin. With this option, phase shift is disabled.
3. Boost Switching Frequency Adjustment: Currently the evaluation board has the potentiometer FSW_R for the boost switching frequency adjustment.
4. Dimming Frequency Adjustment: Use the potentiometer FPWM_R for the dimming frequency adjustment.
5. LED Peak Current Adjustment: Adjust the LED peak current with change to the resistance of the potentiometers, ISET_R.
6. OVP Threshold Setting: The OVP level can be set based on Equation 4. The boost can regulate down to 30% of OVP. The OVP level should be considered max forward voltage of strings and margin of low temperature start-up.

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 4)}$$

Please refer to the ISL97694A datasheet for detailed switching and regulation adjustment.

LED Current Setting and Analog Dimming

The max LED current is set by using a resistor on the ISET pin. This resistor R_{SET} is calculated per Equation 5:

$$I_{LEDmax} = \frac{1066}{R_{SET}} \quad \text{(EQ. 5)}$$

- R_{ISET}: Resistance from ISET pin to GND (Ohm)
- I_{LEDmax}: Peak current set by resistor R_{SET} (A)

For example, if the required max LED current (I_{LEDmax}) is 20mA, then the R_{SET} value needed is:

R_{SET} = 1066/0.02 = 53.3kΩ

Choose nearest standard resistor: 53.3kΩ, 0.1%

Using the above concept, DC dimming (also called analog dimming) can be done by applying a DC voltage VDIM to the ISET pin via a resistor as shown in Figure 3.

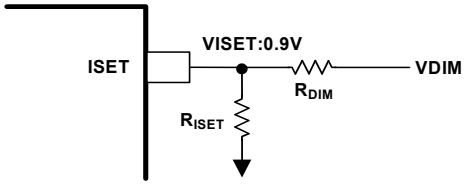

FIGURE 3. ANALOG DIMMING CONFIGURATION

If the VDIM is above VISET = 0.9V, the brightness will reduce and vice versa.

**Note: The LED driver calibrates itself in start-up, so it is important that the control voltage be set to the maximum brightness level when the ISL97694A is enabled, even if the LEDs are not lit at this point.

**Note: To configure analog dimming, pull down the SCL pin to GND and pull up the FPWM pin to VIN. This needs to be done prior to applying VIN to the IC.

How to Set Up the ISL97694A to Run 2-Cell Battery in Series

1. It is important that VIN stay below the absolute rating of 5.5V (see Figure 4).
2. Remove the jumper on JP_IC_VIN on the left of inductor and open R_1 resistor.
3. Using two power supplies, connect one of the power supply positive terminals to VIN and the negative terminal to PGND and the second power supply positive terminal to the pin VIN_IC and the negative supply to AGND.
4. Remember that the IC can be damaged if VIN_IC > 5.5V.
5. With this configuration, the first power supply that is connected to the VIN can go above 5.5V and is capable of running a 2S battery configuration.

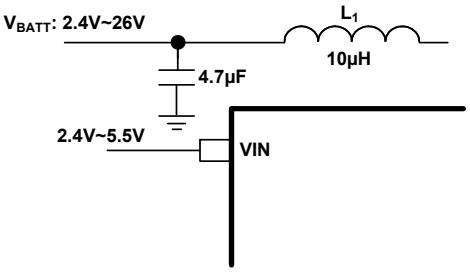

FIGURE 4. 2-CELL BATTERY SUPPLY CONFIGURATION

Configuration and Operation of the Charge Pump

The ISL97694AIRT-EVZ evaluation board can be optionally configured with the charge pump to run 8 LEDs. The typical output voltage of the 8 LEDs will be about 26V and absolute maximum rating of ISL97694A is 28V. In the worst case of LEDs forward mismatch and lower temperature start-up condition, a certain amount of transient voltage possibly applied to the LX node and damaging the boost FET. The charge pump can be configured as shown in the evaluation board schematic in Figure 7 with populating diodes D_1, D_2 and capacitor C_3 and removing diode D_3. This configuration of the charge pump circuit always disables the boost FET to see higher voltage than V_{OUT} - V_{IN}.

The configured charge pump will work as follows and refer to the circuit diagram in Figure 5.

a) When the FET is ON, there are two current paths that sum to the LX node. One path is through the inductor and the other path is through D_1 Schottky diode and C_C capacitor. A voltage VC across to the C_C is V_{IN}-Vd and inductor voltage VL will be V_{IN}.

b) When the FET is OFF, LX goes high and generates an output voltage V_{OUT} equal to V_{IN}-2Vd+1/(1-D)*V_{IN}.

c) Therefore, the LX node will see V_{OUT}-V_{IN}-2Vd so it will be safe even with 8 LEDs driving with V_{OUT}: 26V.

d) The charge pump configured circuit limits V_{IN} to be lower than $V_{OUT}/2$ because the charge pump itself will step up about 2 times of V_{IN}. The boost converter will not have any headroom to control if V_{IN} is higher than $V_{OUT}/2$.

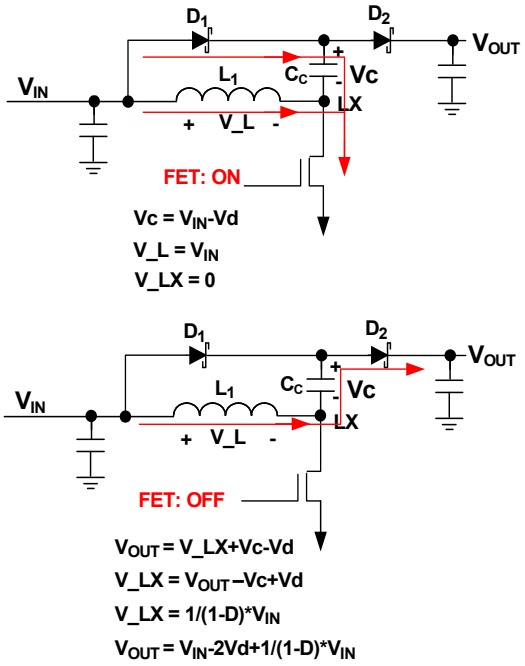

FIGURE 5. CHARGE PUMP OPERATION

PCB Layout with TQFN Package

Great care is needed in designing a PC board for stable ISL97694A operation. As shown in Figure 7, the separation of PGND and AGND is essential, keeping the AGND referenced only local to the chip. This minimizes switching noise injection to the feedback sensing and analog areas, as well as eliminating DC errors form high current flow in resistive PC board traces. PGND and AGND should be on the top and bottom layers, respectively, in the two layers of the PCB. A star ground connection should be formed by connecting the LED ground return and AGND pins to the thermal pad with vias. The ground connection should be into this ground net, on the top plane. The bottom plane then forms a quiet analog ground area that both shields components on the top plane, as well as providing easy access to all sensitive components. For example, the ground side of the FSW and I_{SET} resistor can be dropped to the bottom plane, providing a very low impedance path back to the AGND pin, which does not have any circulating high currents to interfere with it. The bottom plane can also be used as a thermal ground, so the AGND area should be sized sufficiently large to dissipate the required power. For multilayer boards, the AGND plane can be the second layer. This provides easy access to the AGND net, but allows a larger thermal ground and main ground supply to come up through the thermal vias from a lower plane.

Figures 8 and 9 show the evaluation board PCB layout example of the ISL97694A. This type of layout is particularly important for this type of product, resulting in high current flow in the main loops traces. Careful attention should be focused in the following layout details:

1. Boost input capacitors, output capacitors, inductor and Schottky diode should be placed together in a nice tight layout. Keeping the grounds of the input and output connected with low impedance and wide metal, is very important to keep these nodes closely coupled.
2. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close to the VIN pin.
3. For optimum load regulation and true VOUT sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection then needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation.
4. The COMP network and the rest of the analog components (on ISET, FPWM, FSW, etc.) should be referenced to AGND.
5. The heat of the chip is mainly dissipated through the exposed thermal pad, so maximizing the copper area around it is a good idea. A solid ground is always helpful for the thermal and EMI performance.

The inductor and input and output capacitors should be mounted as tight as possible, to reduce the audible noise and inductive ringing.

General Power PAD Design Considerations

Figure 6 shows an example of how to use vias to remove heat from the IC. We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad footprint with vias spaced such that the center-to-center spacing is three times the radius of the via. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

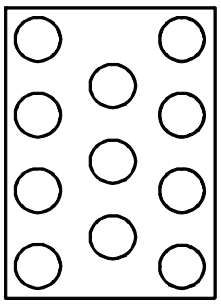

FIGURE 6. EXAMPLE OF POWER PAD

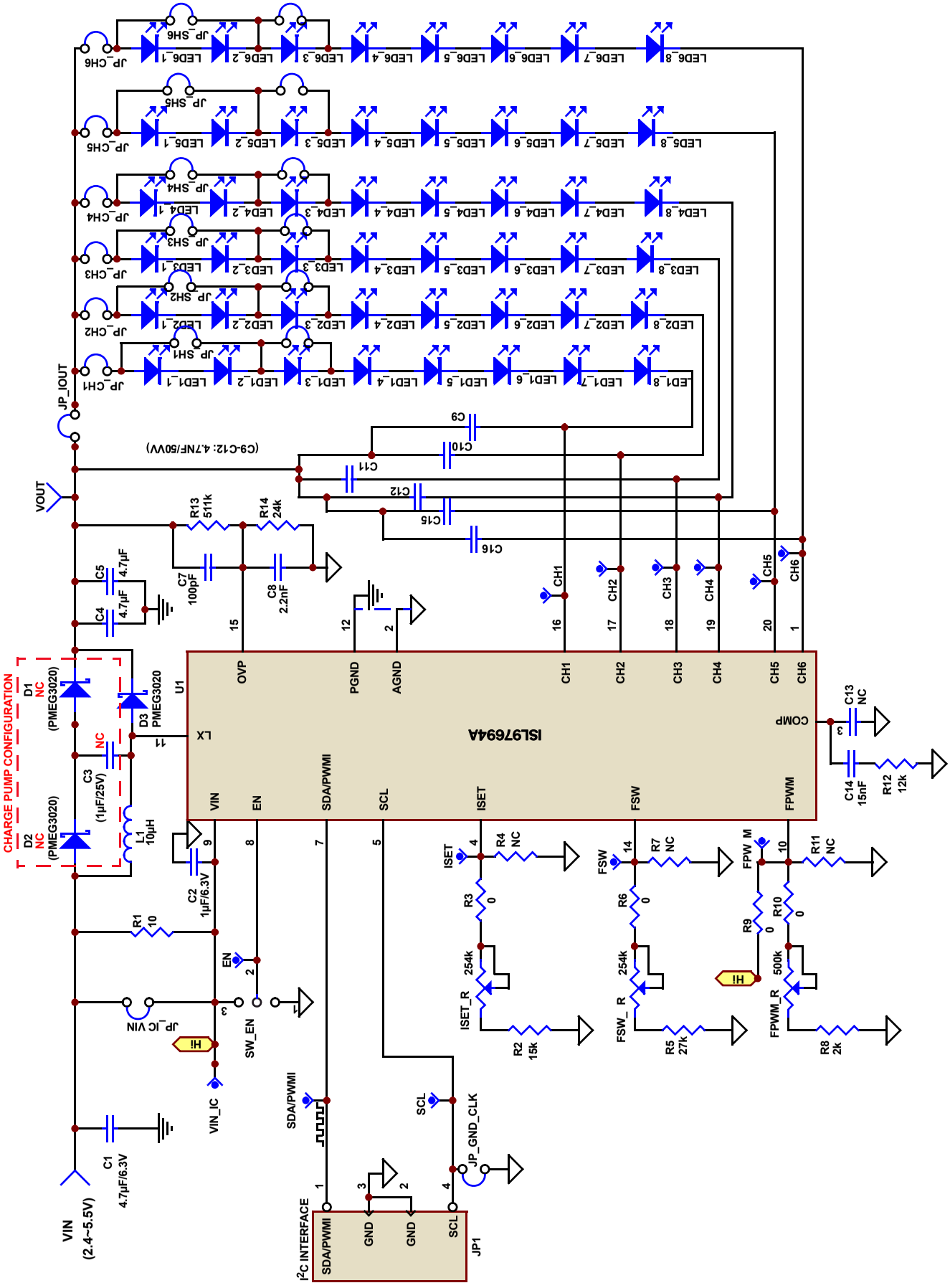

FIGURE 7. SCHEMATIC OF ISL97694A EVALUATION BOARD

ISL97694AIRT-EVZ Evaluation Board Layout

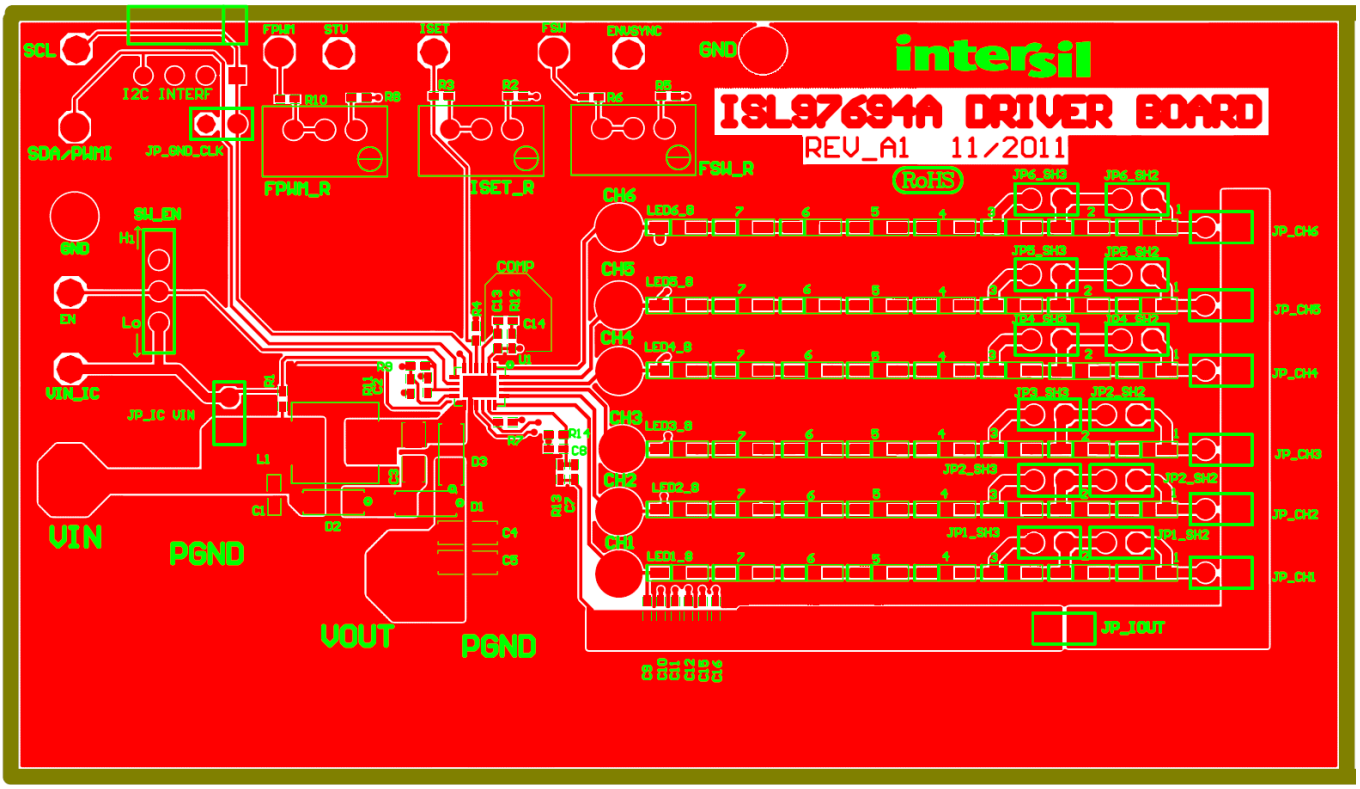

FIGURE 8. PCB LAYOUT (TOP LAYER) OF ISL97694A EVALUATION BOARD

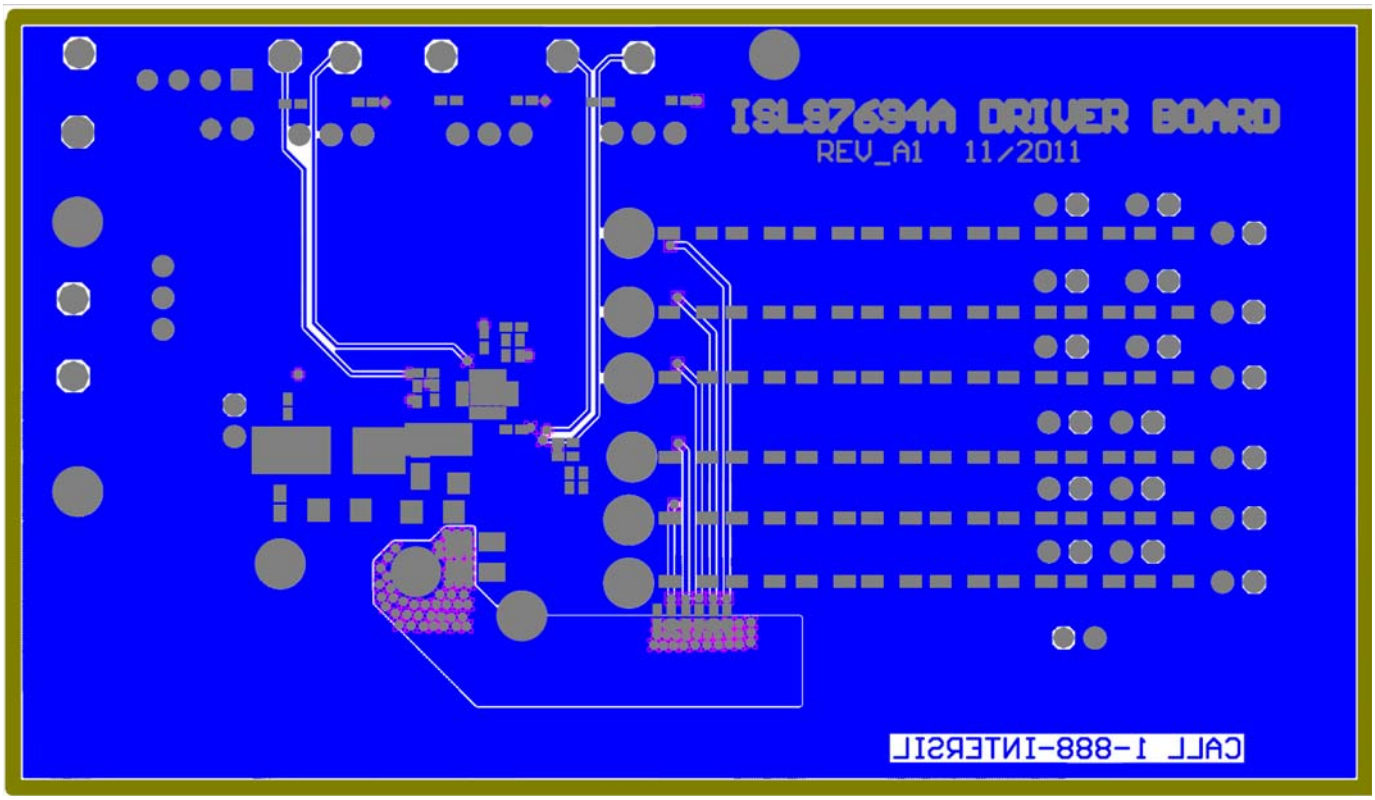

FIGURE 9. PCB LAYOUT (BOTTOM LAYER) OF ISL97694A EVALUATION BOARD

Bill of Materials for ISL97694A Evaluation Board

PART TYPE	DESIGNATOR	FOOTPRINT
0Ω	R3, R6, R9, R10	402
1µF/6.3V	C2	402
2.2nF	C8	402
4.7nF	C9, C10, C11	402
4.7nF	C12, C15, C16	402
4.7µF	C4, C5	805
4.7µF/6.3V	C1	603
10Ω	R1	402
12kΩ	R12	402
15kΩ	R2	402
15nF	C14	402
10µH	L1	Refer to PIMB061H-100MS datasheet
24kΩ	R14	402
27kΩ	R5	402
2kΩ	R8	402
100pF	C7	402
500kΩ	FPWM_R	POT
254kΩ	ISET_R, FSW_R	POT
511kΩ	R13	402
LED-SMT	All LEDS	Refer to LW_Y87C datasheet
PMEG3020	D3	Refer to SOD-123W datasheet
ISL97694AIRT-EVZ	U1	Refer to LPP20.3X4 datasheet