

RTKA2109252H00000BU

User's Manual: Evaluation Board

Industrial Analog and Power

## 1. Overview

The [RAA210925](#) is a pin-strap configurable dual 25A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally-enhanced HDA packaging technology, the module can deliver up to 25A of continuous output current without the need for airflow or additional heat sinking. The RAA210925 simplifies configuration and control of Renesas [digital power technology](#) while offering an upgrade path to full PMBus configuration through the pin-compatible ISL8274M.

The RAA210925 comes with a preprogrammed configuration for operating in Pin-strap mode. A standard PMBus interface addresses fault management, real-time full telemetry, and point-of-load monitoring.

The RAA210925 uses ChargeMode™ control architecture, which responds to a transient load within a single switching cycle. Operating across an input voltage range from 4.5V to 14V, the RAA210925 offers adjustable output voltage from 0.6V to 5V.

The RTKA2109252H00000BU evaluation board is a 4.0in x 4.5in 8-layer FR4 board with 2oz. copper on top and bottom layer and 1oz. copper in buried layers. This evaluation board comes with a placeholder for pin-strap resistors to adjust output voltage, switching frequency, input Undervoltage Lockout (UVLO) protection threshold, device PMBus address, overcurrent limit, ASCR setting, and soft start setting. More configurations can be easily programmed or changed using a PMBus compliant serial bus interface.

The ZLUSBEVAL3Z (USB to PMBus adapter) is provided with this evaluation board, which connects the evaluation board to a PC to activate the PMBus communication interface. The PMBus command set is accessed by using the [PowerNavigator™](#) evaluation software from a PC running Microsoft Windows. The RTKA2109252H00000BU can operate in Pin-Strap mode without needing the ZLUSBEVAL3Z adapter or PMBus communication.

### 1.1 Key Features

- $V_{IN}$  range of 4.5V to 14V,  $V_{OUT}$  adjustable from 0.6V to 5V. Up to 95.5% efficiency
- Pin-strap mode for standard settings:  $V_{OUT}$ , switching frequency, ASCR setting, input UVLO, soft-start/stop, tracking, and external synchronization
- Real time telemetry for  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{OUT}$ , temperature, duty cycle, and switching frequency and fault logging
- ChargeMode™ control that is tunable with pin-strap resistors or the PMBus interface
- Mechanical switch for enable and the power-good LED indicator

### 1.2 Specifications

This board is configured and optimized for the following operating conditions:

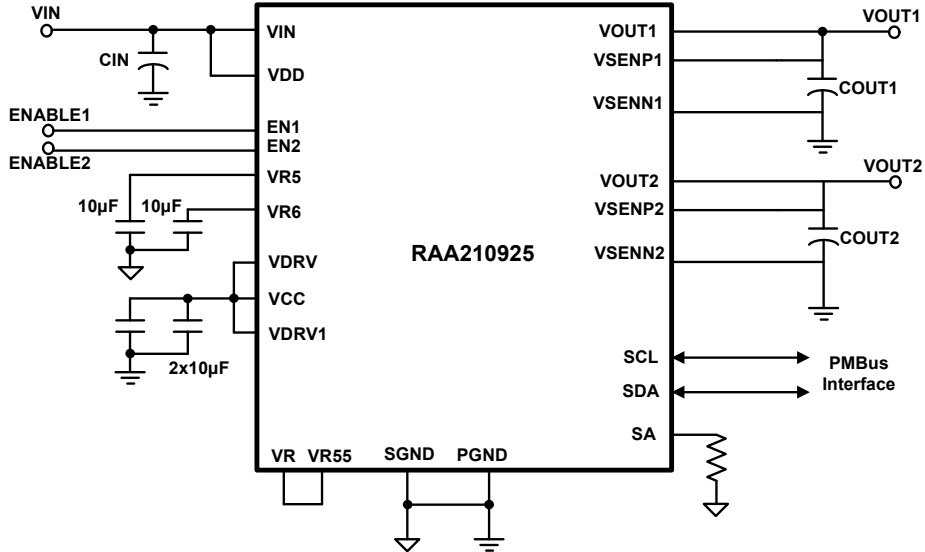
- $V_{IN}$  = 5V to 12V
- $V_{OUT}$  = 1.5V
- $I_{MAX}$  = 25A per channel,  $I_{OUT\_avg\_OCP}$  = 35A per channel
- $f_{SW}$  = 889kHz
- ASCR gain = 525, ASCR residual = 90
- On/off delay = 5ms (Ch1), 5ms (Ch2), on/off ramp time = 2ms (Ch1), 5ms (Ch2)
- Input UVLO = 4.5V
- PMBus address = 0x28h

### 1.3 Ordering Information

Part Number	Description
RTKA2109252H00000BU	RTKA2109252H00000BU evaluation board (ZLUSBEVAL3Z adapter and USB cable included)

### 1.4 Related Literature

- For a full list of related documents, visit our website
- [RAA210925](#) product page



Note: This figure represents a typical implementation of the RAA210925. For PMBus operation, Renesas recommends tying the enable pin (EN) to SGND.

Figure 1. RTKA2109252H00000BU Block Diagram

## 2. Functional Description

The RTKA2109252H00000BU provides all circuitry required to evaluate the features of the RAA210925. A majority of the features of the RAA210925, such as compensation-free ChargeMode control, soft-start delay, and ramp times are available on this evaluation board.

### 2.1 Recommended Equipment

- DC power supply with minimum 15V/40A sourcing capacity
- Electronic load capable of sinking current up to 25A per channel
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

### 2.2 Quick Start Guide

#### 2.2.1 Pin-Strap Option

The RTKA2109252H00000BU can be configured in Pin-Strap mode with standard 1% resistors. The PMBus interface is not required to evaluate the RAA210925 in Pin-Strap mode. Output voltages ( $V_{OUT}$ ), switching frequency ( $f_{SW}$ ), input Undervoltage Protection (UVLO) threshold, output average overcurrent threshold, tracking mode setting, ASCR setting, output delay/ramp setting, and the device PMBus address can be changed by populating the recommended resistors at placeholders provided in the evaluation board.

By default, the evaluation board is programmed to regulate at the following:

- $V_{OUT} = 1.5V$
- $f_{SW} = 889kHz$
- $UVLO = 4.5V$
- $OCP = 35A$
- Tracking disabled
- $ASCR\_gain = 525$
- $ASCR\_residual = 90$
- On/off delay = 5ms (Ch1), 5ms (Ch2)
- On/off ramp time = 2ms (Ch1), 5ms (Ch2)
- PMBus address = 28h

Complete the following steps to evaluate the RAA210925 in Pin-Strap mode.

- (1) Set the ENABLE switch to “DISABLE” for both channels (SW<sub>1</sub> and SW<sub>2</sub>).
- (2) Connect a load to the VOUT<sub>1/2</sub> banana connectors (VOUT<sub>1</sub>/GND and VOUT<sub>2</sub>/GND).
- (3) Connect a power supply to the VIN connectors (VIN/GND). Make sure the power supply is not enabled when making the connection.
- (4) Adjust the  $V_{IN} = 12V$  and turn the power supply on.
- (5) Set the ENABLE switch to “ENABLE” for both channels (SW<sub>1</sub> and SW<sub>2</sub>).
- (6) Measure 1.5V  $V_{OUT}$  at probe jumpers VOUT<sub>1</sub>/GND (J<sub>11</sub>) and VOUT<sub>2</sub>/GND (J<sub>12</sub>).
- (7) Observe the switching frequency of 889kHz at probe jumpers PHASE1/GND (TP<sub>10</sub>) and PHASE2/GND (TP<sub>11</sub>). The two phases should show 180° phase shift.
- (8) To change the  $V_{OUT}$ , disconnect the board from the setup and populate with a 1% standard 0603 resistor at the RVSET<sub>1/2</sub> placeholder location on the bottom layer. Refer to the “Output Voltage Resistor Settings”

table in the [RAA210925](#) datasheet for recommended values. By default,  $V_{OUT\_MAX}$  is set 110% of  $V_{OUT}$  set by the pin-strap resistor.

- (9) To change the compensation, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the  $R_{14}/R_{37}$  placeholder location on the bottom layer. Refer to the “ASCR Resistor Settings” table in the [RAA210925](#) datasheet for recommended values.
- (10) To change the soft-start/stop and tracking setting, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the  $R_6$  placeholder location on the bottom layer. Refer to the “Soft-Start/Stop and Tracking Resistor Settings” table in the [RAA210925](#) datasheet for recommended values.
- (11) To change the switching frequency and the OCP limit, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the RFSET placeholder location on the bottom layer. Refer to the “Switching Frequency and OCP Limit Resistor Settings” table in the [RAA210925](#) datasheet for recommended values.
- (12) To change the input UVLO and address, disconnect the board from the setup and populate with a 1% standard 0603 resistor at the  $R_4$  placeholder location on the bottom layer. Refer to the “SMBus Address and UVLO Resistor Settings” table in the [RAA210925](#) datasheet for recommended values.

### 2.2.2 PMBus Option

The RTKA2109252H00000BU can be evaluated for all features using the provided ZLUSBEVAL3Z dongle and PowerNavigator evaluation software. PowerNavigator tutorial videos are available on our [website](#). Complete the following steps to evaluate the RAA210925 with the PMBus option.

- (1) Install PowerNavigator.
- (2) Set the ENABLE switch to “DISABLE” for both channels ( $SW_1$  and  $SW_2$ ).
- (3) Connect a load to the  $V_{OUT1/2}$  banana connectors ( $V_{OUT1}/GND$  and  $V_{OUT2}/GND$ ).
- (4) Connect a power supply to the VIN connectors (VIN/GND). Make sure the power supply is not enabled when making the connection.
- (5) Adjust the  $V_{IN} = 12V$  and turn the power supply on.
- (6) Connect the ZLUSBEVAL3Z dongle (USB to PMBus adapter) to the RTKA2109252H00000BU’s 6-pin male connector labeled “PMBus DONGLE IN”.
- (7) Connect the supplied USB cable from the computer through USB to the ZLUSBEVAL3Z dongle.
- (8) Launch PowerNavigator.
- (9) The RAA210925 device on the board operates in Pin-Strap mode from factory default, but the user can modify the operating parameters through PowerNavigator. The default pin-strap configurations are overwritten with PMBus command changes from Power Navigator.
- (10) Set the ENABLE switch to “ENABLE” for both channels ( $SW_1$  and  $SW_2$ ). The PowerNavigator PMBus commands ON\_OFF\_CONFIG and OPERATION can be used to allow PMBus Enable.
- (11) Monitor and configure the RTKA2109252H00000BU using the PMBus commands in PowerNavigator.
- (12) For phase spreading with Interleave or to evaluate multiple digital power products using a single ZLUSBEVAL3Z dongle, the RAA210925 can be daisy chained with other digital power evaluation boards. The PMBus address can be changed by placing a 1% standard 0603 resistor at the  $R_4$  placeholder location on the bottom layer. Refer to the “SMBus Address and UVLO Resistor Settings” table in the [RAA210925](#) datasheet for recommended values.

## 2.3 Operating Range

By default, the RTKA2109252H00000BU is configured to operate at  $V_{OUT} = 1.5V$ ,  $f_{SW} = 889kHz$ .  $V_{IN}$  ranges from 4.5V to 12V. The board can also support a wider operating range to meet the requirements of specific applications.  $V_{OUT}$  can be adjusted from 0.6V to 5V. Load current range per channel is 0A to 25A. Note that airflow across the board may be needed for continuous operation at 25A at elevated ambient temperatures. The  $f_{SW}$  and output voltage can also be tuned.

To ensure sufficient stability margins, switching frequency and output capacitors can only be selected using values in the [RAA210925](#) datasheet. If the input voltage is less than 5.3V, tie the VCC test point directly to VIN or to a separate 5V power supply for optimal operation and efficiency. If external synchronization is used, connect the SYNC test point to the external clock. The external clock signal should be active before the module is enabled.

### 3. Evaluation Board Information

If the input voltage is less than 5.3V, tie the  $V_{CC}$  test point directly to VIN or to a separate 5V power supply for best efficiency. If external synchronization is used, connect the SYNC test point to the external clock. Note that the external clock signal should be active before the module is enabled.

#### 3.1 $V_{OUT}$ Transient Response Check

The RTKA2109252H00000BU board has a built-in transient load test circuit (see the schematic in [Figure 2](#)). A 100A N-Channel MOSFET (Manufacturer PN: BSC010NE2LSI) is connected across  $V_{OUT}$  and PGND. A 10m $\Omega$  current-sense resistor ( $R_{24}/R_{54}$ ) monitors the drain-to-source current of the MOSFET. For a transient load test, inject the gate drive pulse signal at  $J_4/J_{16}$ . The load current can be monitored through  $J_3/J_{15}$ . Because the MOSFET operates in the saturation region instead of the linear region when the gate turn-on signal is applied, the pulse width and duty cycle of the gate signal must be limited enough to avoid MOSFET overheating (the recommended duty cycle should be less than 2%). The amplitude of the gate driver pulse voltage can be adjusted to obtain a desired transient load current step size.

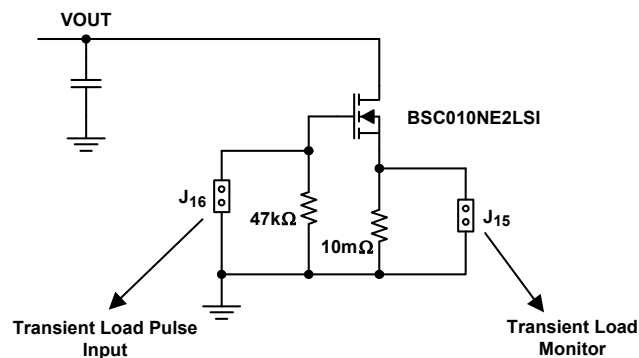


Figure 2. Schematic for Transient Load Measurement

#### 3.2 External Clock Synchronization

The RAA210925 can synchronize to an external clock. External clock synchronization allows the user to operate multiple converters at the same switching frequency and can lead to improved EMI characteristics. The RTKA2109252H00000BU evaluation board can be used to assess this functionality. A function generator is required. Complete the following steps to operate the RAA210925 with an external clock frequency of 593kHz:

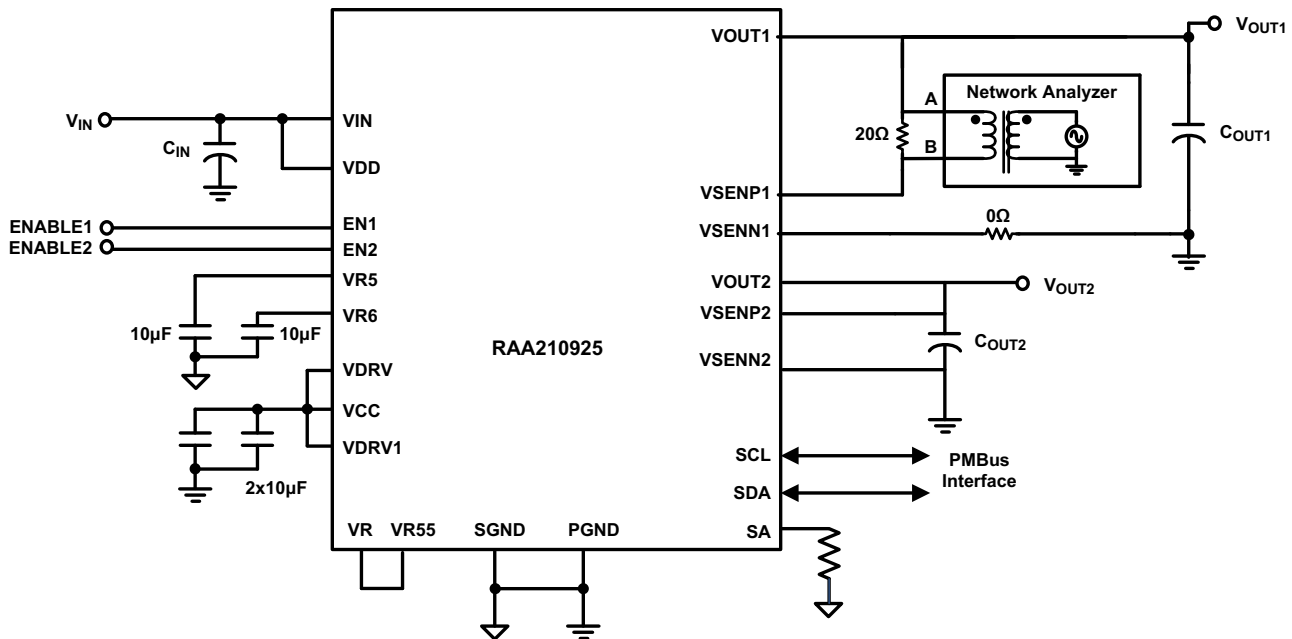
- (1) Set the Enable switch to the “DISABLE” position.
- (2) Solder a 17.8k $\Omega$  resistor at RSET on the CFG pin ( $R_5$ ).
- (3) Program the function generator to output a continuous square pulse waveform of 593kHz. Program the pulse width to be at least 150ns.
- (4) Ensure that the clock signal is stable by monitoring the waveform on an oscilloscope.
- (5) After verifying clock stability, connect the output cables from the function generator to test point TP<sub>3</sub> (labeled “SYNC\_OCP/GND”).
- (6) Turn the function generator output to “ON”.
- (7) Enable the module by setting the Enable switch to the “ENABLE” position.
- (8) Observe the switching frequency at test points TP<sub>10</sub> and TP<sub>11</sub> (labeled “PHASE1” and “PHASE2”, respectively).
- (9) The module synchronizes to the 593kHz external clock from the function generator.
- (10) Always ensure that the module is disabled before changing the frequency of the external clock.
- (11) A Loss of Sync fault is generated when the external clock is lost.

### 3.3 Bode Plot Measurements

Assessing the stability of the converter is an important step in the design process. Bode plots are a useful and reliable tool to identify the converter's loop response. Phase and gain margins give an insight into the stability of the system, and bandwidth can indicate how quickly the converter responds to disturbances in input voltage or load transients. Correctly measuring the loop response is critical for designing stable converter systems.

A network analyzer is required to perform the frequency response measurements on the RTKA2109252H00000BU evaluation board. Complete the following steps to evaluate the loop response for Channel 1 of the RAA210925 on the RTKA2109252H00000BU evaluation board.

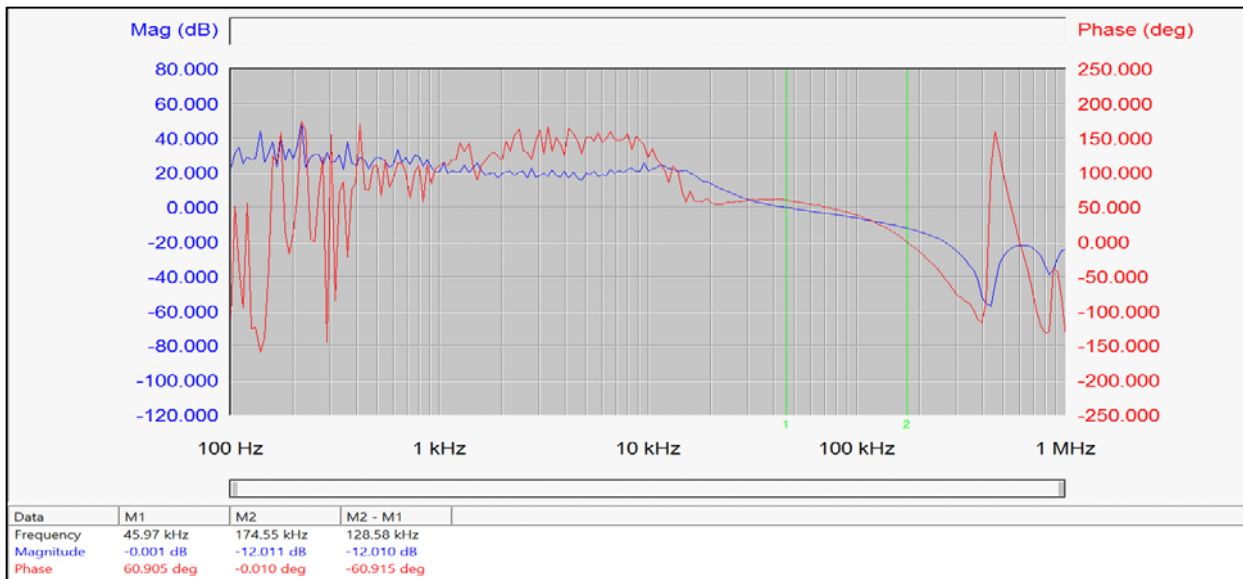
- (1) Break the feedback loop by removing resistor  $R_{11}$  in remote sense path, connected between VSEN+ and VOUT.
- (2) Solder a  $20\Omega$  resistor in  $R_{11}$ 's place. The value of the resistor should be in the range of  $10\Omega$  to  $50\Omega$ .
- (3) Solder a twisted wire pair to the  $20\Omega$  resistor. Ensure that the wires are short in length. A small twisted pair works well by minimizing noise pickup, which is important for a good measurement.
- (4) Enable Channel 1.
- (5) Use a network analyzer to inject a small AC signal ( $\sim 20\text{mV}$ ) across the  $20\Omega$  resistor as shown in [Figure 3 on page 8](#).
- (6) Measure the amplitudes of the signals at points A and B as shown in [Figure 3 on page 8](#).
- (7) Sweep the frequency using the network analyzer to observe the bandwidth, phase, and gain margin.



**Figure 3. Network Analyzer Connection**

[Figure 4](#) shows an example plot generated by the network analyzer for the RAA210925 at 12V input and 1.5V/25A output at 421 kHz with  $12 \times 100\mu\text{F}$  ceramic capacitors +  $1 \times 470\mu\text{F}$  POSCAPs at output. ASCR values are set to Gain = 250 and Residual = 100. The plot shows a crossover frequency of 45.97 kHz with a phase margin of  $60.91^\circ$ . A 12dB gain margin is observed at 174.55 kHz.





**Figure 4. Example of Bode Plot Generated Using Network Analyzer**

Refer to the [RAA210925](#) datasheet for detailed design guidelines, including selection of input/output capacitors and different ASCR gain and residual values.

### 3.4 Using the Tracking Function

Numerous high-performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core; therefore, the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications. In this condition, the voltage tracking function is expected to ensure a safe power up.

The RAA210925 integrates a tracking scheme that allows one of its outputs (Channel 1 or Channel 2) to track a voltage applied to the VTRKP and VTRKN pins with no external components required. The VTRKP and VTRKN pins are analog inputs that configure the voltage applied to the VTRKP and VTRKN pins to act as a reference for the device's output regulation when tracking is enabled.

The VOUT\_COMMAND needs to be set the same as the target tracking voltage when tracking is enabled. For example, the VOUT\_COMMAND of Channel 2 (VOUT2 which enables the tracking) must be set to 1V if tracking 100% is selected and a ramp of 1V is applied to VTRKP and VTRKN. The VOUT\_COMMAND of Channel 2 (VOUT2 which enables the tracking) must be set to 1V if tracking 50% is selected and a ramp of 2V is applied to VTRKP and VTRKN.

To set Channel 2 (VOUT2 = 1V) to 100% track Channel 1 (VOUT1 = 1V), complete the following steps:

- (1) Choose the RSET on SS/Track pin based on the desired Ton/off delay and ramp time (refer to the "VSET\_FINE Settings" table in the [RAA210925](#) datasheet). Populate this chosen resistor value at placeholder R6 on the RTKA2109252H00000BU evaluation board.
- (2) Connect VOUT1 to VTRKP by populating a 0Ω resistor at R30.
- (3) Connect VTRKN to GND by populating a 0Ω resistor at R33.
- (4) Populate RVSET1 and RVSET2 with 0Ω resistors to set VOUT\_COMMAND of VOUT1 and VOUT2 to 1V.
- (5) Enable Channel 2 first, then enable Channel 1.
- (6) Observe the VOUT1, VOUT2, PHASE1, and PHASE2 waveforms on an oscilloscope. VOUT2 follows VOUT1 as shown in [Figure 5 on page 10](#).
- (7) Disable Channel 1. VOUT2 follows VOUT1 as shown in [Figure 6 on page 10](#).

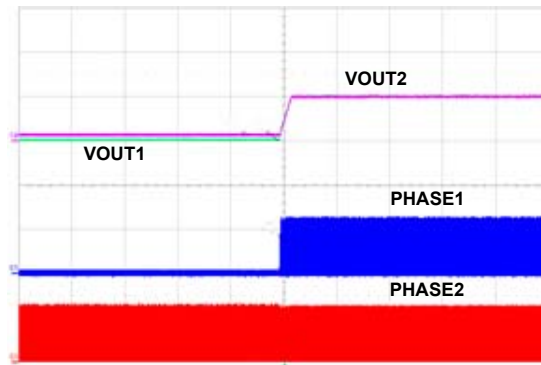


Figure 5. VOUT2 Tracking VOUT1 when Channel 1 is Enabled



Figure 6. VOUT2 Tracking VOUT1 when Channel 1 is Disabled

### 3.5 Interleave Operation

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the  $I_{RMS}^2$  are reduced dramatically.

To enable phase spreading in a multi-module operation, all converters must be synchronized to the same switching clock. The phase offset of each device may be set to any value between  $0^\circ$  and  $360^\circ$  in  $22.5^\circ$  increments by choosing the device PMBus address from the “INTERLEAVE” table in the [RAA210925](#) datasheet. The lower four bits of the PMBus address set the value of the INTERLEAVE command. To implement Interleave functionality for a two module operation, complete the following steps:

- (1) Choose SA (SMBus Address) for Module 1 and Module 2 from the “INTERLEAVE” table in the [RAA210925](#) datasheet based on the desired phase difference. Populate the corresponding RSET for SA ( $R_5$ ) according to the [RAA210925](#) datasheet.  
For example, when Module 1 has SA = 28h (INTERLEAVE = 8,  $180^\circ$  phase shift from the rising edge of the external clock) and Module 2 has SA = 24h (INTERLEAVE = 4,  $90^\circ$  phase shift from the rising edge of the external clock), the net phase difference between Module 1 and Module 2 is  $90^\circ$  ( $180^\circ - 90^\circ$ ).
- (2) Populate RSET on CFG for both boards to sync to an external clock source of a particular switching frequency based on the “External Frequency SYNC Settings” table in the [RAA210925](#) datasheet.
- (3) Connect the power supply to the VIN connectors (VIN/GND) on both boards.

- (4) Connect the ZLUSBEVAL3Z dongle to the 6-pin male connector labeled “PMBus DONGLE In” to one of the boards.
- (5) Daisy chain the second board to the first board by connecting “PMBus DONGLE Out” of first board to the “PMBus DONGLE In” of the second board.
- (6) Provide an external clock on the SYNC pins of the two boards from a function generator. The external clock frequency from the function generator should be within  $\pm 10\%$  of the listed options shown in the “External Frequency SYNC Settings” table in the [RAA210925](#) datasheet. The incoming clock signal must be stable before the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns.
- (7) Turn the input power supply ON. Next, set the ENABLE switch to the “ENABLE” position.
- (8) Monitor the switch node at the probe points labeled “PHASE1” (TP<sub>10</sub>) and “PHASE2” (TP<sub>11</sub>) on the two boards using an oscilloscope to verify the phase spread set.
- (9) The internal two phases of a module always maintain a phase difference of 180°.
- (10) This functionality can also be verified using the INTERLEAVE command in PowerNavigator.

Note that every module gets assigned a unique Rail ID based on the SA setting. This can be observed in the Power Map window of PowerNavigator.

### 3.6 Thermal Considerations and Current Derating

Board layout is very critical to make the module operate safely and deliver maximum allowable power. To work in the high temperature environments and carry large currents, the board layout needs to be carefully designed to maximize thermal performance. To achieve this, select enough trace width, copper weight, and the proper connectors. The RTKA2109252H00000BU evaluation board is designed for running 25A per channel at room temperature without additional cooling systems needed. However, if the output voltage is increased or the board is operated at elevated temperatures, then the available current is derated. Refer to the derated current curves in the [RAA210925](#) datasheet to determine the maximum output current the evaluation board can supply.  $\theta_{JA}$  is measured by inserting a thermocouple inside the module to measure peak junction temperature.

## 4. PCB Layout Guidelines

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary.

- Establish separate SGND plane and PGND planes, then connect SGND to the PGND plane on a middle layer and underneath PAD<sub>6</sub> with a single point connection. For SGND and PGND pin connections, such as small pins H<sub>16</sub>, J<sub>16</sub>, M<sub>5</sub>, and M<sub>17</sub>, use multiple vias for each pin to connect to inner SGND or PGND layers.
- Place enough ceramic capacitors between VIN and PGND and VOUT and PGND. Bypass capacitors between VDD, VDRV, and the ground plane, as close to the module as possible to minimize high-frequency noise. It is critical to place the output ceramic capacitors close to the VOUT pads and in the direction of the load current path to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for the power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers. Renesas recommends enlarging PAD<sub>11</sub> and PAD<sub>9</sub> to place more vias on them. The ceramic capacitors CIN can be placed on the bottom layer under these two pads.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation and place the two traces in parallel. Route a trace from VSEN<sub>1</sub>/VSEN<sub>2N</sub> and VSEN<sub>1</sub>/VSEN<sub>2P</sub> to the point of load where tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN and VSENP sensing lines, near the SW pins.
- PAD<sub>14</sub> and PAD<sub>16</sub> (SW<sub>1</sub> and SW<sub>2</sub>) are noisy pads but are beneficial for thermal dissipation. If the noise issue is critical for the applications, Renesas recommends using only the top layer for the SW pads. For better thermal performance, use multiple vias on these pads to connect into the SW inner and bottom layers. However, use caution when placing a limited area of SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid noise coupling.
- Renesas recommends connecting pins SWD<sub>1</sub> (L<sub>3</sub>) and SWD<sub>2</sub> (P<sub>10</sub>) to the related SW<sub>1</sub> and SW<sub>2</sub> pads with short loop traces. The trace width should be more than 20 mils.

### 4.1 Board Pictures

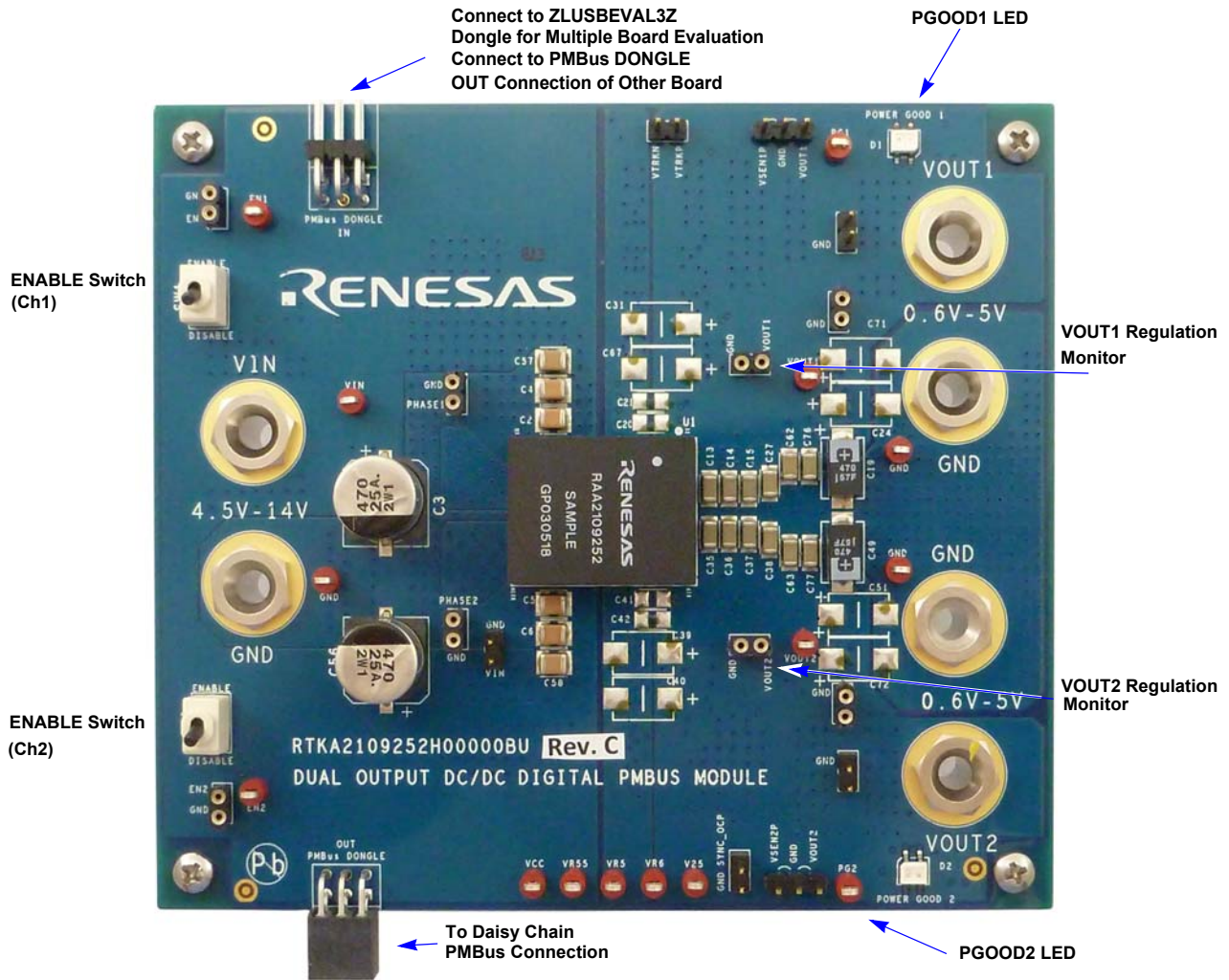


Figure 7. Top of Board

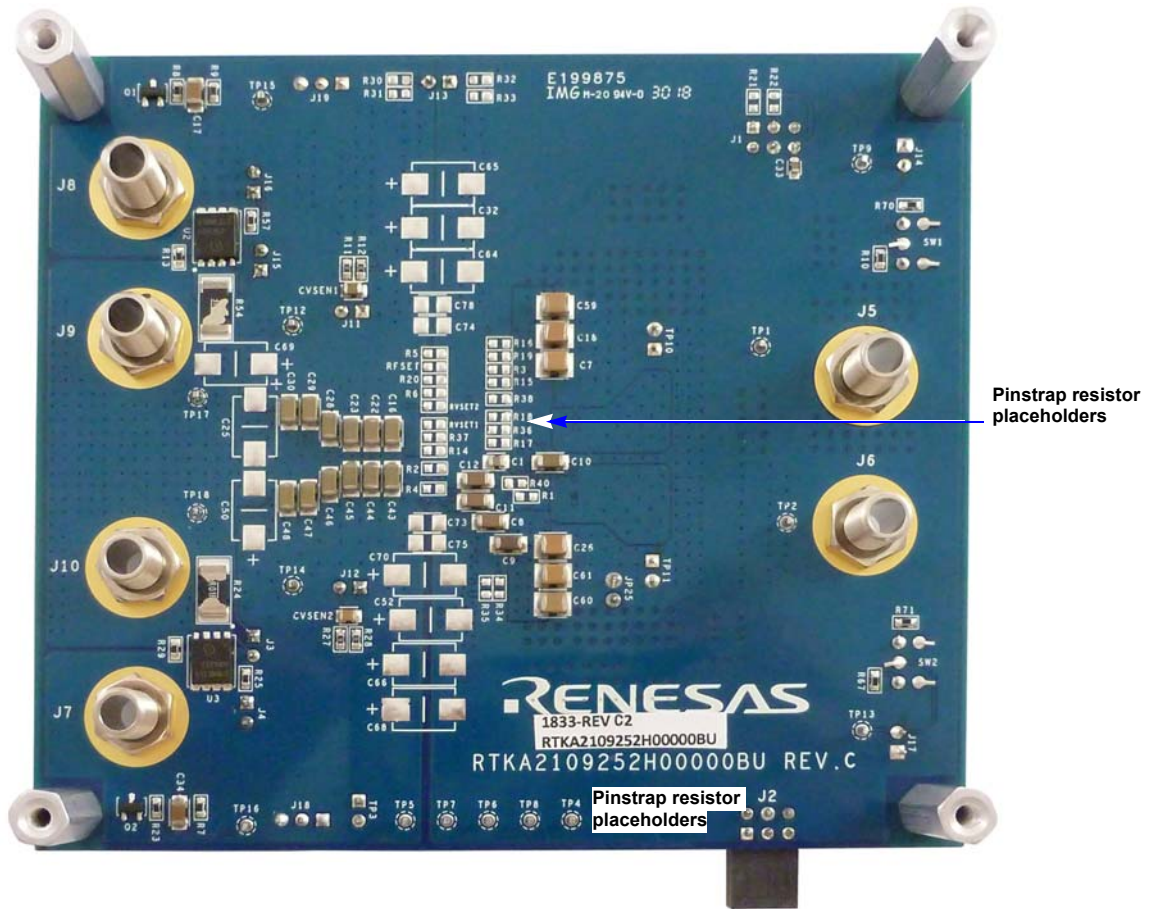


Figure 8. Bottom of Board

### 4.2 RTKA2109252H00000BU Schematic

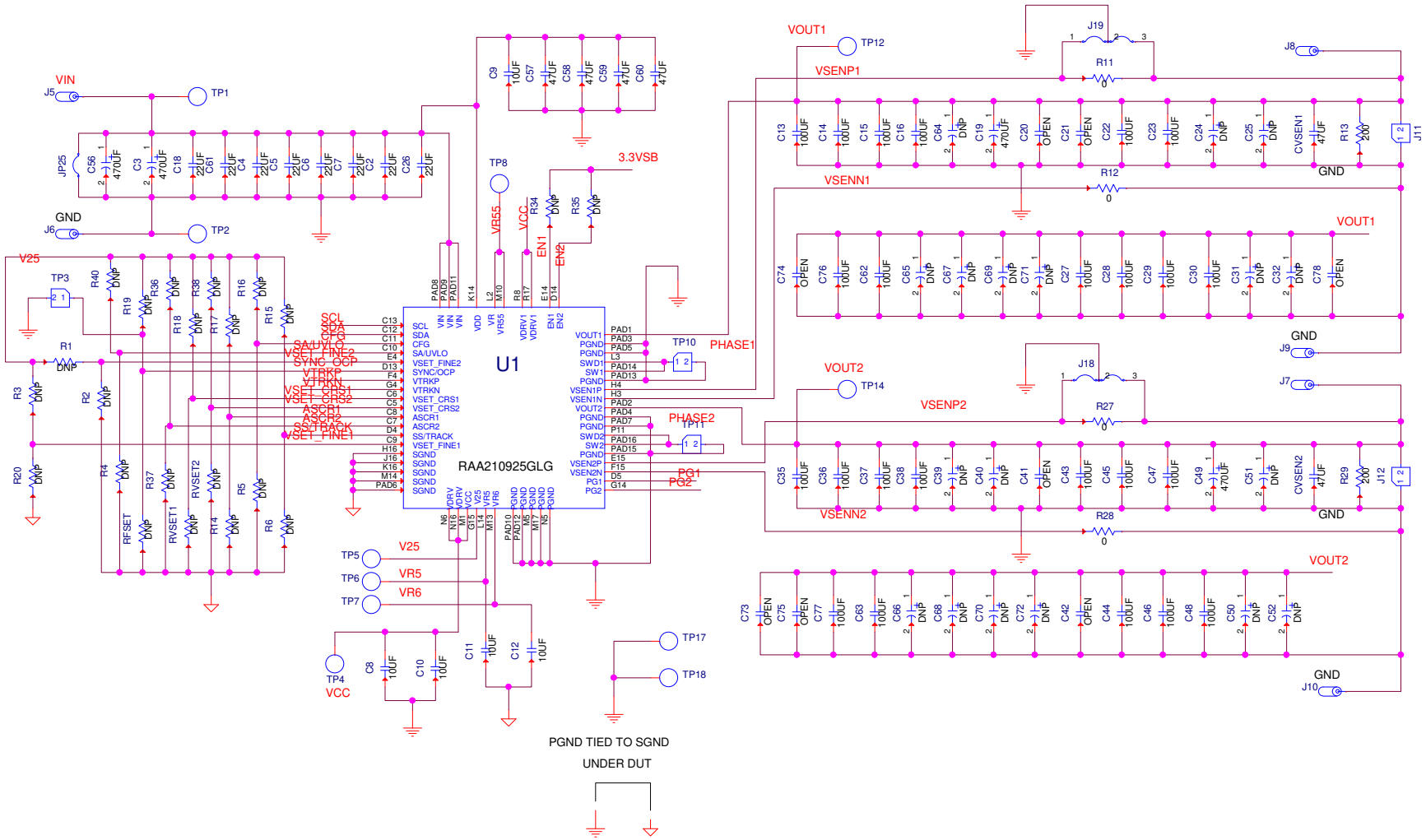


Figure 9. Schematic (1 of 2)

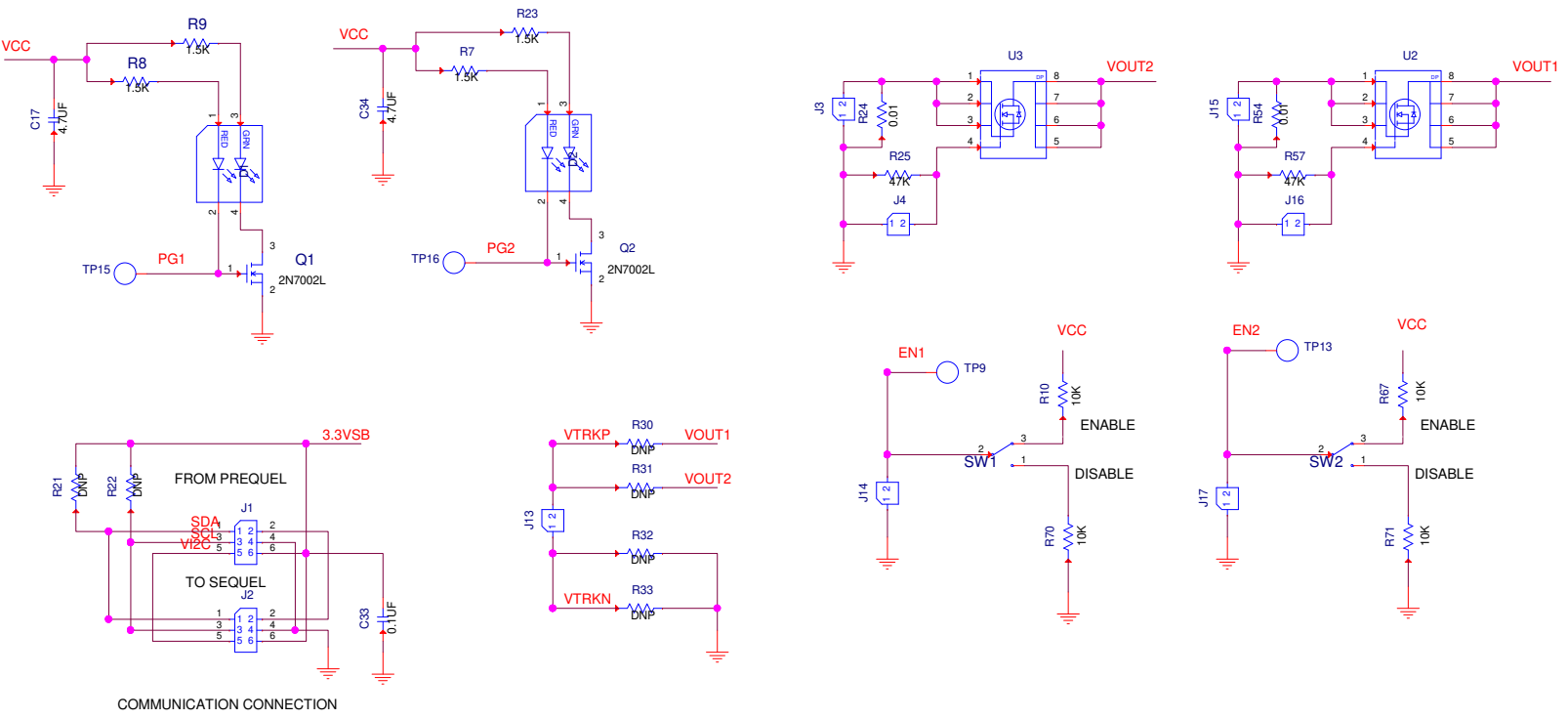


Figure 10. Schematic (2 of 2)



### 4.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1		PCB, RTKA2109252H00000BU, RoHS	Renesas	PCB, RTKA2109252H00000BU
24	C13, C14, C15, C16, C22, C23, C27, C28, C29, C30, C35, C36, C37, C38, C43, C44, C45, C46, C47, C48, C62, C63, C76, C77	CAP CER 100 $\mu$ F, 6.3V, 20%, X6T, 1206, RoHS	Murata	GRM31CD80J107ME39L
2	C17, C34	CAP CER 4.7 $\mu$ F, 10V, 10%, X7R, 1206, RoHS	Murata	GRM31CR71A475KA01L
2	C19, C49	CAP TANT POLY 470 $\mu$ F, 6.3V, 20%, 10m $\Omega$ , 2917, RoHS	Panasonic	6TPF470MAH
8	C2, C4, C5, C6, C7, C18, C26, C61	CAP CER 22 $\mu$ F, 25V, 10%, X7R, 1210, RoHS	Murata	GRM32ER71E226KE15L
8	C20, C21, C41, C42, C73, C74, C75, C78	DO NOT POPULATE_PLACE HOLDER		
18	C24, C25, C31, C32, C39, C40, C50, C51, C52, C64, C65, C66, C67, C68, C69, C70, C71, C72	DO NOT POPULATE_PLACE HOLDER		
2	C3, C56	CAP ALUM 470 $\mu$ F, 20%, 25V, SMD, RoHS	Panasonic	EEE1EA471P
1	C33	CAP CER 0.1 $\mu$ F, 25V, 10%, X7R, 0603, RoHS	KEMET	C0603X104K3RACTU
4	C57, C58, C59, C60	CAP CER 47 $\mu$ F, 16V, 10%, X5R, 1210, RoHS	Murata	GRM32ER61C476KE15L
4	C8, C10, C11, C12	CAP CER 10 $\mu$ F, 10V, 10%, X7R, 1206, RoHS	Murata	GRM31CR71A106KA01L
1	C9	CAP CER 10 $\mu$ F, 25V, 10%, X7R, 1206, RoHS	Murata	GRM31CR71E106KA12L
2	CVSEN1, CVSEN2	CAP CER 47 $\mu$ F, 10V, 20%, X5R, 0805, RoHS	Murata	GRM21BR61A476ME15L
4	R10, R67, R70, R71	RES SMD 10k $\Omega$ , 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1002V
4	R11, R12, R27, R28	RES SMD 0 $\Omega$ JUMPER, 1/10W, 0603, RoHS	Panasonic	ERJ-3GEY0R00V
2	R13, R29	RES SMD 200 $\Omega$ , 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF2000V
28	R1, R2, R3, R4, R5, R6, R14, R15, R16, R17, R18, R19, R20, R21, R22, R30, R31, R32, R33, R34, R35, R36, R37, R38, R40, RFSET, RVSET1, RVSET2	DO NOT POPULATE_PLACE HOLDER		
2	R24, R54	RES 0.01 $\Omega$ , 1%, 2W, 2512, RoHS	Vishay	WSL2512R0100FEA
2	R25, R57	RES SMD 47k $\Omega$ , 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF4702V
4	R7, R8, R9, R23	RES SMD 1.5k $\Omega$ , 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1501V

1	U1	25A/25A Dual Channel Digital PMBus Step-Down Power Module, RoHS	Renesas	RAA210925GLG
2	U2, U3	MOSFET N-CH 25V, 39A, TDSO8, RoHS	Infineon	BSC010NE2LS
2	D1, D2	LED GREEN/RED CLEAR AXIAL SMD, RoHS	Lumex Opto	SSL-LXA3025IGC
2	Q1, Q2	MOSFET N-CH 60V, 0.115A, SOT-23, RoHS	ON Semiconductor	2N7002L
2	SW1, SW2	SWITCH TOGGLE SPDT, 0.4VA, 20V, RoHS	C&K	GT13MCBE
12	TP1, TP4, TP5, TP6, TP7, TP8, TP9, TP12, TP13, TP14, TP15, TP16	Miniature Red Test Point .100 Pad .040 Thole	Keystone Electronics	5000
3	TP2, TP17, TP18	Miniature Black Test Point .100 Pad .040 Thole	Keystone Electronics	5001
1	J1	CONN-HEADER, 2x3, BRKAWY, 2.54mm, TIN, R/A, RoHS	Samtec	TSW-103-08-T-D-RA
2	J18, J19	3 Positions Header, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold, RoHS	Amphenol	68000-103HLF
1	J2	CONN-SOCKET STRIP, TH, 2x3, 2.54mm, TIN, R/A, RoHS	Samtec	SSQ-103-02-T-D-RA
8	J3, J11, J12, J14, J15, J17, TP10, TP11	2 Positions Receptacle Socket, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold, RoHS	Mill-Max	310-93-164-41-001000
5	J4, J13, J16, TP3, JP25	CONN HEADER 2POS .100" SNGL, RoHS	Samtec	TSW-102-07-F-S
6	J5, J6, J7, J8, J9, J10	Banana Jack Connector Standard Banana Threaded, External (Nut), RoHS	Clinch Connectivity	108-0740-001

### 4.4 Layout

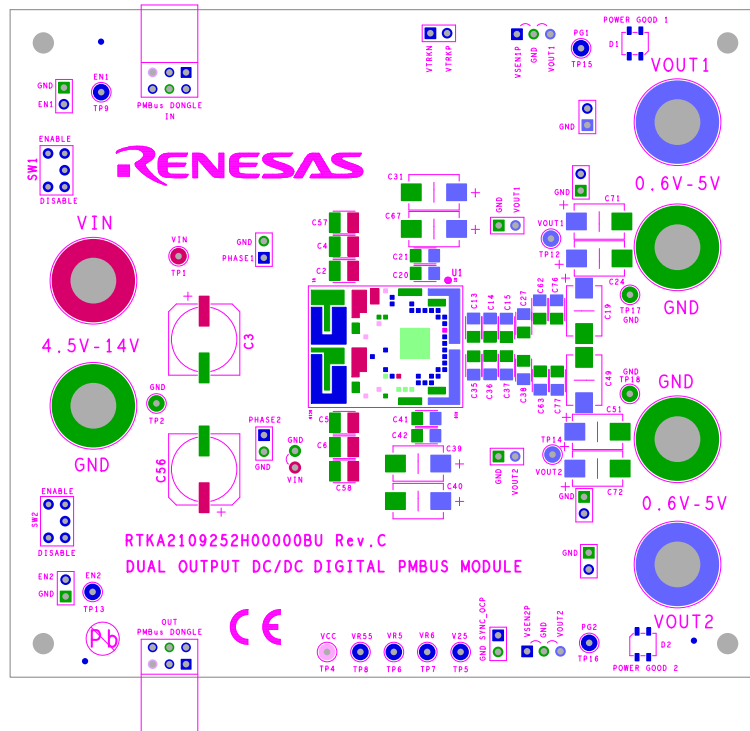


Figure 11. Silkscreen Top

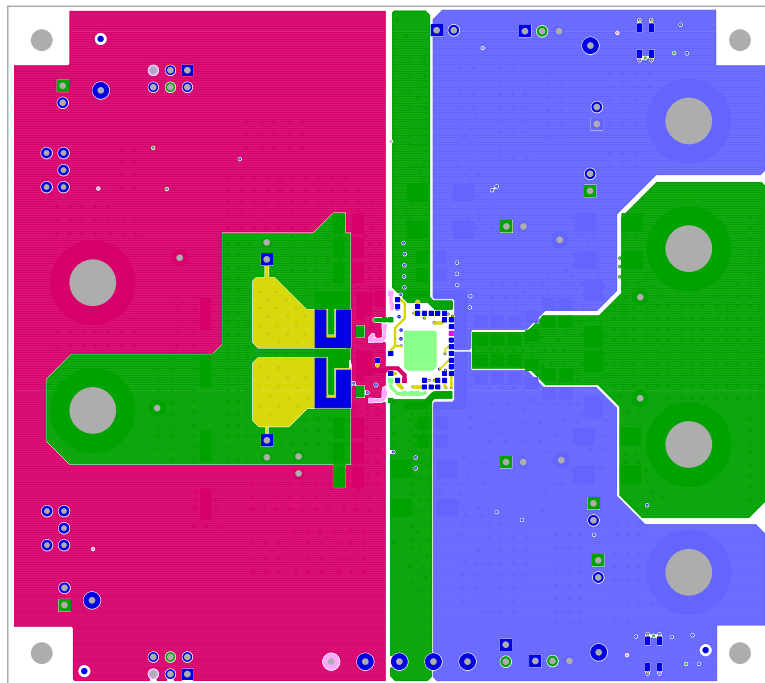


Figure 12. Top Layer

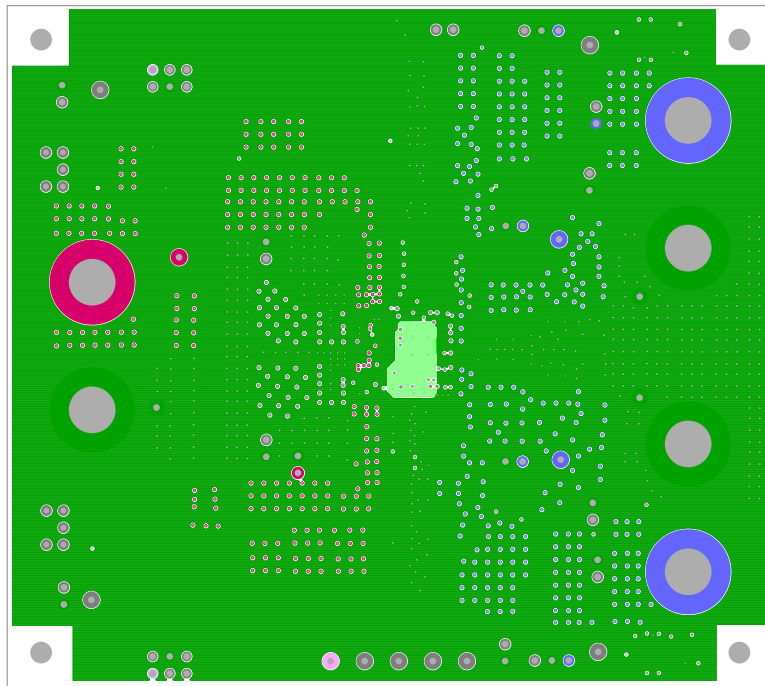


Figure 13. Layer 2

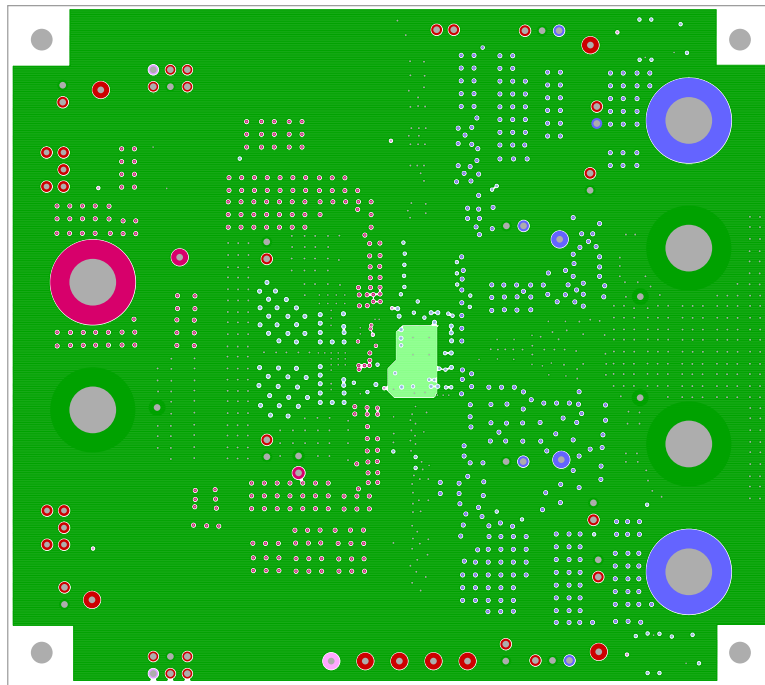


Figure 14. Layer 3

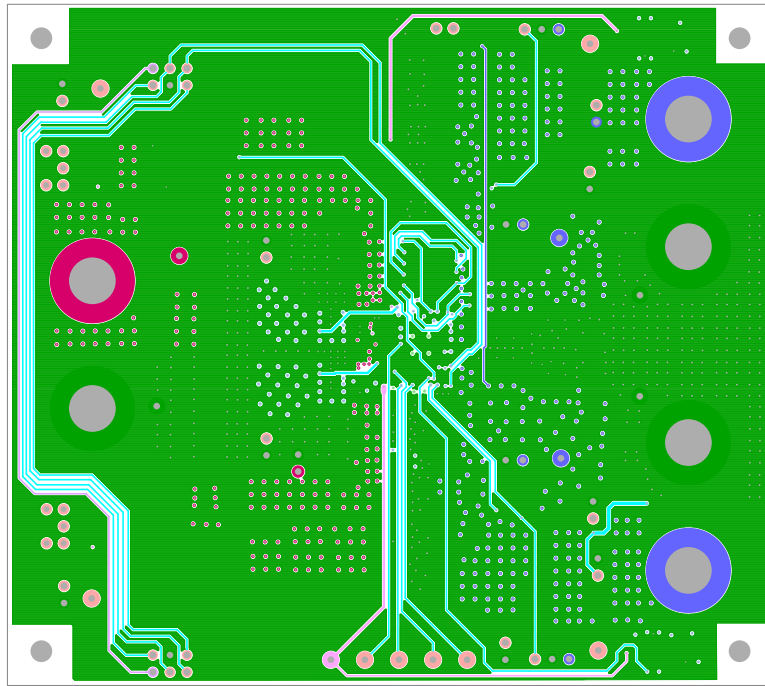


Figure 15. Layer 4

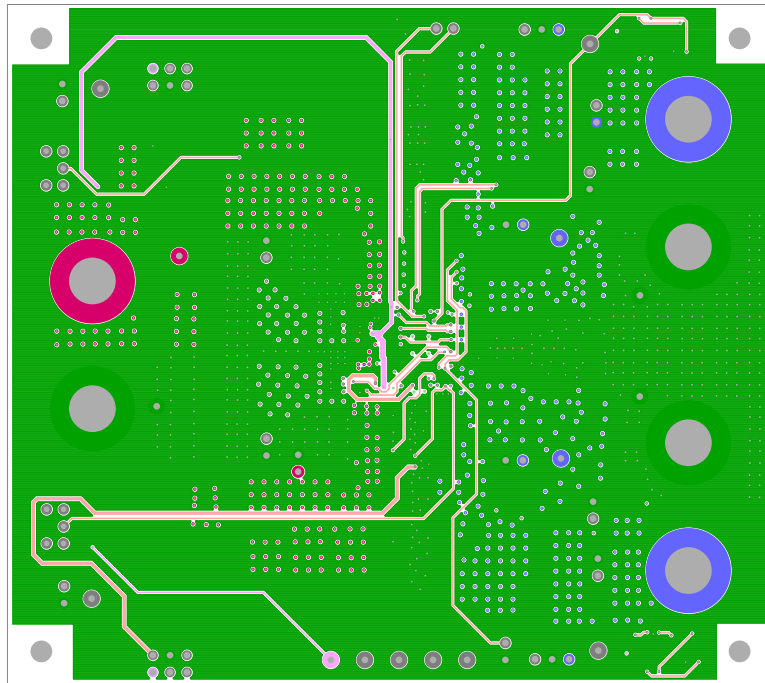


Figure 16. Layer 5

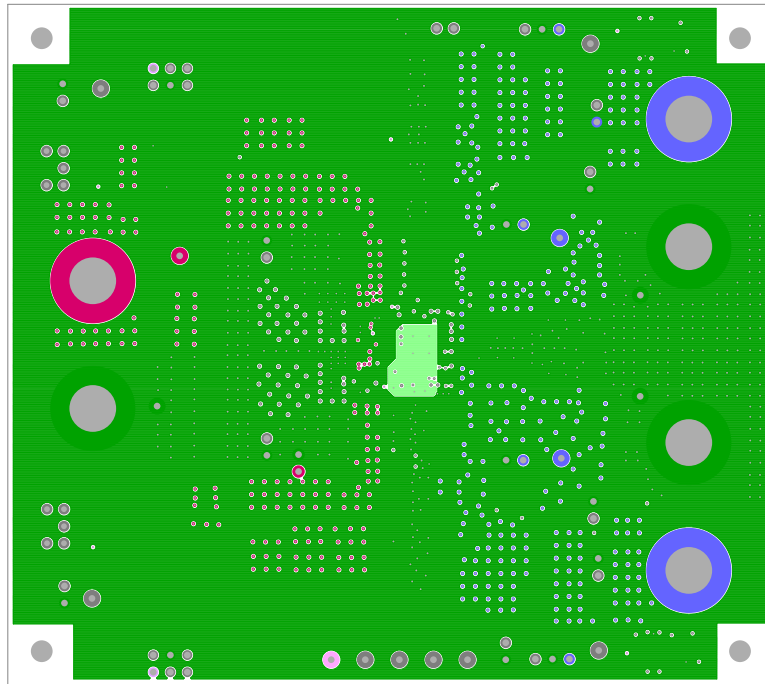


Figure 17. Layer 6

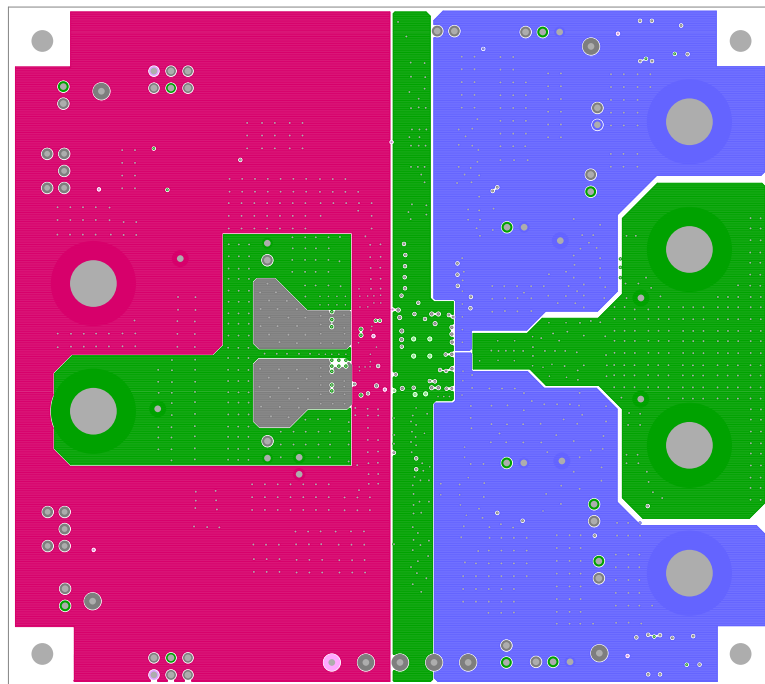


Figure 18. Layer 7

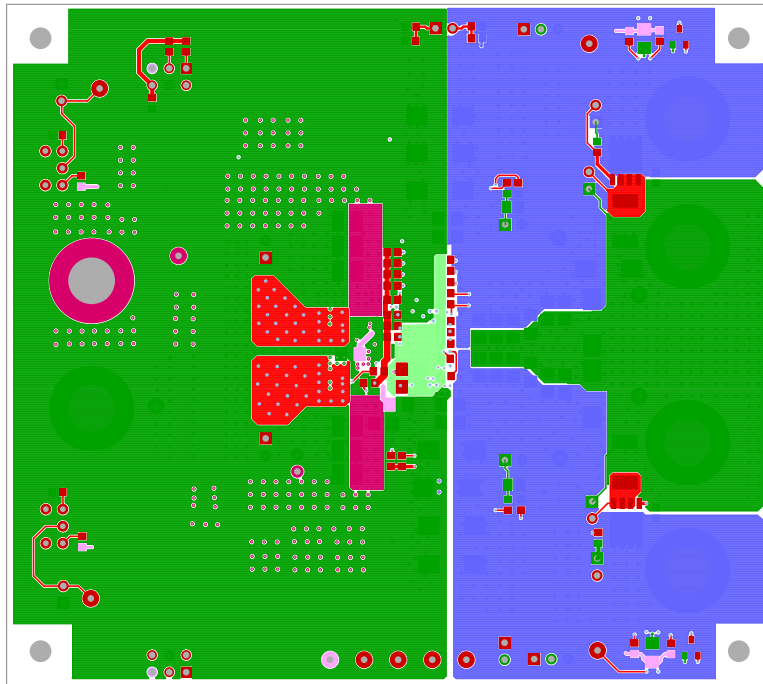


Figure 19. Bottom Layer

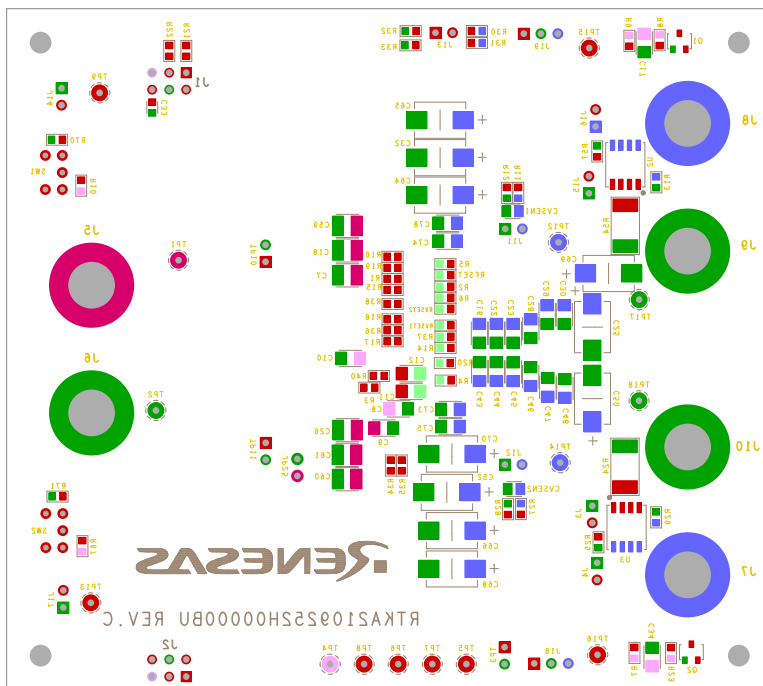


Figure 20. Silkscreen Bottom

## 5. Typical Performance Data

The following data was acquired using an RTKA2109252H00000BU evaluation board. Operating conditions:  $T_A = 25\text{ }^\circ\text{C}$ , no air flow.  $C_{out} = 1 \times 470\mu\text{F POSCAP} + 12 \times 100\mu\text{F ceramic}$ . Values are typical unless otherwise noted.

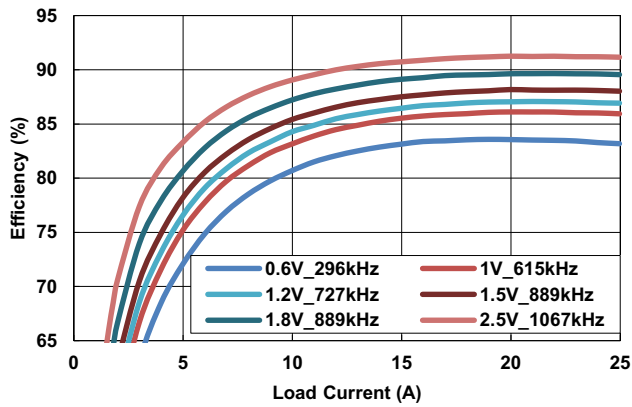


Figure 21. Single Channel Efficiency vs Output Current

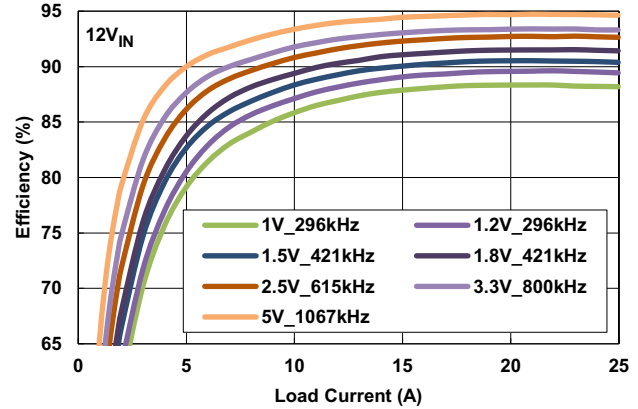


Figure 22. Single Channel Efficiency vs Output Current

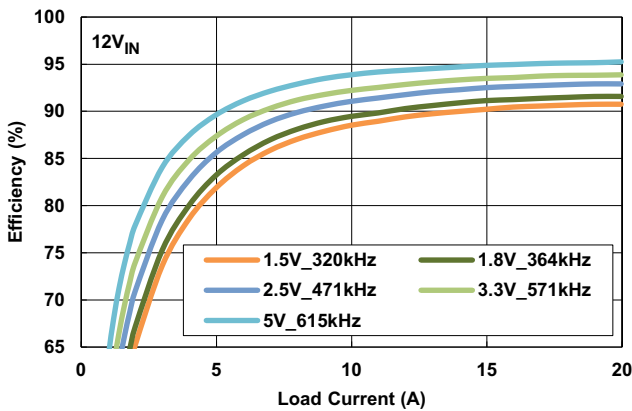


Figure 23. Single Channel Efficiency vs Output Current

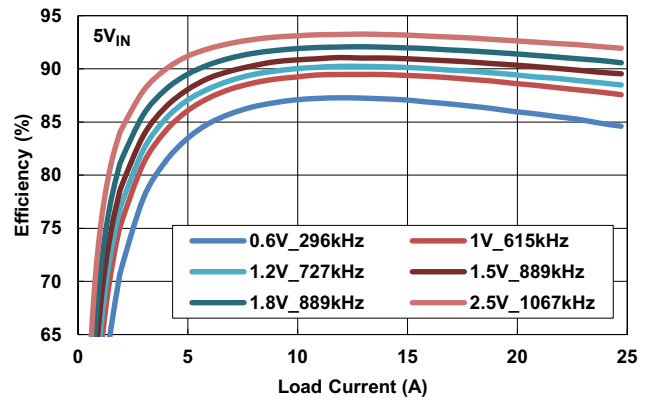


Figure 24. Single Channel Efficiency vs Output Current

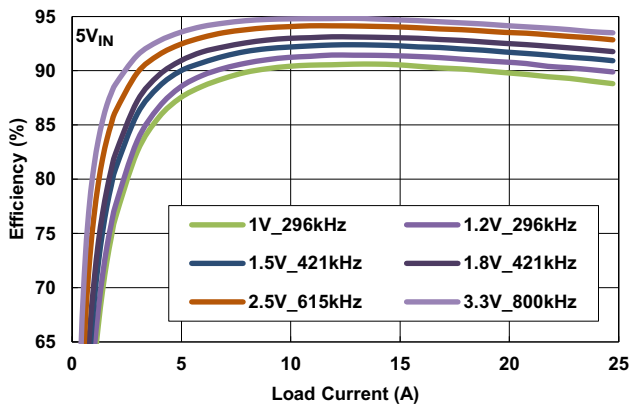


Figure 25. Single Channel Efficiency vs Output Current

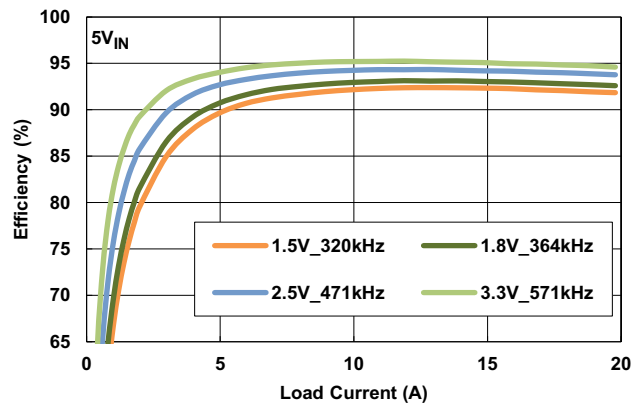


Figure 26. Single Channel Efficiency vs Output Current



The following data was acquired using an RTKA2109252H00000BU evaluation board. Operating conditions:  $T_A = 25\text{ }^\circ\text{C}$ , no air flow.  $C_{out} = 1 \times 470\mu\text{F POSCAP} + 12 \times 100\mu\text{F ceramic}$ . Values are typical unless otherwise noted. **(Continued)**

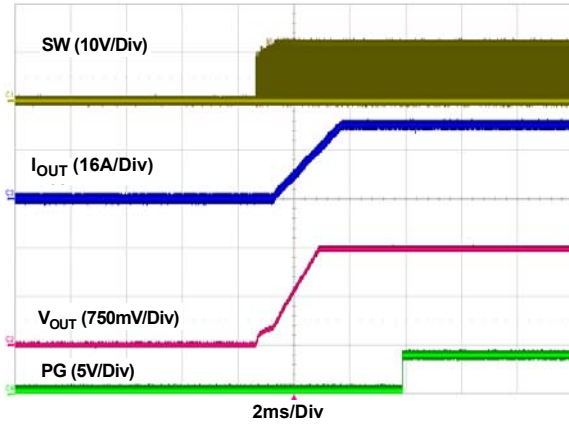


Figure 27. Single Channel Startup  $12\text{V}_{IN}$ ,  $1.5\text{V}_{OUT}$ ,  $25\text{A}$

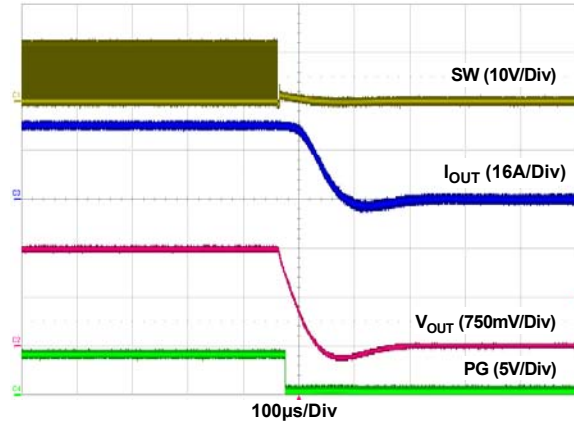


Figure 28. Single Channel Shutdown  $12\text{V}_{IN}$ ,  $1.5\text{V}_{OUT}$ ,  $25\text{A}$

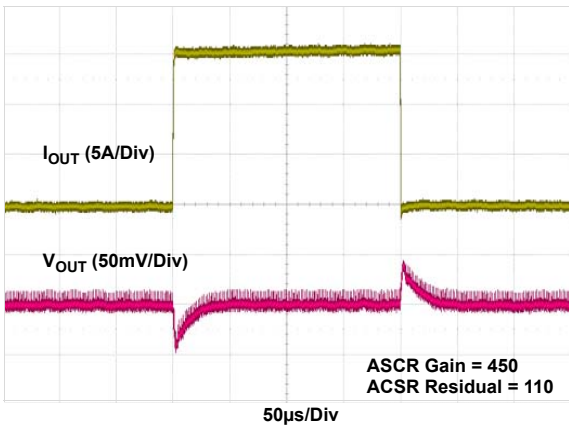


Figure 29.  $0\text{A} - 15\text{A}$ ,  $12\text{V}_{IN}$ ,  $1\text{V}_{OUT}$ ,  $615\text{kHz}$

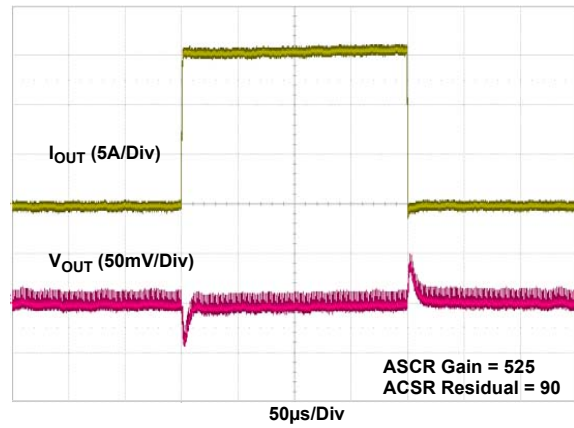


Figure 30.  $0\text{A} - 15\text{A}$ ,  $12\text{V}_{IN}$ ,  $1.5\text{V}_{OUT}$ ,  $889\text{kHz}$

## 6. Revision History

Rev.	Date	Description
0.00	Sep 11, 2018	Initial release

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