DA14535

USB Development Kit Hardware

This document outlines the system design, configuration options, and supported features of DA14535 USB Development Kit revA (610-12-A).

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1. Terms and Definitions

CIB	Communication Interface Board
DCR	Direct Current Resistor
DMIPS	Dhrystone Million Instructions per Second
ESR	Effective Series Resistance
GPIO	General Purpose Input Output
I^2C	Inter-Integrated Circuit
JTAG	Join Test Action Group
LDO	Low Dropout
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
OVP	Over Voltage Protection
PC	Personal Computer
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PLL	Phase-Locked Loop
QSPI	Quad Serial Peripheral Interface
RF	Radio Frequency
RFIO	Radio Frequency Input Output
SDK	Software Development Kit
SIMO	Single-Inductor Multiple-Output
SMA	Sub-Miniature version A
SMD	Surface-Mount Device
SoC	System on Chip
SOIC	Small Outline Integrated Circuit
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

2. References

[1] DA14535, Datasheet, Renesas Electronics.

[2] AN-B-052, DA1458x/68x Development kit J-Link Interface, Application Note, Renesas Electronics.

[3] AN-B-072, DA1453x Booting Options, Application Note, Renesas Electronics.

[4] AN-B-027, Designing Printed Antennas for Bluetooth Smart, Application Note, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

This document describes Renesas DA14535 USB development kit (board reference number 610-12-A). This kit offers a low-cost development board with basic functionality. The development kit is implemented on a single PCB. The block diagram, the actual board, the various sections, and settings as well as the connectivity are presented. The purpose of this cost-effective USB kit is to provide users with the capability for:

- Software development
- Programming DA14535 via JTAG or UART using Renesas DA14535 SDK
- Connecting mikroBUS™ modules.

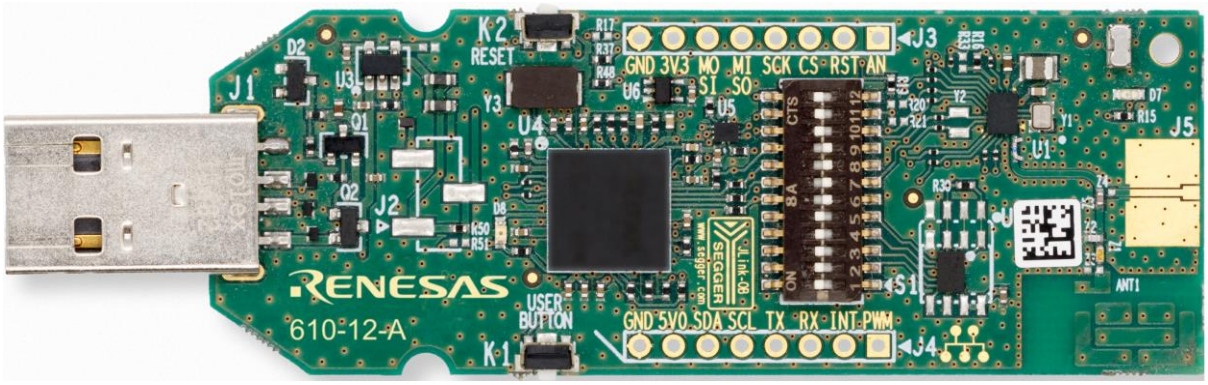

Figure 1. DA14535 USB kit

4. System Overview

4.1 Features

The features of DA14535 USB kit include:

- Highly integrated DA14535 Bluetooth® Smart SoC from Renesas Electronics.
- Access on GPIOs provided from the chip, when no mikroBUS™ is plugged in.
- The ability to be connected directly to PC USB without extra cables.
- Reset push button.
- General purpose LED and button.
- Using USB LDO 3V3 as a power source.
- Unpopulated coin cell battery holder as a powering option.
- JTAG and UART interface over USB (on-board SEGGER J-Link).
- 2 Mbit SPI flash on board.
- 2.4-GHz printed antenna and option for SMA connector.
- 32 MHz main crystal and option for 32.768 kHz low-power crystal.
- Low cost.
- Compact design.

4.2 System and Components Description (Top View)

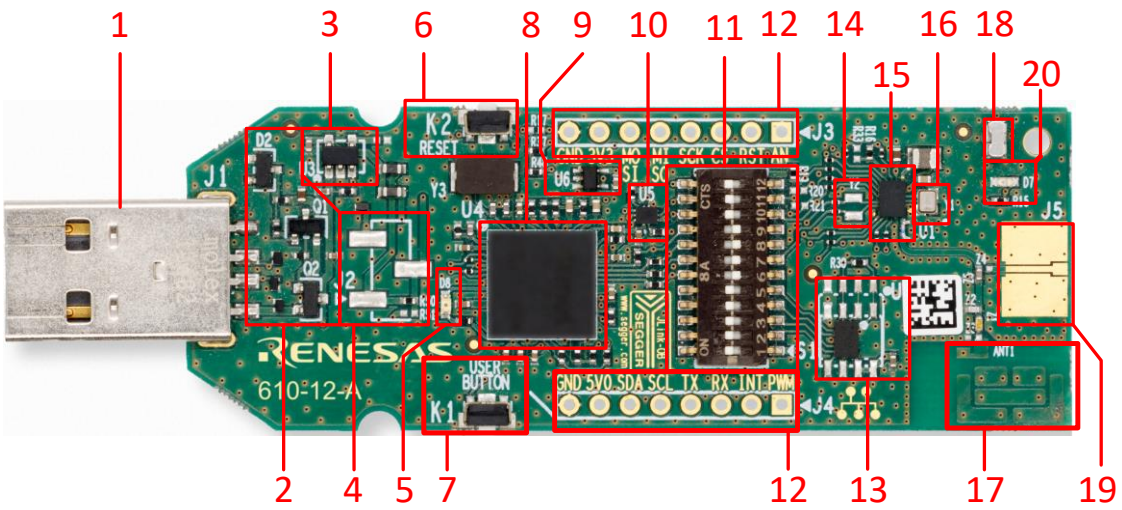

Figure 2. USB kit – top side

This USB development kit is based on the DA14535 SoC in an FCGQFN-24 package. The marked and numbered sections of the system are (see Figure 2):

1. Type-A USB connector (J1).
2. OVP Circuit.
3. LDO 3.3 V (U3).
4. Unpopulated power selection header (J2).
5. J-Link status LED (green).
6. Reset button (SW1).
7. User button (SW2).
8. Debug interface µController (U4).
9. Inverter for J-Link reset (U6).
10. Multiplexer for 1-pin UART (U5).
11. System configuration DIP-switch (S1).
12. Unpopulated mikroBus™ socket (or breakout header in general).
13. 2 Mbit SPI Flash (U2).
14. Unpopulated 32.468 kHz crystal (Y2).
15. DA14535 Bluetooth Smart SoC.
16. 32 MHz crystal.
17. Printed Antenna.
18. GND test-point.
19. Unpopulated SMA connector (J5).
20. User LED (orange).

4.3 System and Components Description (Bottom View)

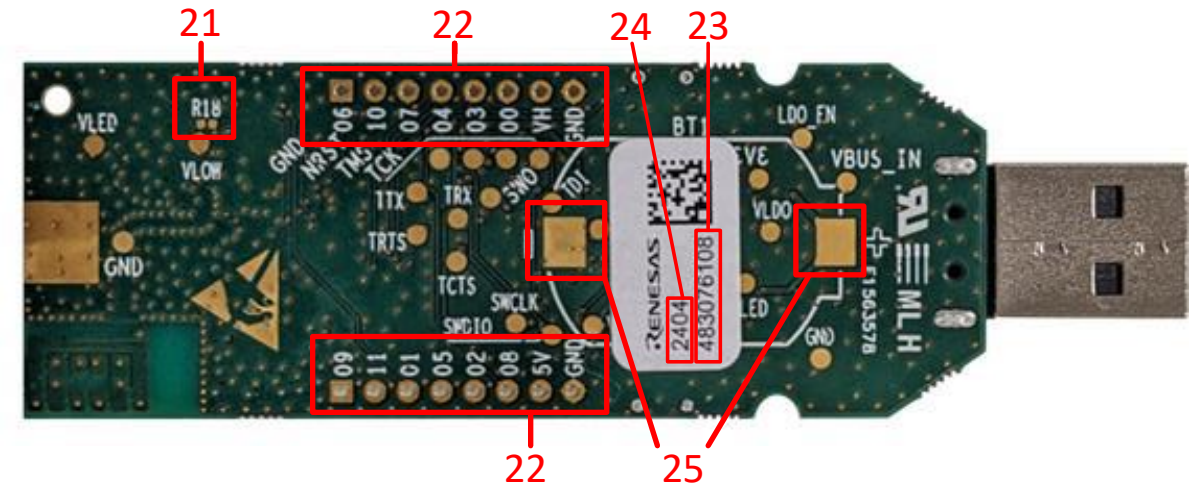

Figure 3. USB Kit - bottom side

The bottom side of the USB development kit provides information about the mikroBus™ pins assignment, the SEGGER ID, and the date code. Test points have been placed for monitoring various signal behaviors and voltage levels of the components. The marked and numbered sections of the system are:

21. Unpopulated resistor for bypass mode.
22. GPIO numbers (add P0_ before the number for the full name).
23. J-Link debugger serial number.
24. Production Date Code (See Appendix D).
25. Pads to solder a coin cell holder.

5. USB Kit System

5.1 Overview

- Board name/number:
  - DA14535 USB development kit/610-12-A.
- SoC:
  - DA14535 in FCGQFN-24 package.
- Flash memory:
  - AT25DF021A, 2 Mbit, QSPI Flash Memory in 8-pin U-SON (2 mm × 3 mm) package. Note that it is accessed in plain SPI mode.
  - 3.3 V power supply (V_{HIGH}).
- Clock inputs:
  - 32 MHz crystal.
  - Optional low power 32.768 kHz crystal.
- Power
  - 3.3 V LDO powering V_{HIGH} on DA14535 (buck mode configuration).
- Ports:
  - USB port for debugging purposes.
- Interfaces:
  - UART-J-Link CDC UART Port (listed under Ports in Device Manager).
  - JTAG-J-Link Driver (listed under Universal Serial Bus Controllers in Device Manager).
  - DIP switch to select between interfaces and isolate the signals for accurate power measurements.
- Connectivity expansion connectors:
  - One mikroBUS™ module can be plugged to J3/J4. Note that most GPIOs are already used for booting and debugging, so compatibility with any random Click™ board is not guaranteed.

5.2 DA14535 System

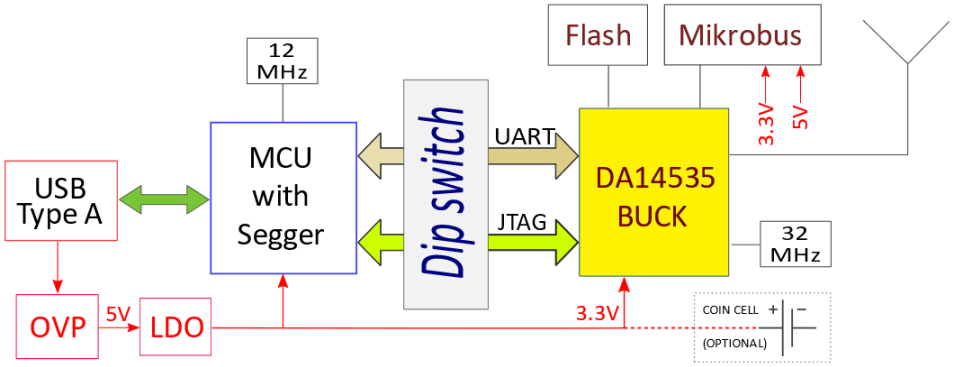

Figure 4. Block diagram of DA14535 USB development kit

Renesas DA14535 is an ultra-low power SoC integrating a 2.4 GHz Bluetooth Low Energy transceiver and an Arm® Cortex®M0+ microcontroller with 48 kB RAM and 32 kB One-Time Programmable (OTP) ROM. It can be used as a standalone application processor or as a data pump in hosted systems.

The DA14535 SoC also includes a cryptography engine, a power management unit, digital and analog peripherals, and a radio transceiver.

The DA14535 has dedicated hardware for the Link Layer implementation of Bluetooth LE and interface controllers for enhanced connectivity capabilities. The radio transceiver, the baseband processor, and the qualified Bluetooth low energy stack is fully compliant with the Bluetooth Low Energy 5.3 standard.

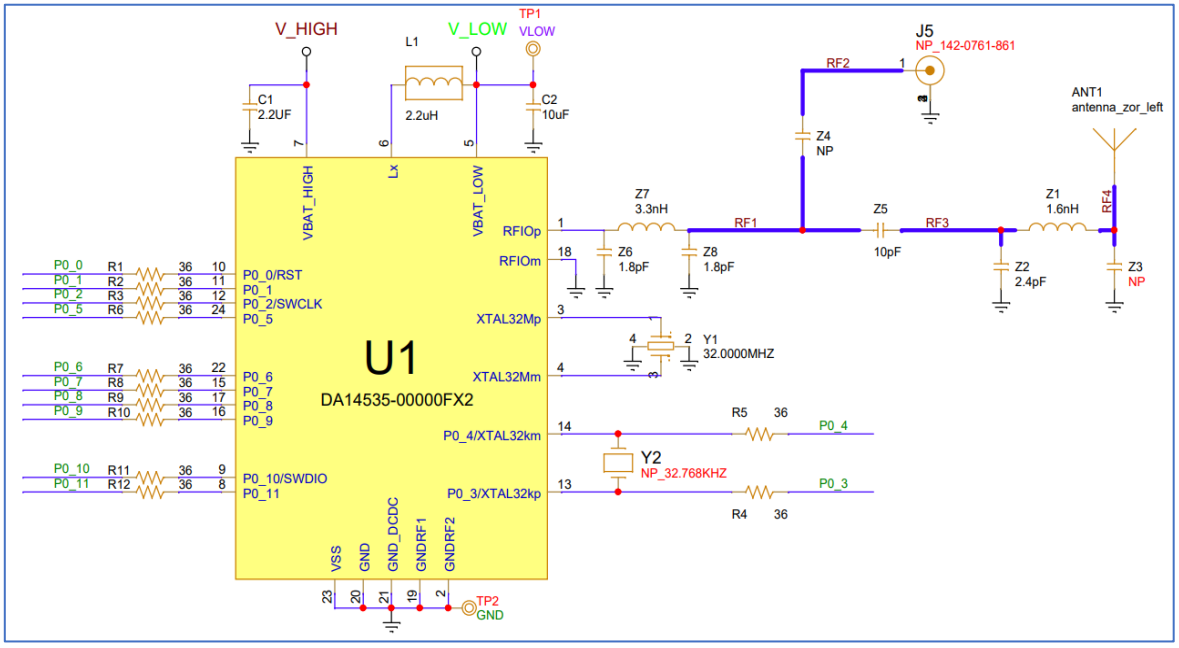

Figure 5. DA14535 section schematic

The DA14535 SoC power management subsystem consists of:

- VHIGH: LDO/Battery input (buck configuration, default is 3.3 V from LDO).
  - A 2.2 µF decoupling capacitor (C1) is required close to the pin.
- VLOW: 1.1 V typical output (buck configuration).
  - A 10 µF decoupling capacitor (C2) is required close to the pin.
- The inductor needed for DC-DC operation is placed externally. A low DCR 2.2 µH inductor (L1) is connected between LX and VLOW pins.

5.3 DA14535 GPIO Assignment

Most of the available signals are utilized or extracted on the breakout connectors.

Table 1 shows the pin assignment on the development kit peripheral function and the related pin name on the FCGQFN24 package of the DA14535.

Table 1. DA14535 USB development kit pin assignment

		UART 2-wires	JTAG	SPI Flash	Full UART	XTAL 32kHz	Single UART	Other
GPIOs	P0_0	UTX (Note 1)	SWDIO (Note 1)	MOSI	UTX (Note 1)		UTX/URX (Note 1)	SW1/ RESET
	P0_1	URX (Note 1)		/CS	URX (Note 1)			
	P0_2		SWCLK					
	P0_3			MISO	UCTS (Note 1)	XTAL (Note 1)	UTX/URX (Note 1)	
	P0_4			SCK	URTS (Note 1)	XTAL (Note 1)		
	P0_5		SWDIO (Note 1)				UTX/URX	
	P0_6							
	P0_7							
	P0_8							
	P0_9							LED
	P0_10		SWDIO					
	P0_11							BUTTON

Note 1 This option is available for the pin and can be implemented on the board but requires software, hardware, and/or OTP modifications.

5.4 Default Configuration

Because GPIOs P0_0 to P0_6 support multiple functions, the default system is limited to a subset of the possible options. Figure 6 shows the default DIP switch configuration.

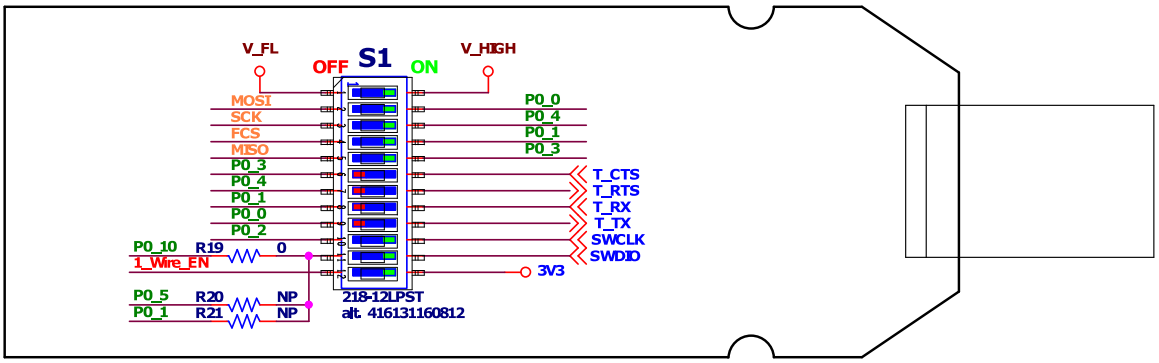

Figure 6. Default DIP switch configuration

This allows the system to boot from external flash or 1-wire UART and communicate through JTAG for debugging.

Table 2. Default configuration DIP settings

DIP number	DA14535 GPIO	Related function
2	P0_0	QSPI MOSI
4	P0_1	QSPI CS
10	P0_2	SWD CLK
5	P0_3	QSPI MISO
3	P0_4	QSPI CLK
12	P0_5 (enable)	1-wire UART
11	P0_10	SWD DIO

5.5 1-wire Bootable UART

Since most UART communication is typically half-duplex, it is possible to use a single pin for both the Rx and the Tx channel. DA14535 has dedicated hardware that supports this function and two related boot steps predefined. An analog multiplexer shown in Figure 7 (controlled by position #12 on the DIP switch) connects the UART signals to P0_5 (which is the first option on boot sequence for 1-wire UART).

The external Tx is connected to the external Rx through a 1 K series resistor. This means that any data transmitted from the host PC will be repeated (looped-back) to the Rx channel. Renesas SmartSnippets Toolbox will automatically filter out the looped data. Non-Renesas tools should take precautions for this.

The host serial port settings required are:

- Baud rate 115.2 kbps
- 8 bits
- No parity
- 1 stop bit.

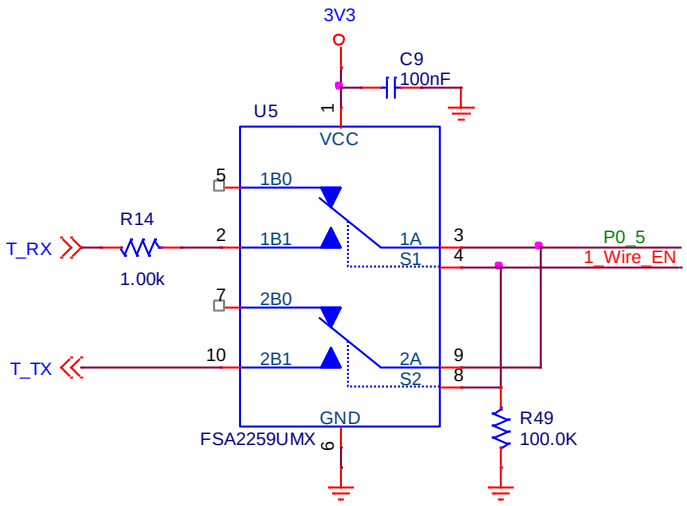

Figure 7. Single pin UART multiplexer

5.6 Optional 2-/4-Wire UART

It is possible to use a 2-wire or 4-wire UART for booting or other activities, but it is not possible to boot from the SPI flash in this configuration. To enable the UART and disable SPI, it is required to modify the DIP switch as shown in Figure 8.

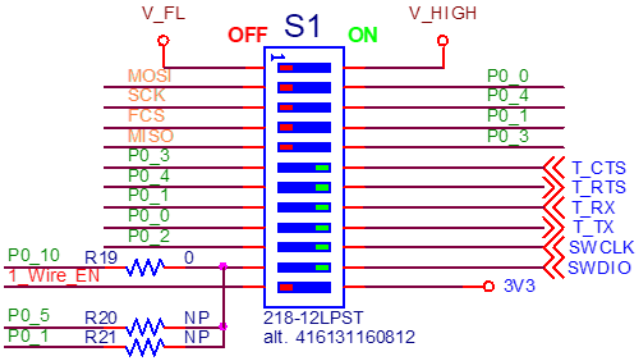

Figure 8. DIP switch configuration for UART

The flow control signals (RTS and CTS) are not needed for booting.

Table 3. UART configuration DIP settings

DIP number	DA14535 GPIO	Related function
9	P0_0	UART Tx
8	P0_1	UART Rx
6	P0_3	UART CTS
7	P0_4	UART RTS

The host serial port settings required are:

- Baud rate 115.2 kbps
- 8 bits
- No parity
- 1 stop bit.

For more details, see Ref. [2] and Ref. [3].

5.7 Crystals

The DA14535 SoC has two Digitally Controlled Crystal Oscillators, one at 32 MHz (XTAL32M) and the other at 32.768 kHz (XTAL32K). XTAL32K has no trimming capabilities and is used as the clock for low power sleep modes, while XTAL32M can be trimmed.

XTAL32K is by default left unpopulated, because it cannot be used together with an SPI flash connected to the same GPIOs. The internal RCX low-power oscillator is capable of operating with reasonable accuracy in most practical cases. XTAL32K may be required for applications that need to have higher accuracy in low power clock timekeeping or as the source for a Real Time Clock. In that case the crystal can be populated but the on-board flash will not be usable as a boot device. The firmware in that case can reside on the OTP memory. Using external flash at different pins as boot device is also possible with the use of a suitable bootloader in OTP memory.

The crystals selected for the basic development kit are specified in Table 4 and Table 5.

Table 4. Y1 (32 MHz crystal) characteristics

Reference designator	Value
Part Number	XRCGB32M000F1H00R0
Frequency	32 MHz
Accuracy	±10 ppm
Load Capacitance (CL)	6 pF
Equivalent Series Resistance (ESR)	60 Ω
Drive Level (PD)	150 µW

Table 5. Y2 (32 kHz crystal) characteristics

Reference designator	Value
Part Number	SC20S-7PF20PPM
Frequency	32.768 kHz
Accuracy	±20 ppm
Load Capacitance (CL)	7 pF
Shunt Capacitance (C0)	1.3 pF
Motional Resistance (ESR)	70 kΩ max
Drive Level (PD)	0.1 µW max

5.8 Antenna and RF Port

A printed ZOR-antenna (ANT1) is used by default as the radiating element for the DA14535 USB development kit. For more details, see Ref. [4].

To perform conducted RF measurements:

1. Remove Z5.
2. Assemble Z4, 10 pF.
3. Assemble J5, SMA 50 Ω board edge type SMT female connector (Cinch Connectivity solutions Johnson 142-0761-861).

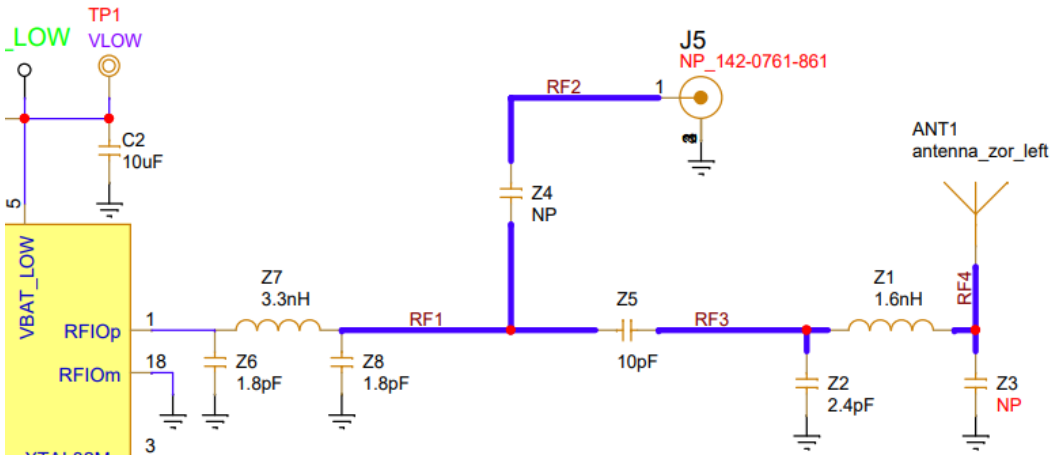

Figure 9. RF section

RF measurements were performed to increase the efficiency of the antenna. The values of the RF matching components are shown in Table 6.

Table 6. RF Components names and values

Component name	Component value	Manufacturer part number
Z1	1.6 nH	LQP15MN1N5W02D
Z2	2.4 pF	GJM1555C1H2R4BB01D
Z3	-	Not populated

5.9 SPI Data Flash Memory (U2)

The DA14535 USB development kit includes an external SPI Data Flash memory (Figure 10).

The selected flash for the DA14535 USB development kit is a 2-Mbit Renesas Semiconductor AT25DF021A-MAHN-T.

The DA14535 USB development kit can also support other types of external SPI flash in USON-8 2 mm × 3 mm, SOIC-8 150 mil, and SOIC-8 208 mil packages (Figure 11).

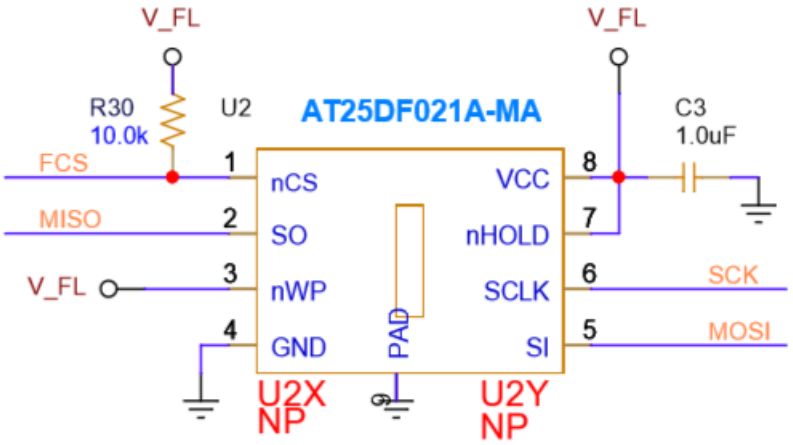

Figure 10. SPI Data Flash

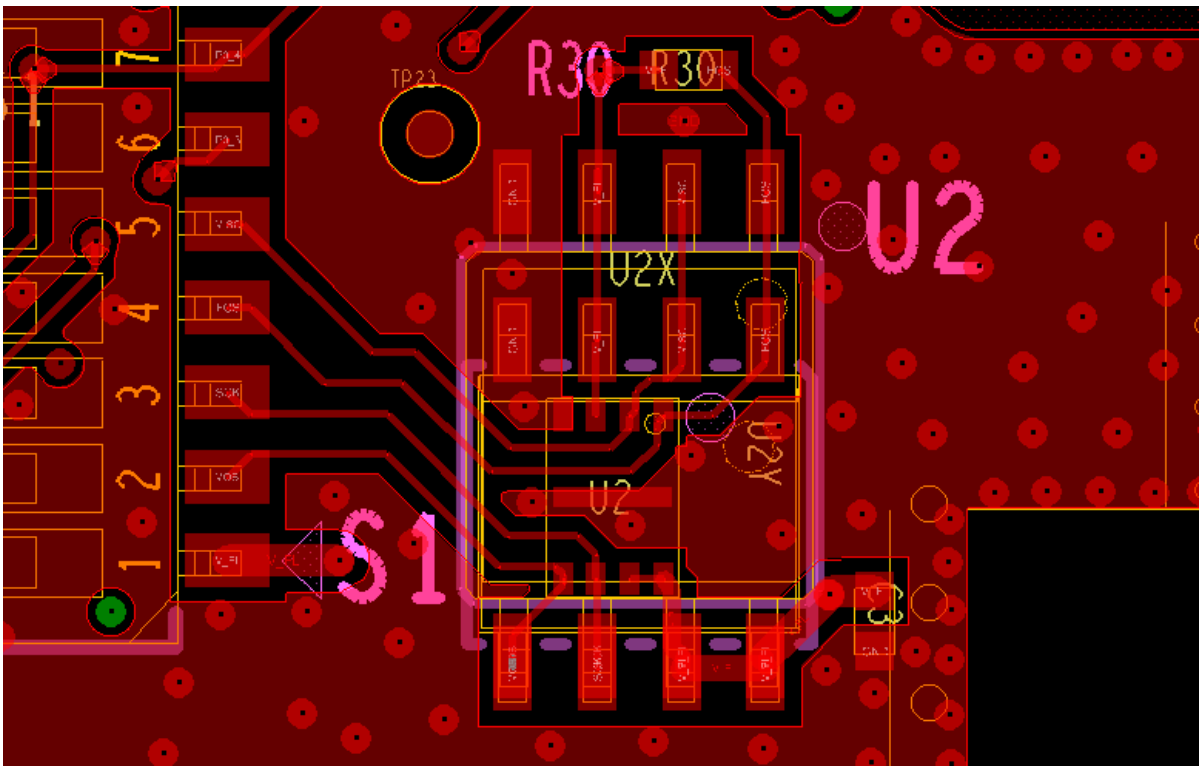

Figure 11. SPI Flash package options

5.10 Reset Circuit

The DA14535 can allocate the power-on-reset input to any GPIO using high or low polarity. This configuration is done by the application software after the boot sequence has finished. However, the only option for a hardware reset before the boot sequence has started is fixed to P0_0 with a high polarity. Because hardware reset is important for development, SW1 is by default connected to P0_0 with high polarity (Figure 12).

There is also an option to connect the button SW1 to GPIO P0_8 through resistor R17.

The JTAG debugger can also drive a hardware reset (T_RST through resistor R48).

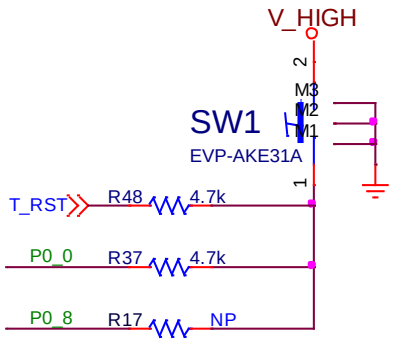

Figure 12. Reset circuit

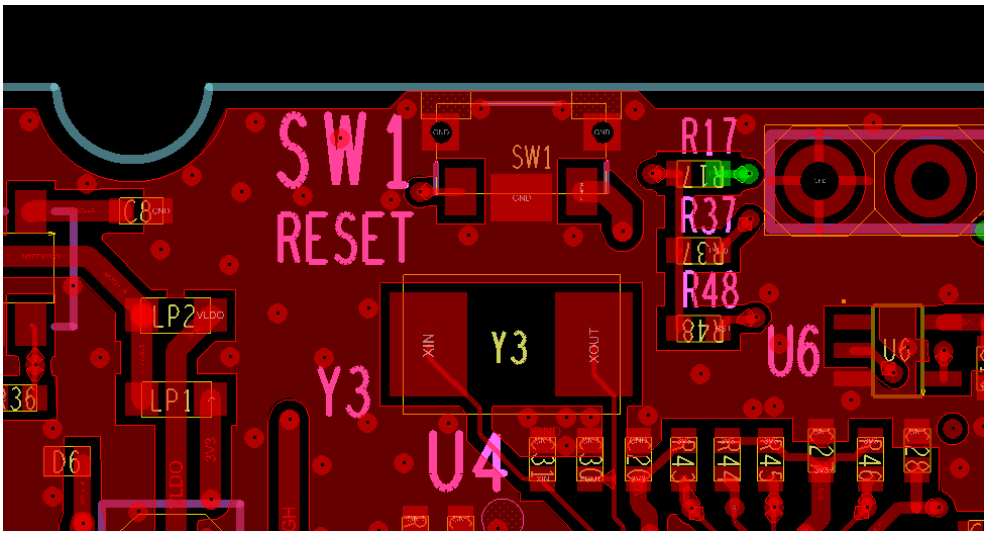

Figure 13. RESET push button (SW1)

5.11 General-Purpose Push Button

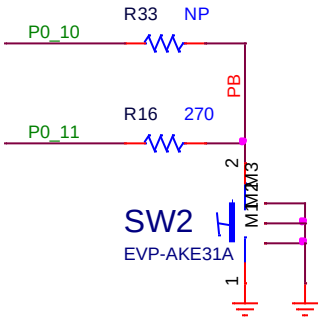

Figure 14. General-purpose push button

The general-purpose push button SW2 is connected by default to GPIO P0_11 and can be connected to P0_10 by soldering resistor R33 (Figure 14).

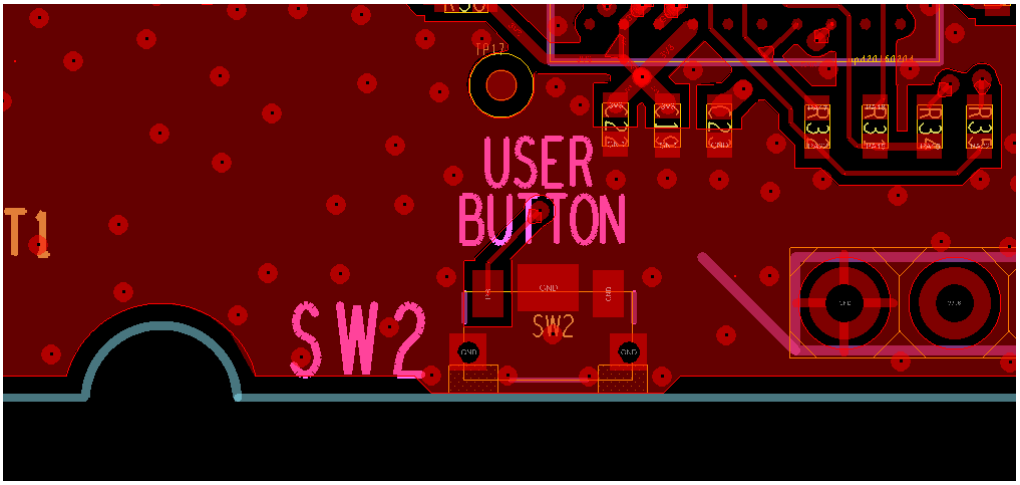

Figure 15. General-purpose push button SW2

5.12 Debugging Port DIP Switch

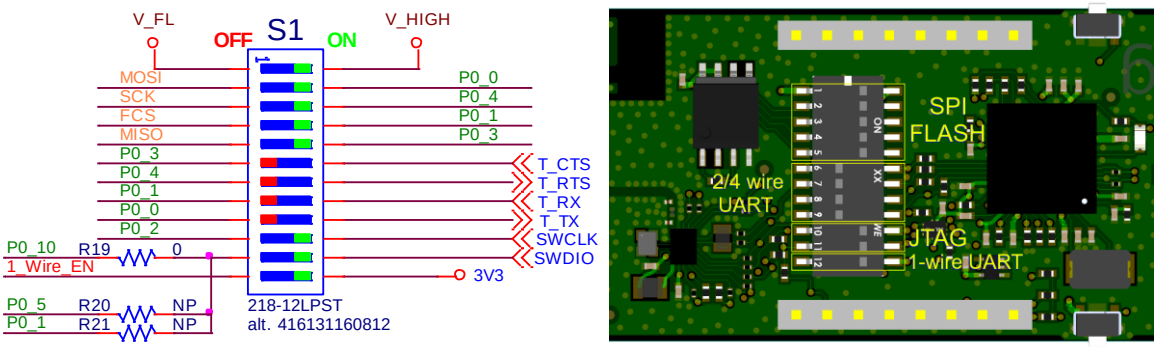

Figure 16. DIP switch configuration

DIP-switch S1 serves a triple purpose (Table 7):

- Allows selection between SPI-Flash and UART as booting options (sharing the same GPIOs).
- Place all switches in the "OFF" position so that the sleep current can be measured accurately.
- Place some switches in the "OFF" position so that the signals can be used for other purposes. For example, if we need more than two analog inputs, these are restricted to use P0_1 or P0_2, assuming the other two options (P0_3 and P0_4) are already utilized.

Table 7. DIP switch configuration

DIP number	DA14535	Related function	Default state
1	VBAT_HIGH (V_{HIGH})	Ext. FLASH power	ON
2	P0_0	QSPI MOSI	ON
3	P0_4	QSPI CLK	ON
4	P0_1	QSPI CS	ON
5	P0_3	QSPI MISO	ON
6	P0_3	UART CTS	OFF
7	P0_4	UART RTS	OFF
8	P0_1	UART Rx	OFF
9	P0_0	UART Tx	OFF
10	P0_2	SWD CLK	ON
11	P0_10	SWD DIO	ON
12	P0_5 (enable)	1-wire UART	ON

5.13 MikroBUS™ Module

The DA14535 USB development kit supports mikroBUS™ modules. Two 8-pin 2.54 mm sockets shall be installed on J3 and J4. A possible female socket type is Sullins Connector Solutions PPTC081LFBN-RC.

Figure 18 shows the notch on the silkscreen which indicates the correct placement for the module. For more information, see *mikroBus™ standard specifications*.

The pin assignment is printed at the bottom of the DA14535 USB kit (Figure 19). A mikroBUS™ module requires a power supply of 5 V, 3.3 V, or both, depending on the module. The voltage for the 5.0 V mikroBUS™ pins is taken from the output of the OVP circuit. The 3.3 V pin is driven from the output of the LDO, which also feeds the debugger section and VHIGH pin on DA14535.

The current measurement point (J2, see Section 5.18) allows the total current flowing from the LDO to DA14535 and any mikroBUS™ peripherals to be measured.

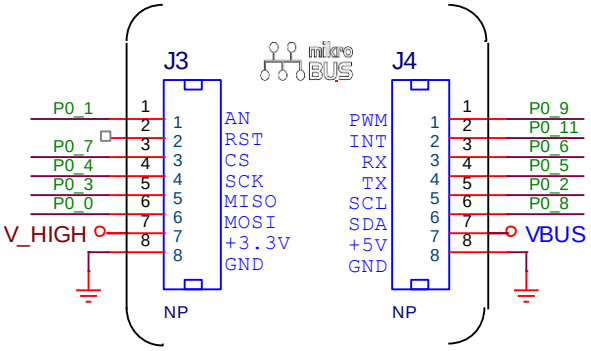

Figure 17. MikroBus™ pin assignment

Figure 18. Guides for proper mikroBus™ click board insertion

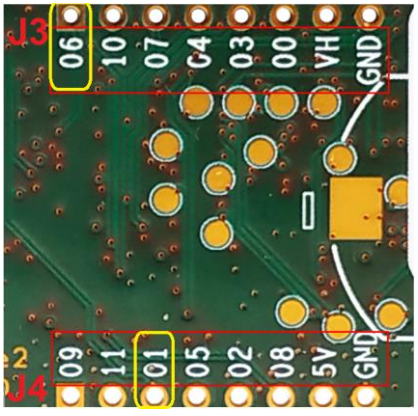

Figure 19. MikroBus™ pin assignment (bottom view)

NOTE
There are wrong labels at the bottom of mikroBus™ headers, (also see Section 5.21): ▪ The label of J3, pin 1 is indicated as P0_6 whereas the pin is connected to pin P0_1 ▪ The label of J4, pin 3 is indicated as P0_1 whereas the pin is connected to pin P0_6

5.14 User Controlled LED

A general-purpose LED (D7, orange) is assigned to GPIO P0_9 (Figure 20). It can be disabled by removing resistor R15.

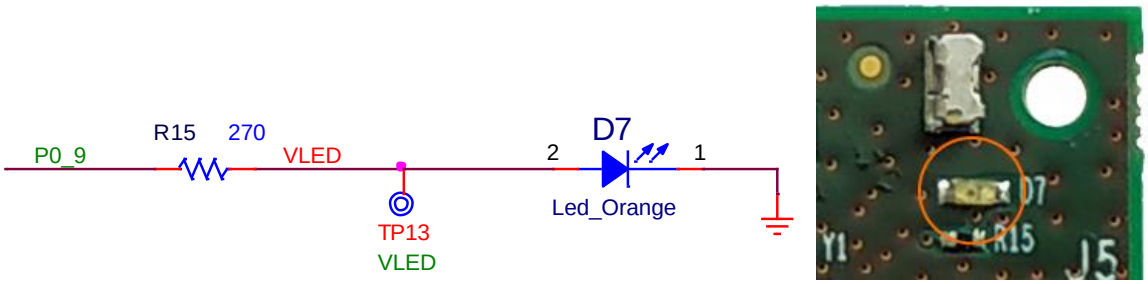

Figure 20. General-purpose LED

5.15 GND Test Point

The ground clip of an oscilloscope can be attached to the test point TP28.

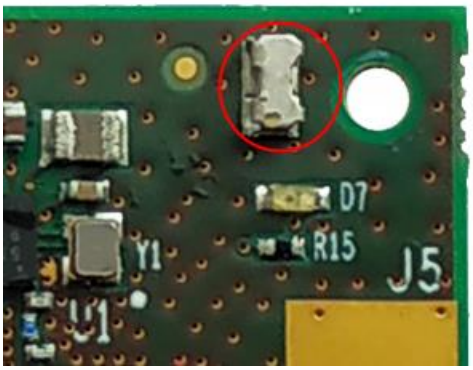

Figure 21. GND support point

5.16 Over Voltage Protection Circuit

The DA14535 USB development kit can be used as a portable standalone device. The power supply can be a power bank or a mobile charger. Figure 22 shows the schematic of the OVP circuit. Overvoltage can be caused not only by the connection of an unsuitable charger, but also by transient voltage surge caused by insertion of a long-length cable. For a normal operation of the DA14535 USB development kit, the input voltage should be between 4.75 V and 5.25 V, as defined in the USB standard, electrical specification.

The OVP circuit can protect the device from transient or permanent overvoltage up to 20 V.

When activated, it disconnects VBUS from VBUS_IN until the condition that caused the activation is corrected. It does not protect the DA14535 USB development kit from an erroneous insertion of power with inverted polarity.

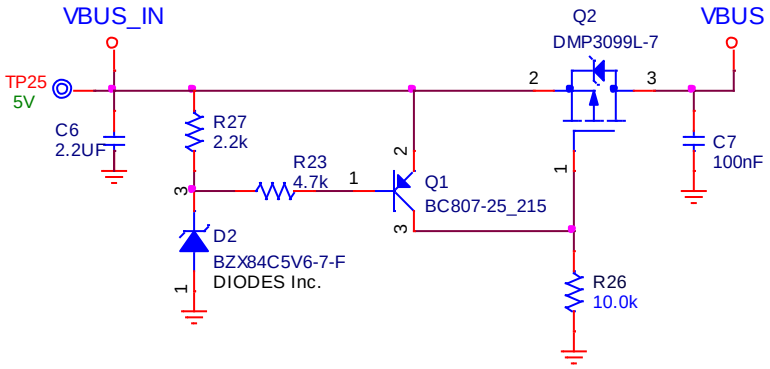

Figure 22. Over voltage protection circuit

5.17 Debug Interface (U4)

Two debugging options (JTAG/UART) are available on the DA14535 SoC and both are implemented with the SAM3U2CA microprocessor (U4) (Figure 23), running the SEGGER J-Link-OB firmware.

The functions served by U4 are:

- SWD debugger interface (SEGGER J-Link-OB)
  - SWCLK connected to DA14535 P0_2
  - SWDIO connected to DA14535 P0_10
- UART connection (for 1-pin, 2-pin, or 4-pin)
- A hardware reset on DA14535 can be asserted through the T_RESETn signal.

The UART port supports hardware flow control (RTS/CTS). It is detected automatically by the J-Link-OB firmware, regardless of the setting on the host machine terminal. The behavior of the UART interface depends on the implementation in the J-Link-OB firmware and is subject to changes by SEGGER Microcontroller with updates to the firmware. For troubleshooting the possible issues with the JTAG Debugger, see the DA14535 datasheet (Ref. [1]). For troubleshooting the possible issues with the serial port, see Ref. [3].

The JTAG operating status is indicated via LED D8 (blinking when there is activity).

The SAM3U2CA (U4) chip is supplied with 3.3 V from U3. A 12-MHz crystal (Y3) is required for the chip operation. U6 inverts T_RESETn to generate an active high signal (T_RST).

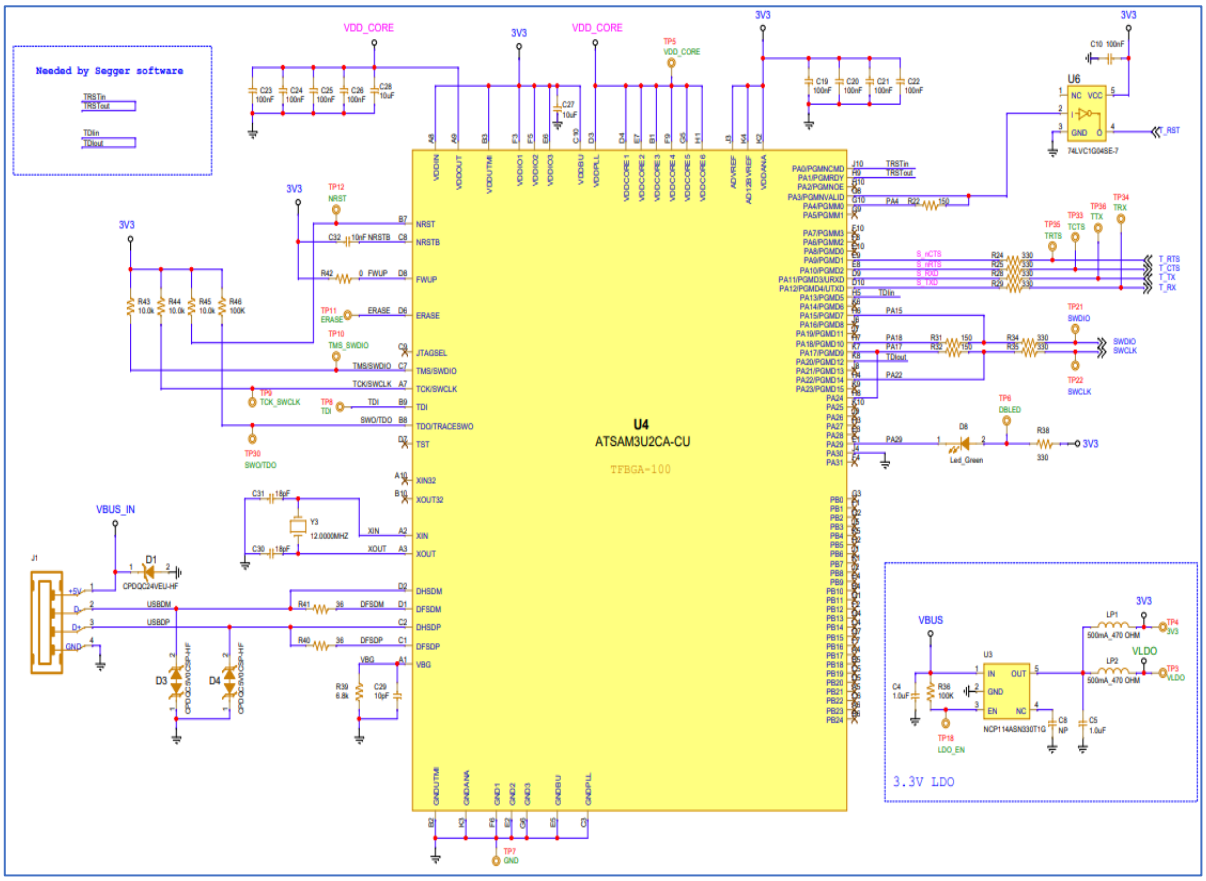

Figure 23. Debugging processor – UART and JTAG interface (U4)

5.18 Power Measurements

If the power consumption of the DA14535 USB development kit needs to be measured accurately, a 3-pin header (for example, a Molex 0878980306) must be placed on J2 and resistor R50 must be removed.

For accurate sleep current measurements, it may be needed to move all segments of the DIP switch S1 to the "OFF" position to eliminate the small leakages through the debug GPIOs.

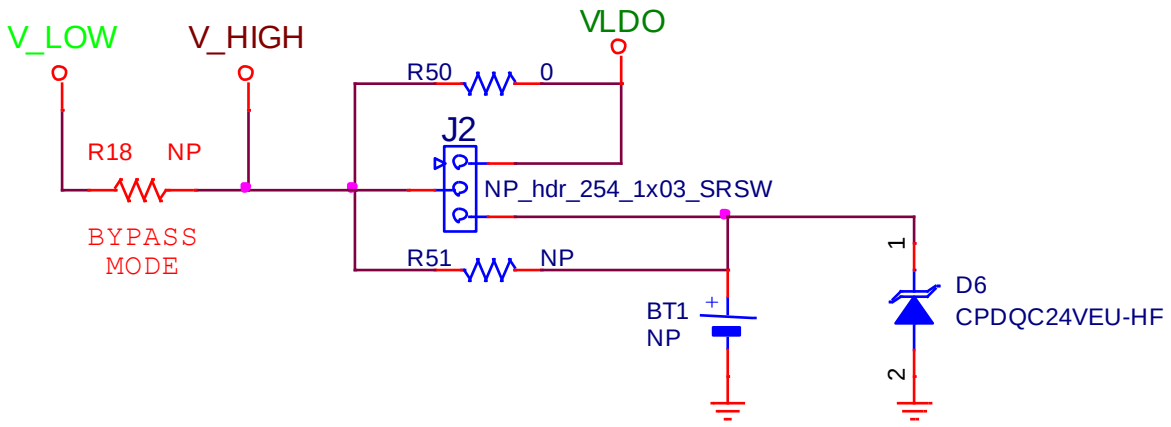

Figure 24. Power measurement header

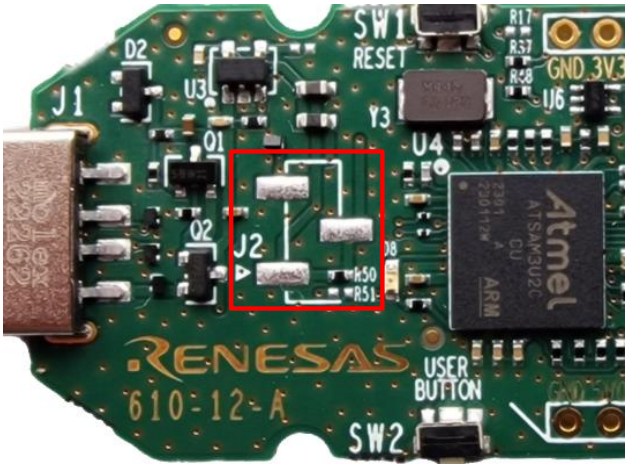

Figure 25. Current measurement header (J2)

An ampere meter can be connected to pin 1 and pin 2 of header J2 for measuring the current supplied by the onboard LDO (U3). The maximum current must not be allowed to rise above ~150 mA which is a total current consumption for DA14535, and all the peripherals connected to V_{HIGH}, because the same LDO also supplies U4 which is rather power-hungry (~115 mA).

Similarly, the ampere meter can be connected to pin 2 and pin 3 of header J2 to measure the current supplied by BT1, if this option is installed.

5.19 Operation from a Wall Adapter or Power Pack

It is possible to power the DA14535 USB development kit from any source with a type-A female powered connector. It may be necessary to remove resistor R48 (Figure 27) to stop any resets issued by the JTAG debugger trying to find a target.

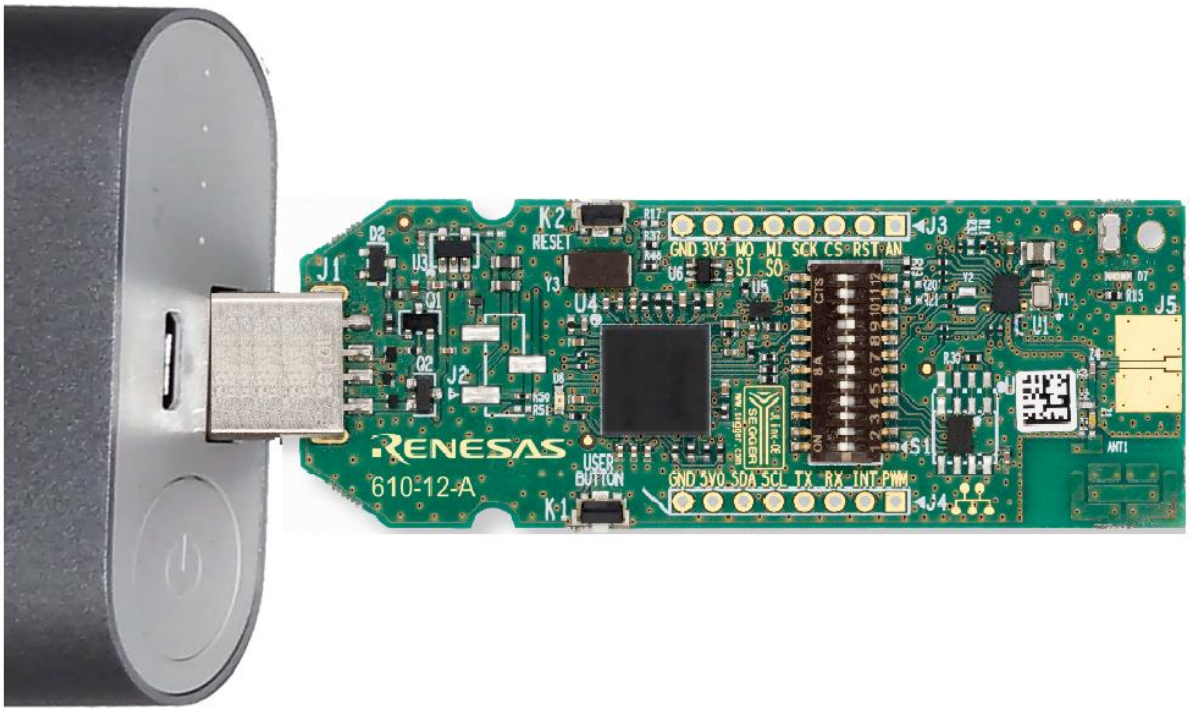

Figure 26. Operation with a battery pack

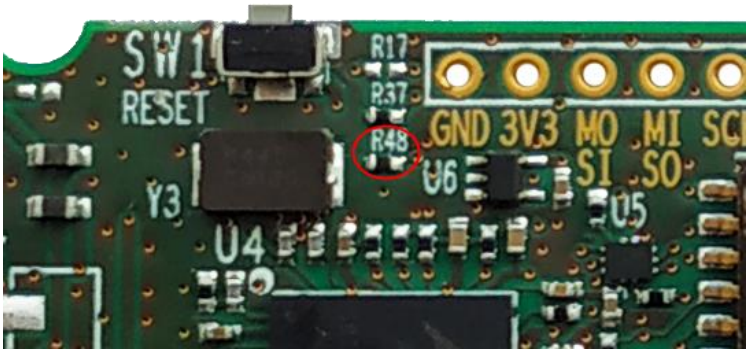

Figure 27. Resistor R48

5.20 Operation from a Coin Cell Battery

It is possible to power the Bluetooth® LE system and maybe a few low-power peripherals on the DA14535 USB development kit with an external battery. A CR2032 battery holder (type BLP2032SM-GTR from MPD or similar) can be soldered at the bottom of the PCB for this purpose.

You must also perform the following steps:

1. Move segments 6 to 12 of the DIP switch S1 to the "OFF" position.
2. If the application does need the SPI flash, move also segments 1 to 5 of the DIP switch S1 to the "OFF" position.
3. Remove R50 and place R51, or move the jumper from position 1-2 to position 2-3, if pin header J2 is installed (Figure 28).

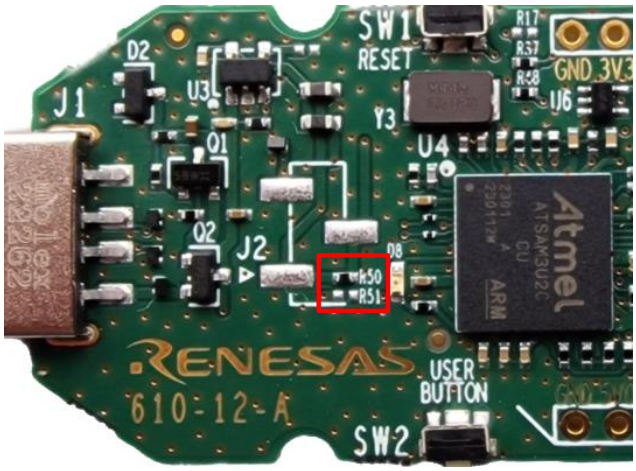

Figure 28. Resistors R50 and R51

5.21 Known Issues

Note that there are wrong labels at the bottom of mikroBus™ headers:

- The label of J3, pin 1 is indicated as P0_6 whereas the pin is connected to pin P0_1.
- The label of J4, pin 3 is indicated as P0_1 whereas the pin is connected to pin P0_6.

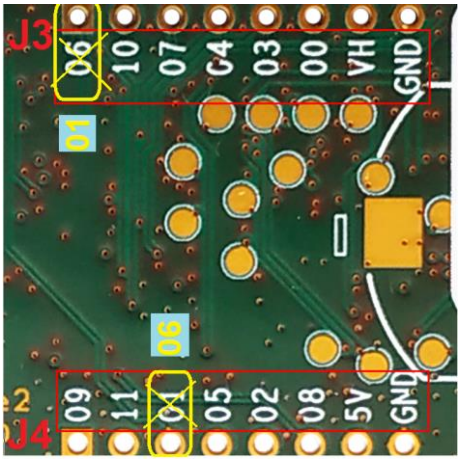

Figure 29. Wrong label on mikroBus™ pin assignment (bottom view)

Appendix A Schematics

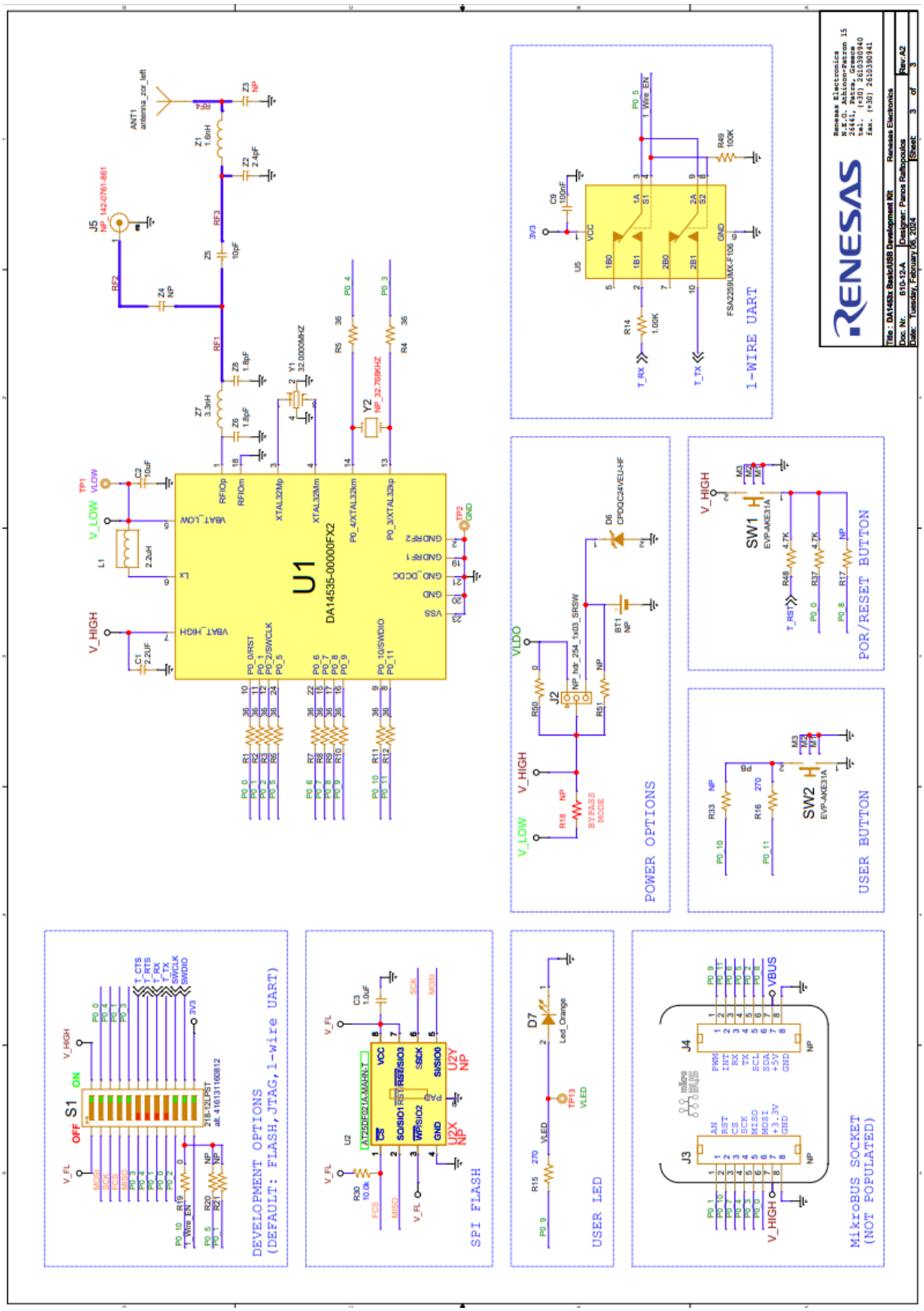

Figure 30. DA14535 SoC and peripherals

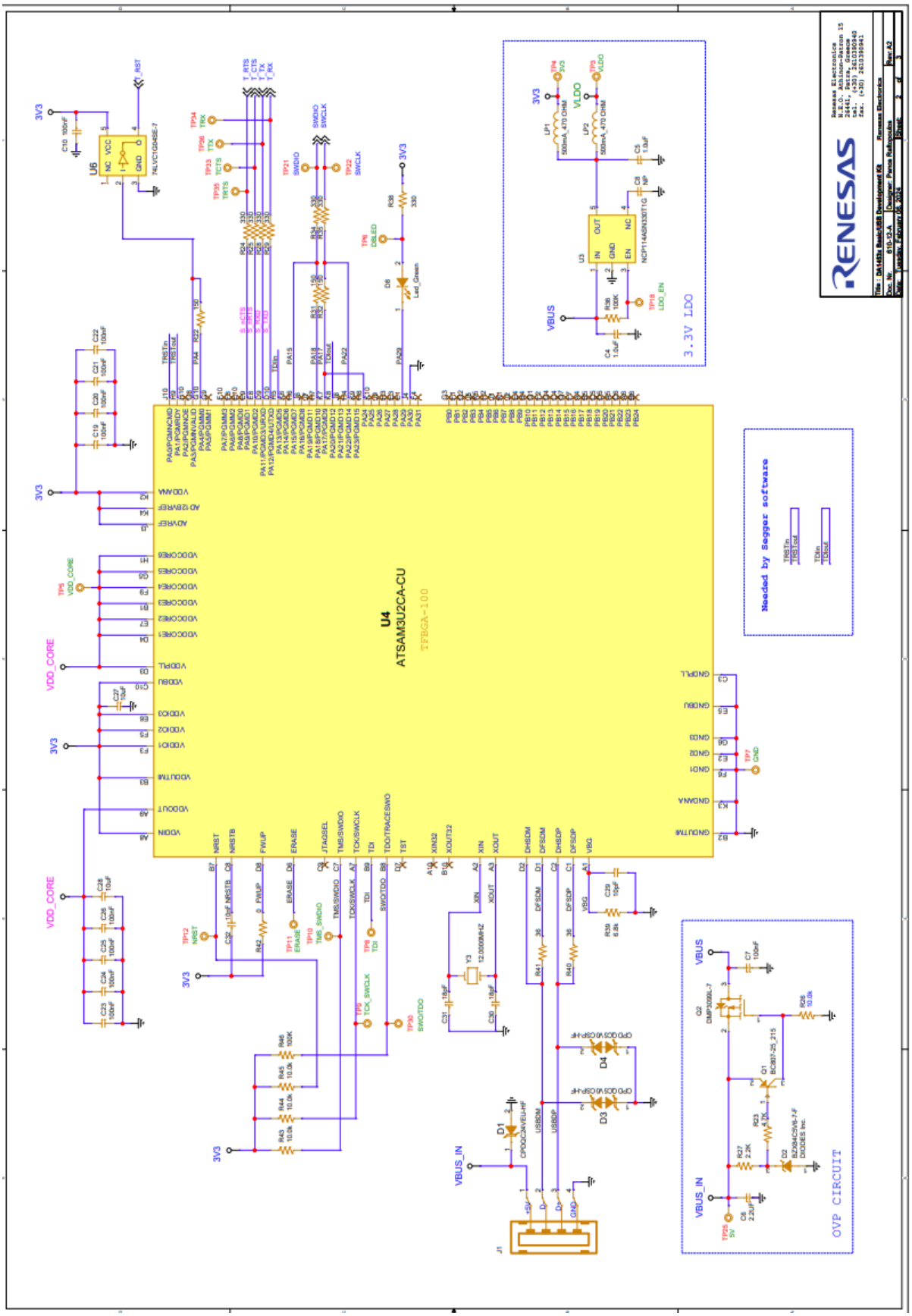

Figure 31. Debug interface (UART/JTAG)

Appendix B Components Placement on PCB

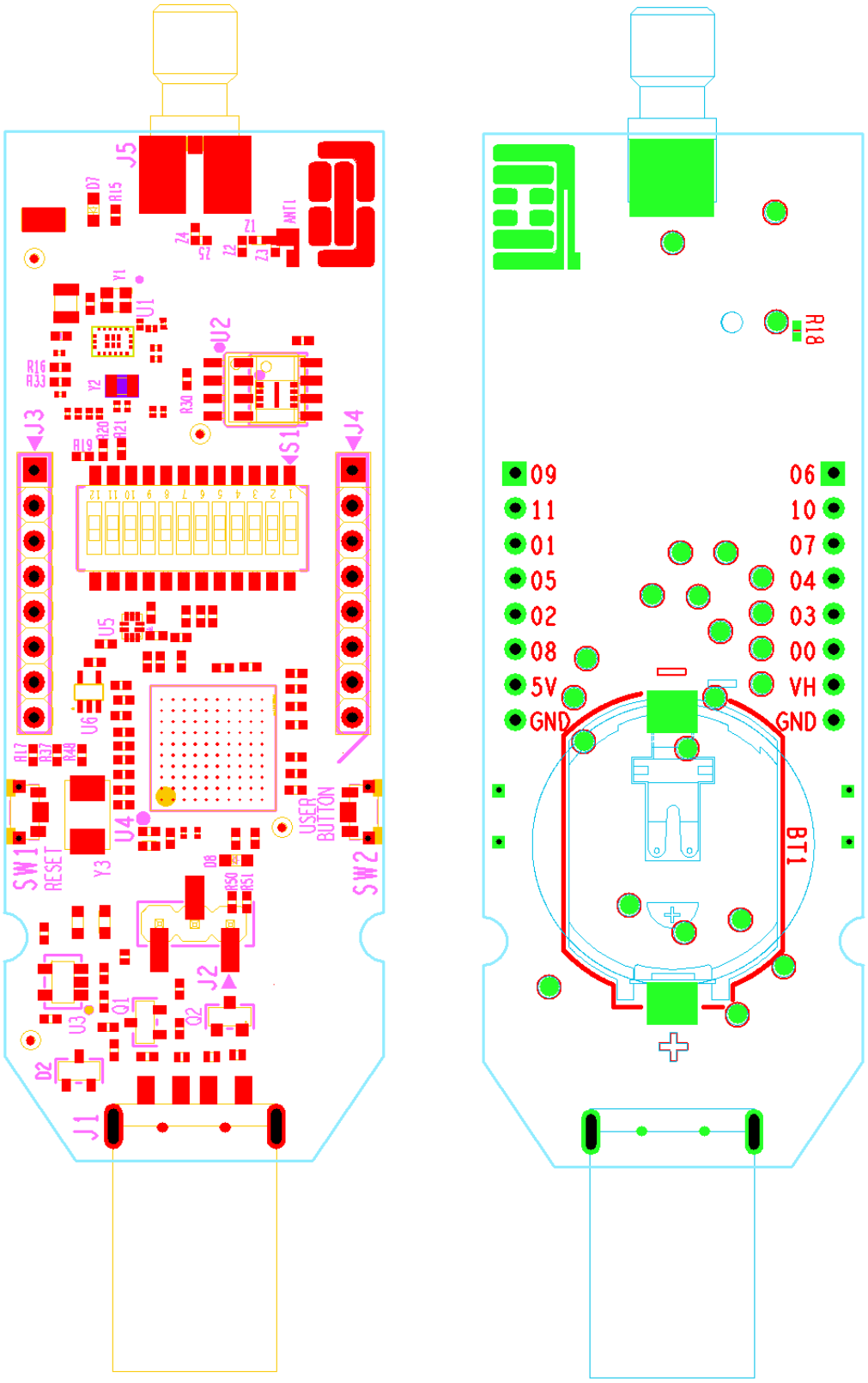

Figure 32. Components placement, top side on the left and bottom side on the right

Appendix C PCB Layer Chart

- Dimensions: 100 mm × 26.5 mm × 11 mm
- Number of layers: 4
- PCB thickness: 1.55 mm
- Material: FR-4
- Solder mask TOP/BOTTOM: Green
- Silkscreen TOP/BOTTOM: White
- Surface finish: Che Ni/Au

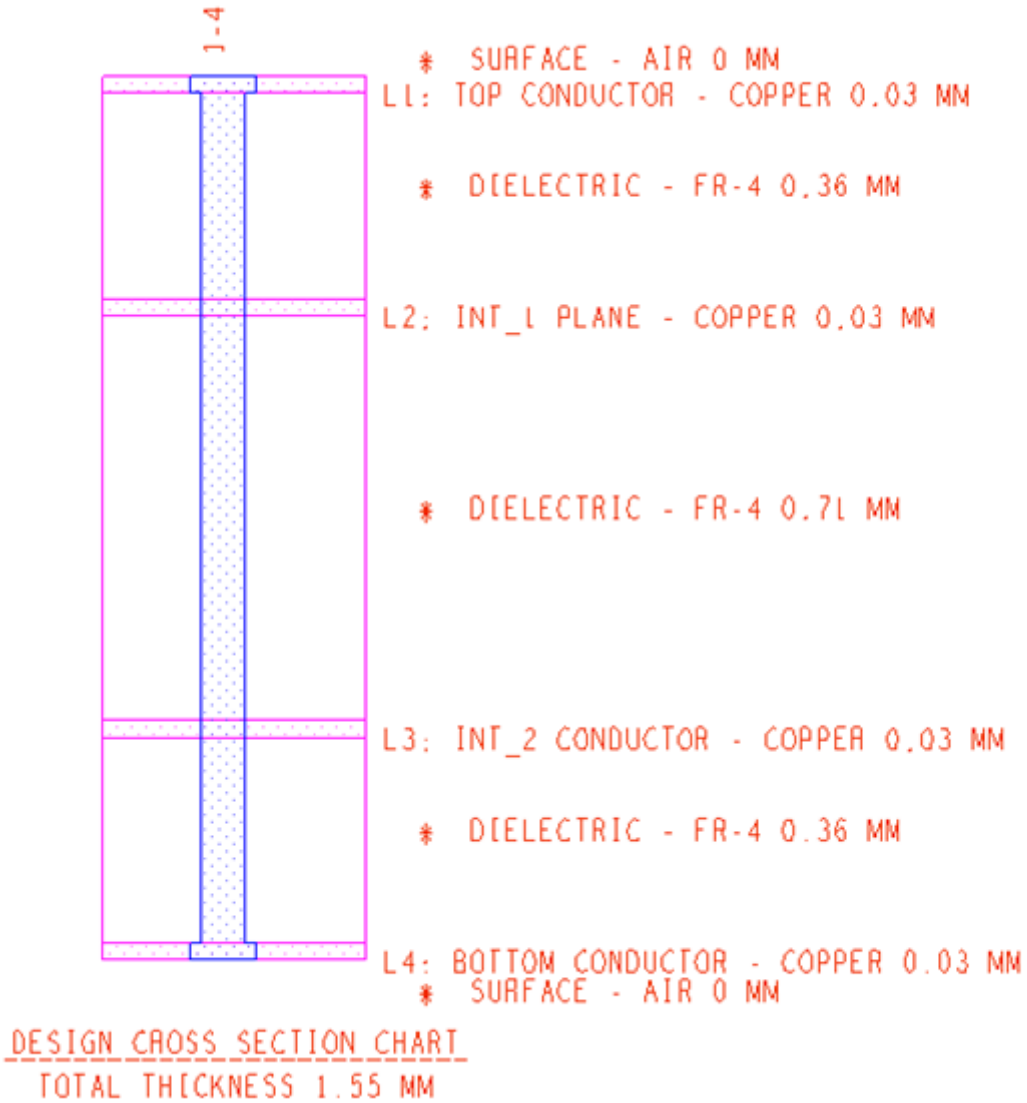

Figure 33. PCB cross section

Appendix D PCBA Label

There is a label stacked on every PCBA. Label provides information for PCBA Production Date and Segger license serial number as follows in Table 8.

Table 8. Information provided on PCBA label

Date Code	<Year> | <week>	2 digits | 2 digits
J-Link debugger serial number	<J-link serial number>	9 digits

Figure 34. Label on PCBA

Appendix E Conformity Assessment

DA14535 USB Kit conforms to laws and regulations that are described in the following subsections.

E.1 FCC Notice (applicable to evaluation kits not FCC-approved)

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

E.2 CE (Radio Equipment Directive 2014/53/EU (RED)) – (Europe)

The DA14535 USB Kit has been tested to RED 2014/53/EU Essential Requirements for Health, Safety, and Radio. The applicable standards are:

- **Radio: EN 300 328 V2.2.2 (2019-07)**
- **Health: EN 62311:2020**
- **Safety: EN 62368-1:2014 + AC:2015 + A11:2017**
- **EMC: ETSI EN 301 489-1 V2.2.3 (2019-11), Draft ETSI EN 301 489-17 V3.2.6 (2023-06)**

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14535 USB Kit is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: www.renesas.com

E.3 UKCA (UK)

The DA14535 USB Kit has been tested and found to comply with the standards harmonized with the regulations listed below according to UKCA-Radio Equipment Regulations 2017-CHAPTER 1 6(1)(a) Health, 6(1)(b) & 6(2). The applicable standards are:

- **Radio: EN 300 328 V2.2.2 (2019-07)**
- **Health: EN 62311:2020**
- **Safety: EN 62368-1:2014 + AC:2015 + A11:2017**
- **EMC: ETSI EN 301 489-1 V2.2.3 (2019-11), Draft ETSI EN 301 489-17 V3.2.6 (2023-06)**

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14535 USB Kit is in compliance with Radio Equipment Regulations 2017. The full text of the UK declaration of conformity is available at the following internet address: www.renesas.com

E.4 MIC (Japan)

The DA14535 USB Kit has received type certification as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

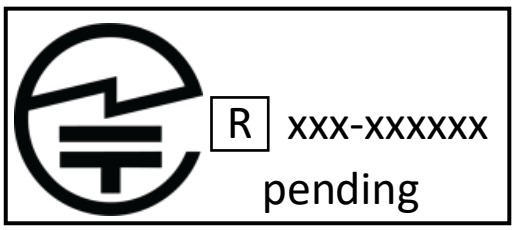

Figure 35. GITEKI mark label

E.5 WEEE Directive (2012/19/EU)

The Waste Electrical and Electronic Equipment Regulations 2013

For customers in the UK and European Union

The WEEE (Waste Electrical and Electronic Equipment)
regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use, the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled, and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back the end of line equipment. Register for this service at https://www.renesas.com/eu/en/support/regional-customer-support/weee.

E.6 RoHS Compliance

Renesas Electronic's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Revision History

Revision	Date	Description
1.0	June 5, 2024	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.