SLG4AF41743

ERM Motor Control

General Description

Silego SLG4AF41743 is a low-power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for use with small devices.

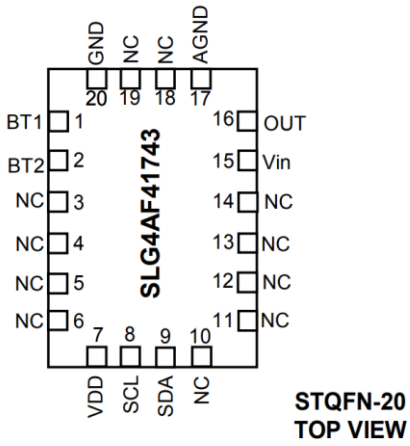
Features

• Low Power Consumption
• Pb-Free / RoHS Compliant
• Halogen-Free
• STQFN-20 Package

Output Summary

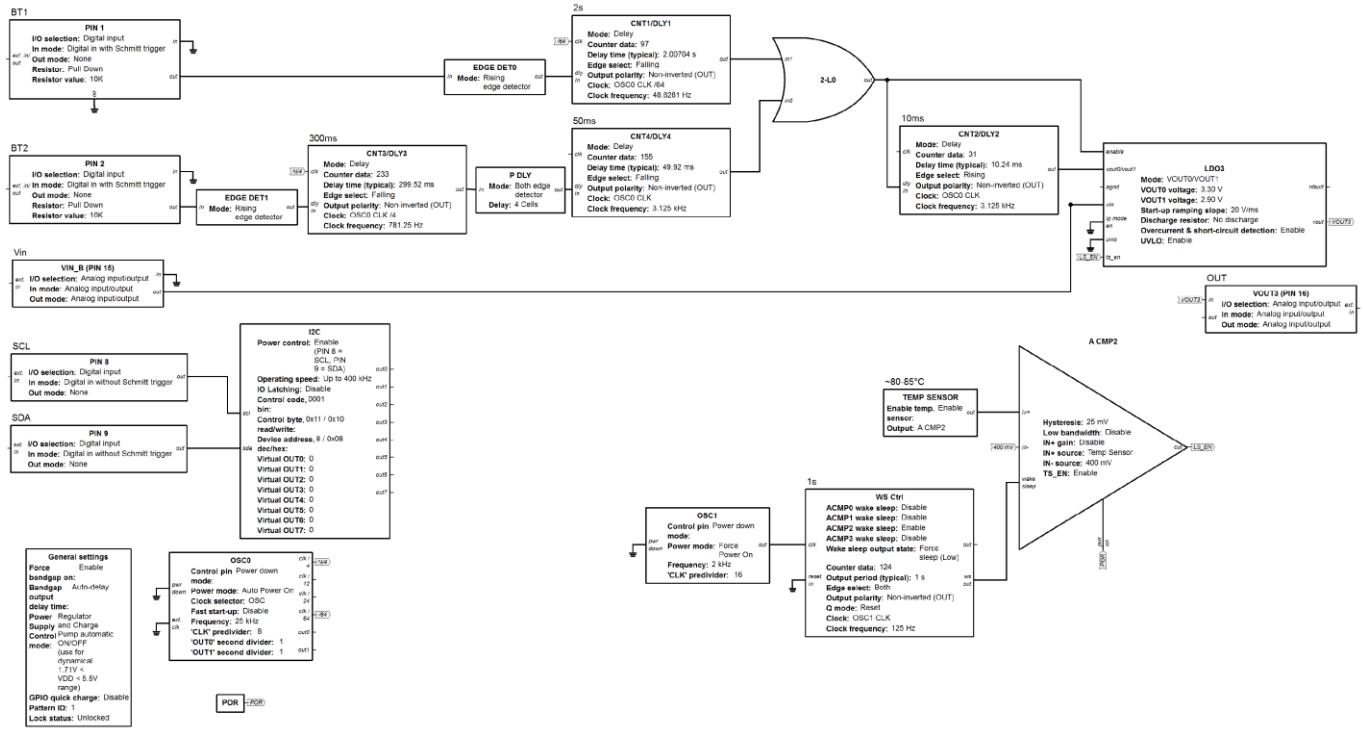
1 Analog output

Pin Configuration



STQFN-20
TOP VIEW

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	BT1	Digital Input	Digital Input with Schmitt trigger
2	BT2	Digital Input	Digital Input with Schmitt trigger
3	NC		Keep Floating or Connect to GND
4	NC		Keep Floating or Connect to GND
5	NC		Keep Floating or Connect to GND
6	NC		Keep Floating or Connect to GND
7	VDD	PWR	Supply Voltage
8	SCL	Digital Input	Digital Input without Schmitt trigger
9	SDA	Digital Input	Digital Input without Schmitt trigger
10	NC		Keep Floating or Connect to GND
11	NC		Keep Floating or Connect to GND
12	NC		Keep Floating or Connect to GND
13	NC		Keep Floating or Connect to GND
14	NC		Keep Floating or Connect to GND
15	Vin	Analog Input/Output	Analog Input/Output
16	OUT	Analog Input/Output	Analog Input/Output
17	AGND	GND	Analog Ground
18	NC		Keep Floating or Connect to GND
19	NC		Keep Floating or Connect to GND
20	GND	GND	Ground

Ordering Information

Part Number	Package Type
SLG4AF41743V	V=STQFN-20
SLG4AF41743VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.3	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and floating outputs	--	TBD	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=3.3V	0.7x VDD	--	VDD	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	0.7x VDD	--	VDD	
		Logic Input, at VDD=5.0V	--	Vlt + 300 mV	--	
		Logic Input with Schmitt Trigger, at VDD=5.0V	--	Vlt + 400 mV	--	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=3.3V	--	--	0.3x VDD	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.3x VDD	
		Logic Input, at VDD=5.0V	--	Vlt - 300 mV	--	
		Logic Input with Schmitt Trigger, at VDD=5.0V	--	Vlt - 400 mV	--	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA

I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
T_{DLY0}	Delay0 Time	At temperature 25°C	--	1	--	s
		At temperature -40°C +85°C (note 1)	--	1	--	
T_{DLY1}	Delay1 Time	At temperature 25°C	--	2	--	s
		At temperature -40°C +85°C (note 1)	-	2	--	
T_{DLY2}	Delay2 Time	At temperature 25°C	--	10	--	ms
		At temperature -40°C +85°C (note 1)	--	10	--	
T_{DLY3}	Delay3 Time	At temperature 25°C	--	300	--	ms
		At temperature -40°C +85°C (note 1)	--	300	--	
T_{DLY4}	Delay4 Time	At temperature 25°C	--	50	--	ms
		At temperature -40°C +85°C (note 1)	--	50	--	
T_{SU}	Start up Time	From VDD rising past PON_{THR}	--	1.3	--	ms

1. Guaranteed by Design.

Chip address

HEX	BIN	DEC
08	0001000	8

Description

This device is created to control ERM motor. It can control motor in 2 ways – 2s vibration pattern (2 s ON) which is controlled by external button (BT1) and 2 short vibrations pattern (50ms ON->250ms OFF->50ms ON) which is controlled by another external button (BT2) and includes following futures: fast start up, overcurrent protection, short-circuit detection and over-temperature protection. Each delay/counter and LDO Vrefs can be reconfigured via I2C.

1.I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte areshown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<xx:yy>.
The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of thedata to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).
With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specificdata byte to be read or written in the command. Figure 1 shows this basic command structure.

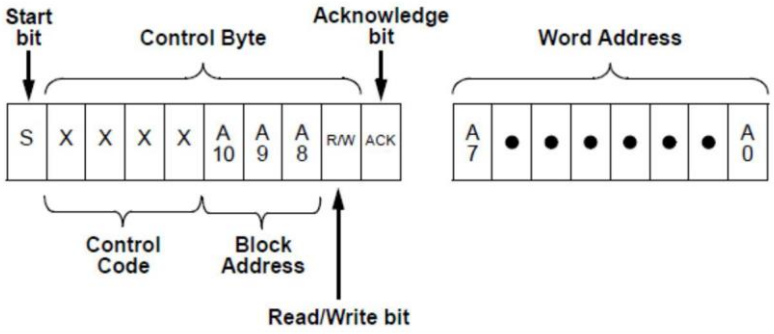


Figure 1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

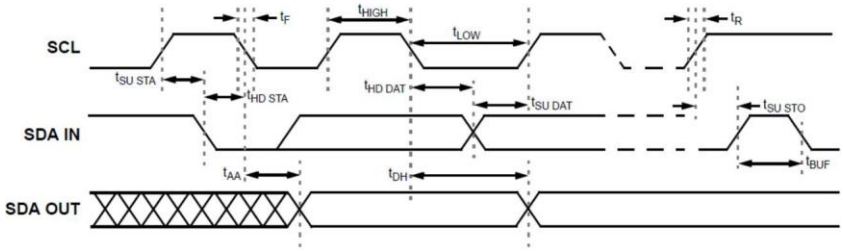


Figure 2. I2C Serial General Timing

3.I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to“0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledgebit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG46533 to the correct data byte to be written. After the SLG46533 sends another Acknowledgebit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG46533 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46533 generates the Acknowledge bit.

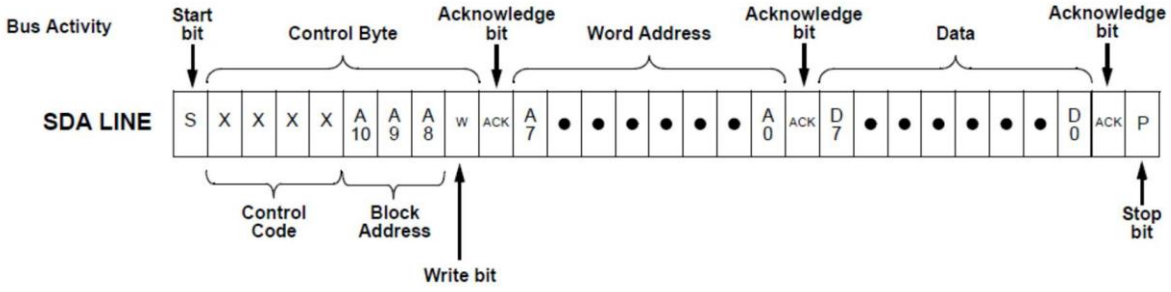


Figure 3. I2C Write Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the sameas the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46533 issues an Acknowledge bit, followed by the requested eight data bits.

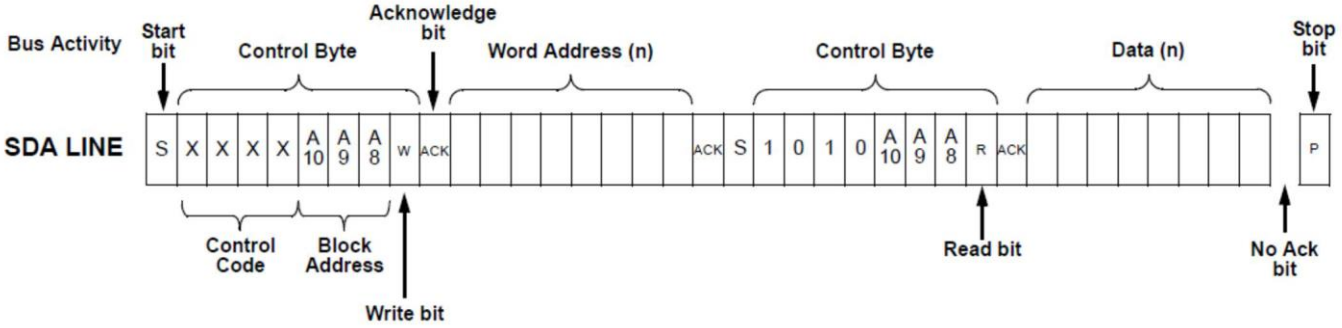


Figure 4. I2C Random Read Command

4. CNT/DLY Settings

The CNT/DLY block registers can be used to change the individual delay times of the delay blocks by changing the control data and the frequency of the clock according to Equation 1. The clock frequency can also be changed by usinga clock pre-divider in the OSC0 block.

Delay time: [(Counter Control Data + 1 + variable) / Frequency], where 0 ≤ variable ≤ 1;

Equation 1: CNT/DLY Time

Address Byte	Register Bit	Block	Function	Range
0xC0	reg<1543:1536>	CNT0	Counter data from 1 to 255 (default setting is 124)	0x01 to 0xFF
0xC1	reg<1551:1544>	DLY1	Counter data from 1 to 255 (default setting is 97)	0x01 to 0xFF
0xC2	reg<1559:1552>	DLY2	Counter data from 1 to 255 (default setting is 31)	0x01 to 0xFF
0xC3	reg<1567:1560>	DLY3	Counter data from 1 to 255 (default setting is 233)	0x01 to 0xFF
0xC3	reg<1567:1560>	DLY4	Counter data from 1 to 255 (default setting is 155)	0x01 to 0xFF

5.LDO Settings

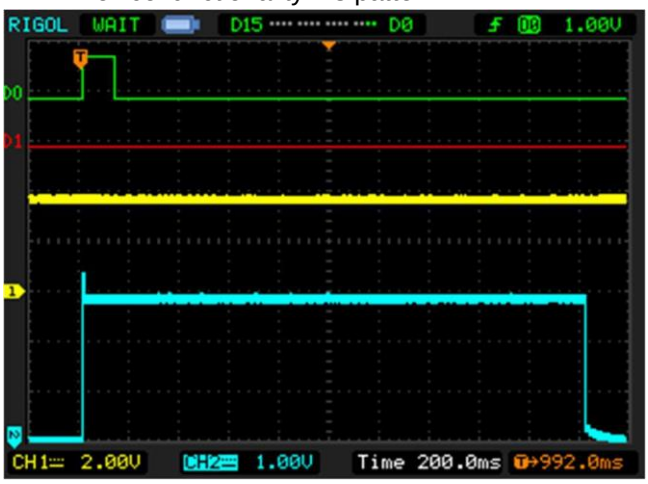
The LDO block is used to control ERM motor with fast start function. After start LDO starts with higher voltage (VOUT0voltage setting) and after 10ms it turns to lower voltage (VOUT1 voltage).

Address Byte	Register Bit	Block	Function	Range
0xCA	reg<1623:1616>	LDO3 VOUT0	LDO VOUT0 ref: 00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:3.70v, 11101:4.00v, 11110:4.30v, 11111:4.35v	0d00000xxx to 0d11111xxx xxx=001
0xE3	reg<1823:1816>	LDO3 VOUT1	LDO VOUT0 ref: 00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:3.70v, 11101:4.00v, 11110:4.30v, 11111:4.35v	0d00000xxx to 0d11111xxx xxx=011

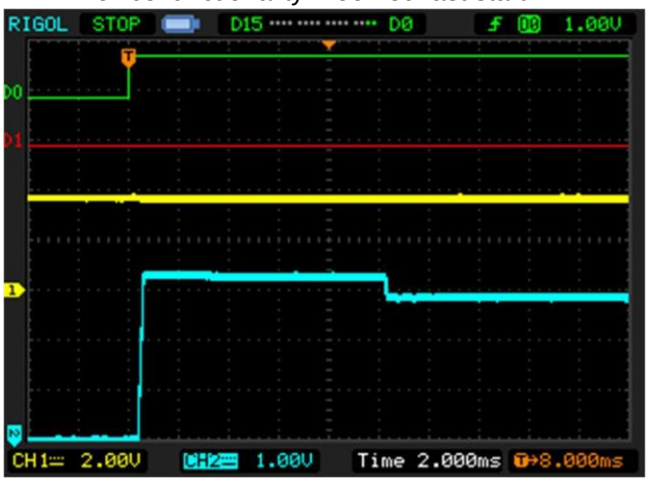
Functionality Waveforms

D0 – PIN#1 (BT1)
D1 – PIN#2 (BT2)
Channel 1 (yellow/top line) – PIN#15 (Vin)
Channel 2 (light blue/2nd line) – PIN#16 (OUT)

1. Device functionality. 2s pattern

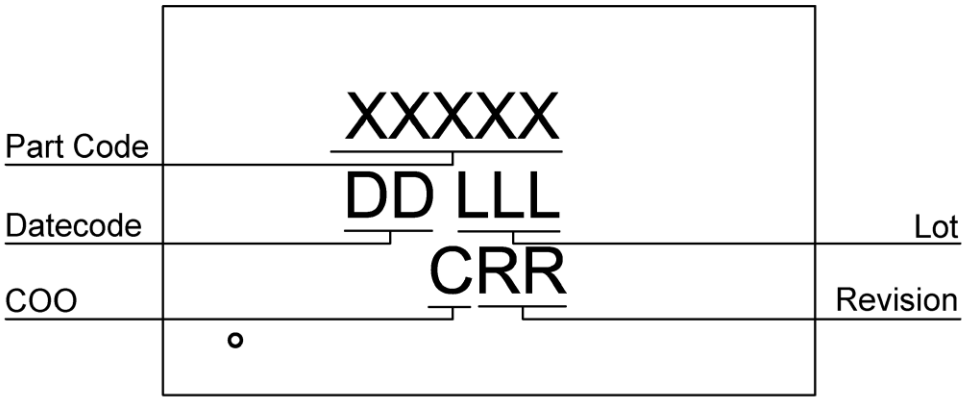


2. Device functionality. Zoomed fast start



3. Device functionality. 2 short vibrations pattern.

Package Top Marking



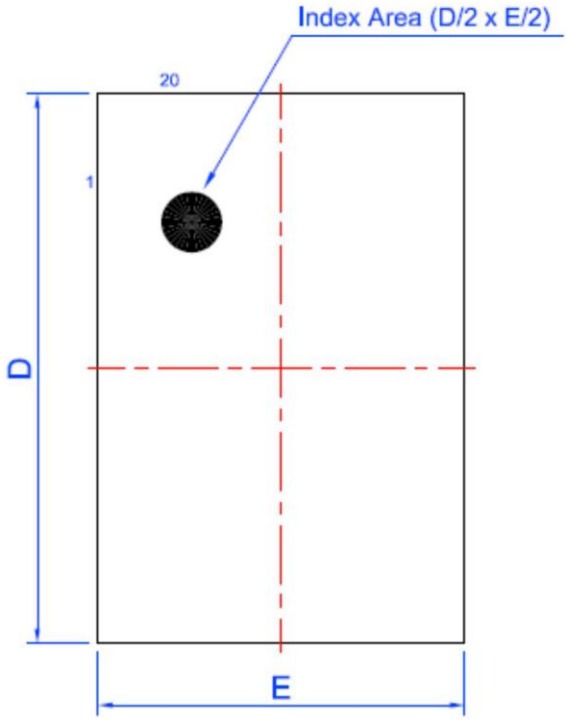
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.10	001	U			03/30/2016

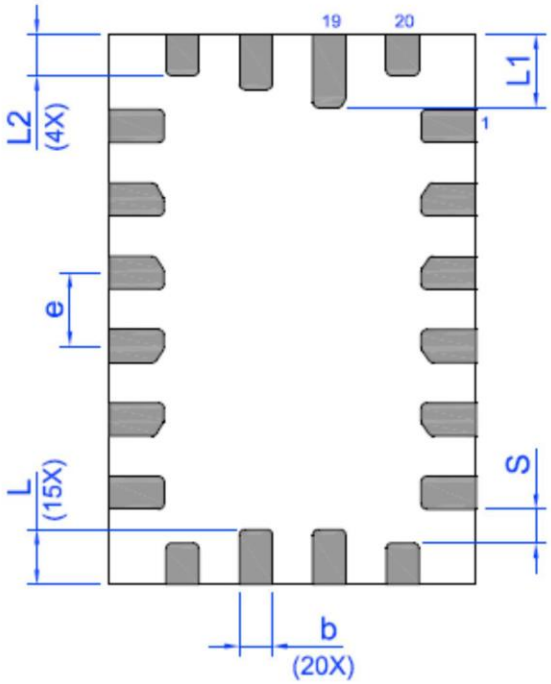
The IC security bit is locked/set for code security for production unless otherwise specified. Revisionnumber is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE



Marking View



BTM View

Side View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			L2	0.175	0.225	0.275
S	0.185 TYP						

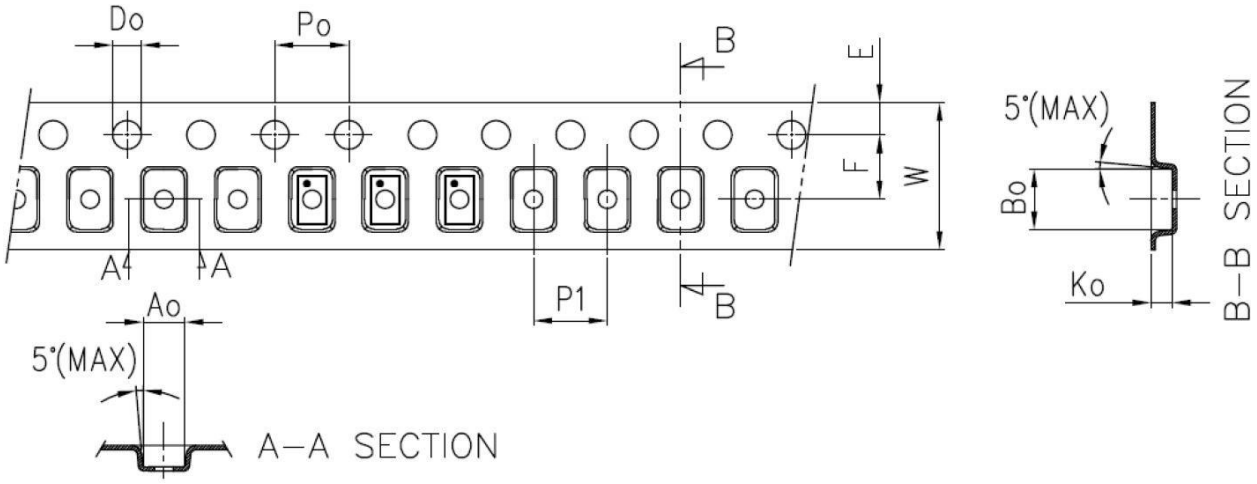
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

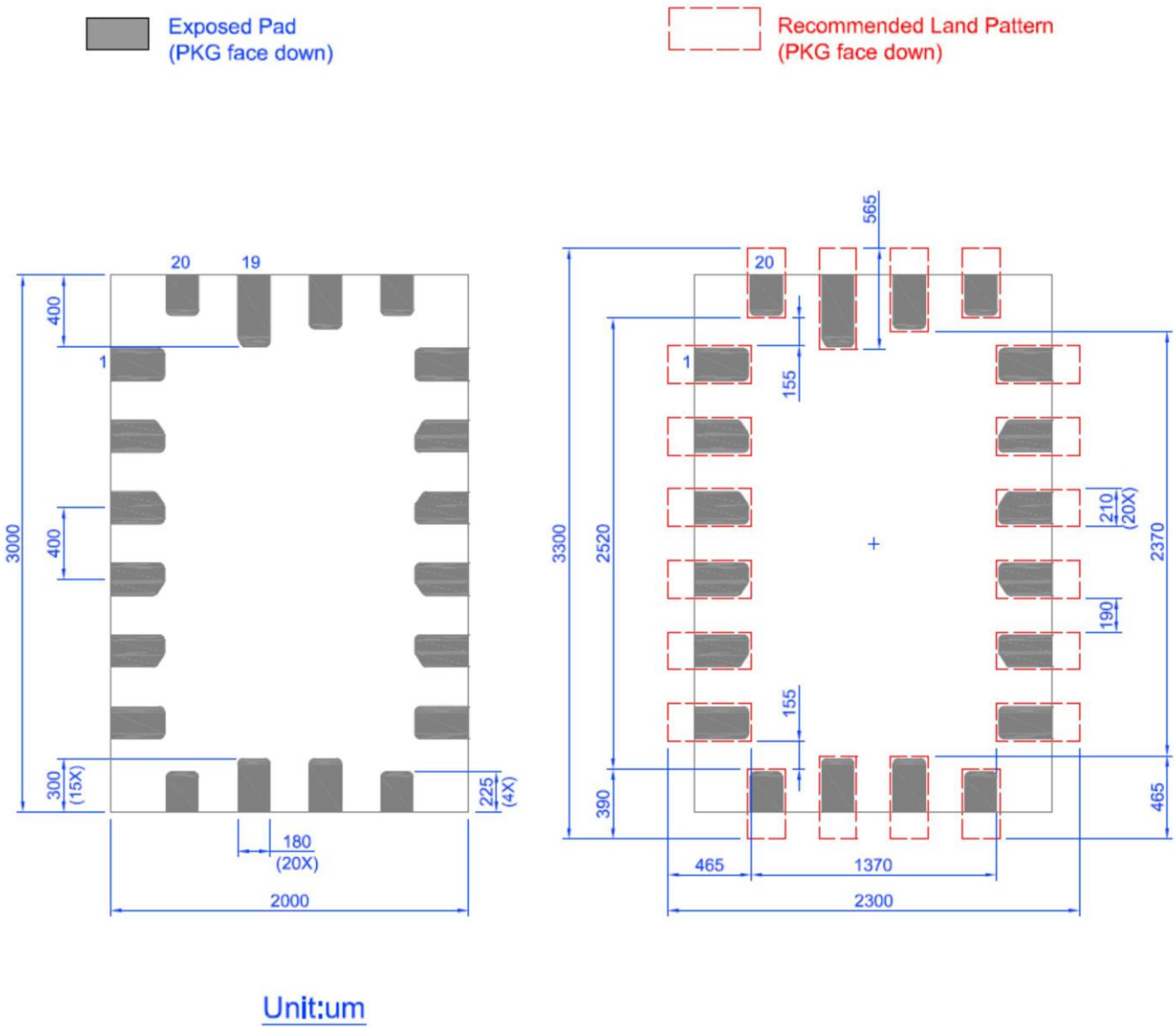
Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal).More information can be found at www.jedec.org.

Recommended Land Pattern



Unit:um

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