ISL5216EVAL Schematics

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Highest Referenced Designators:

C109
J14
JP12
L1
R61
TP11
T9
U17
Y1

Unused Designators:

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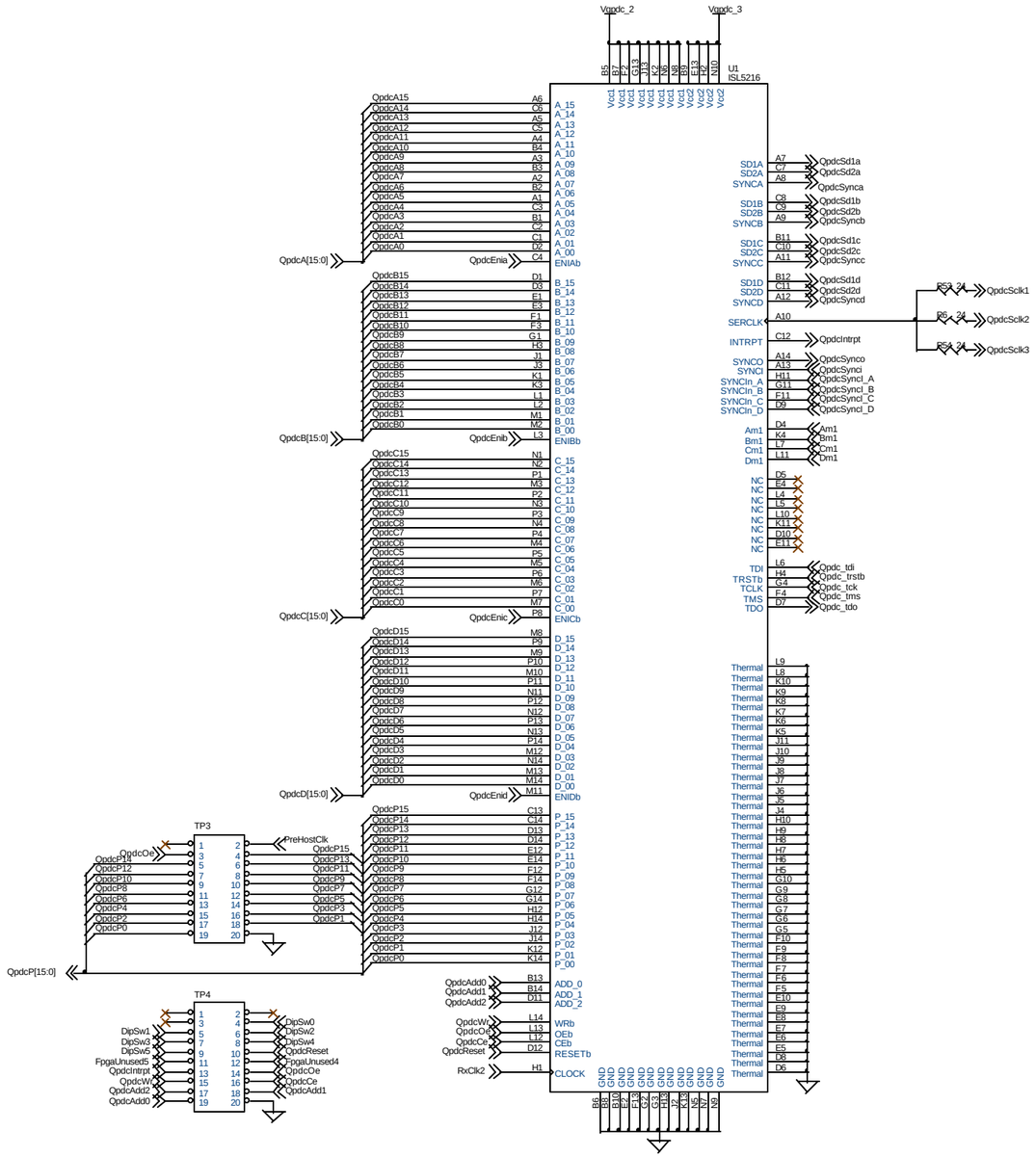

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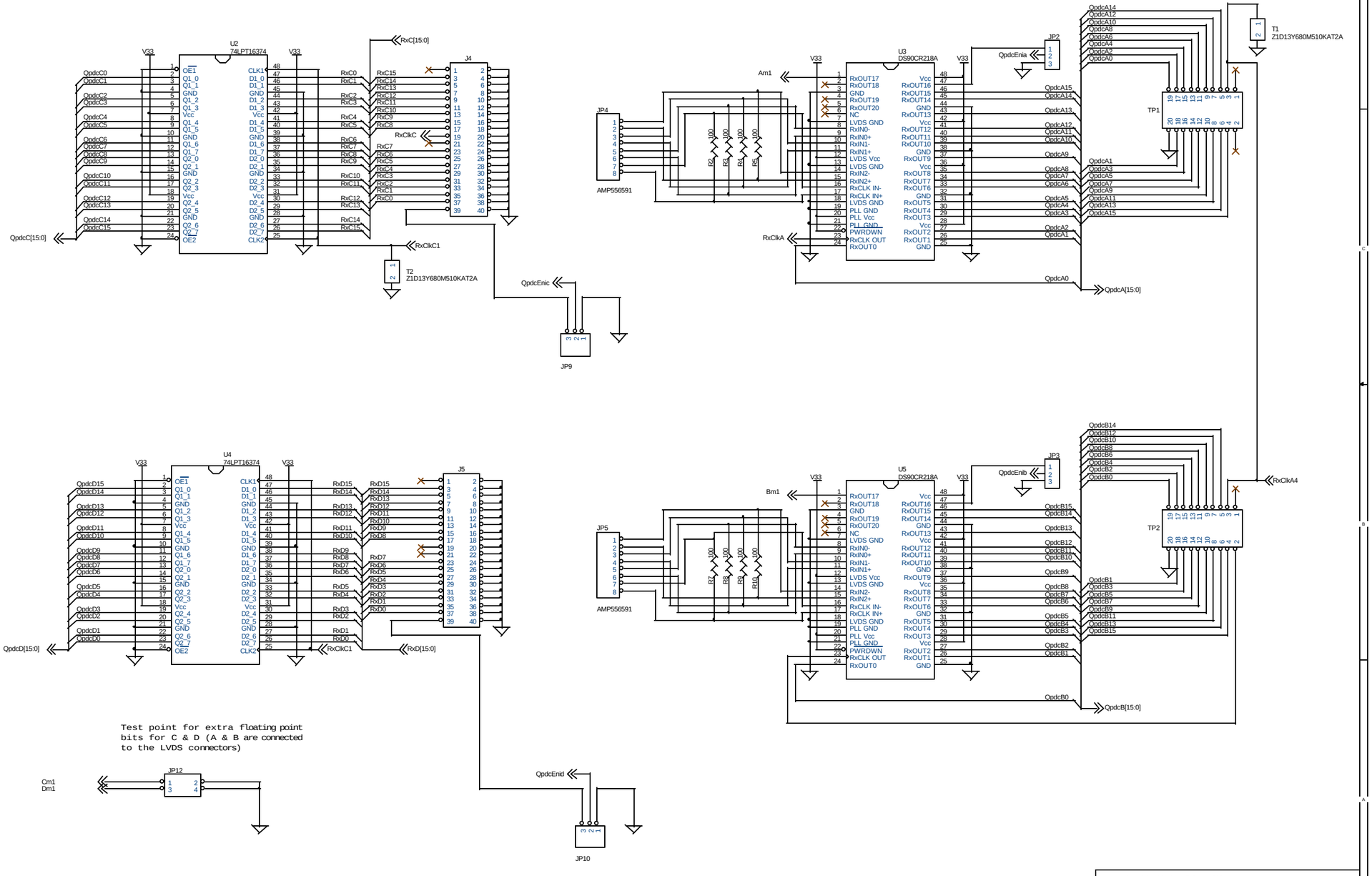

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Title	ISL5216EVAL Schematics - Data Input	
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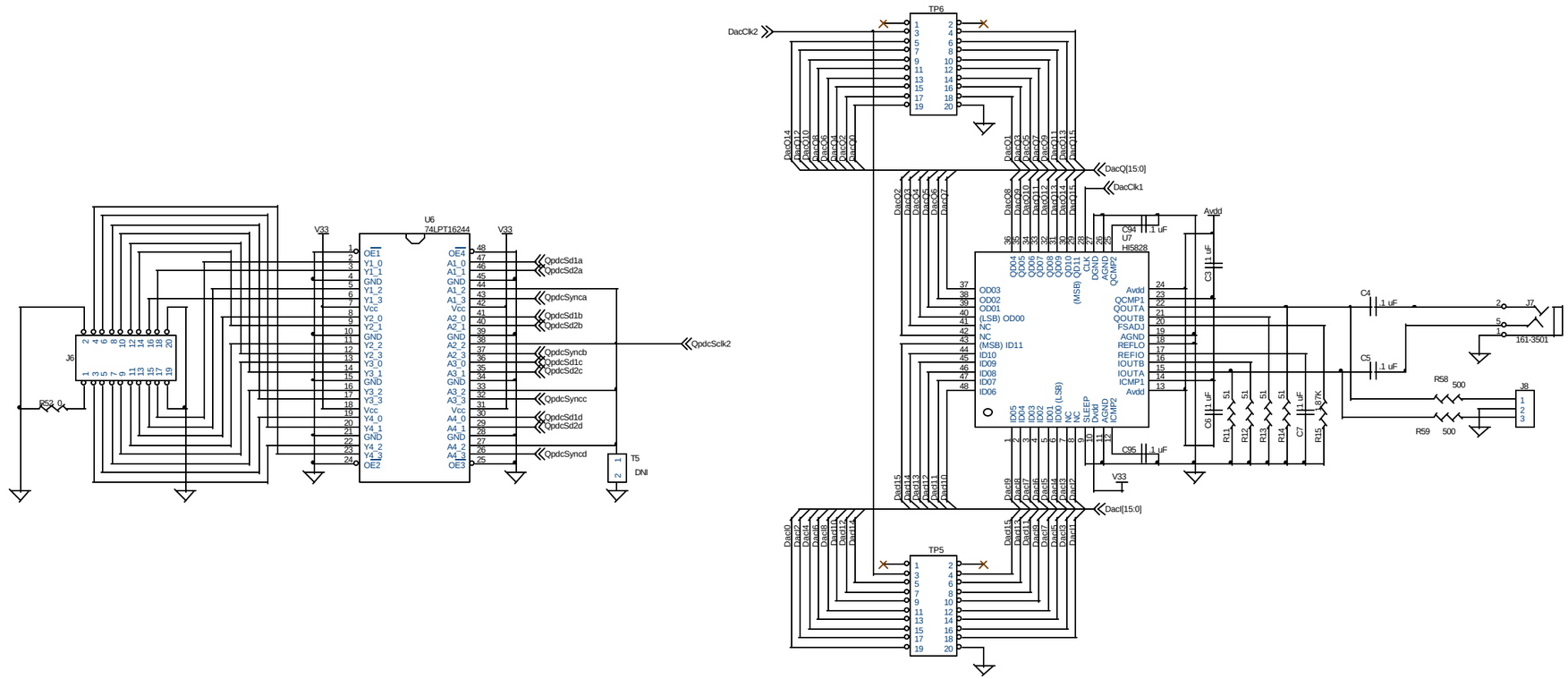

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Title	ISL5216EVAL Schematics - Data Output	
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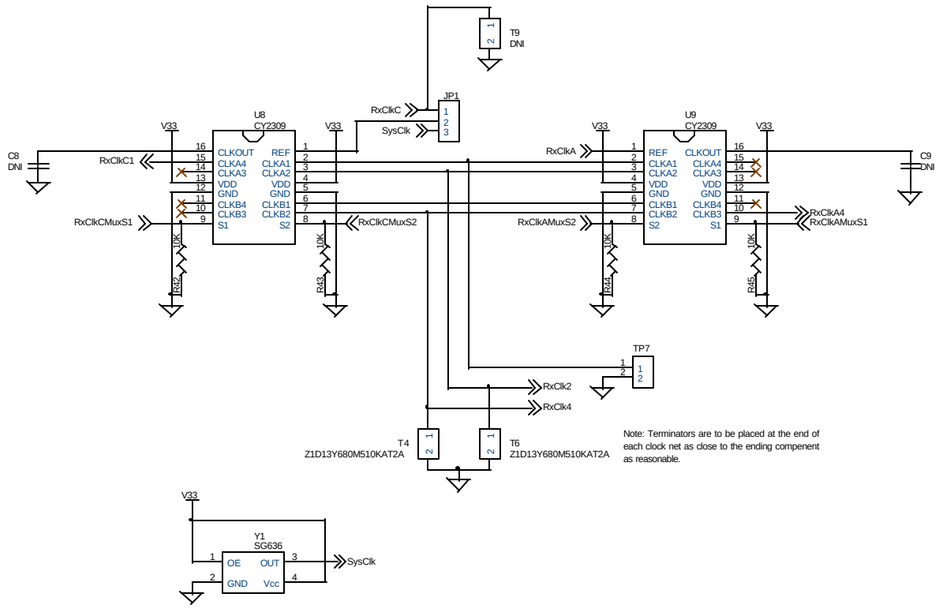

Note: Terminators are to be placed at the end of each clock net as close to the ending compenent as reasonable.

Title	ISL5216EVAL Schematics - Clock Distribution	
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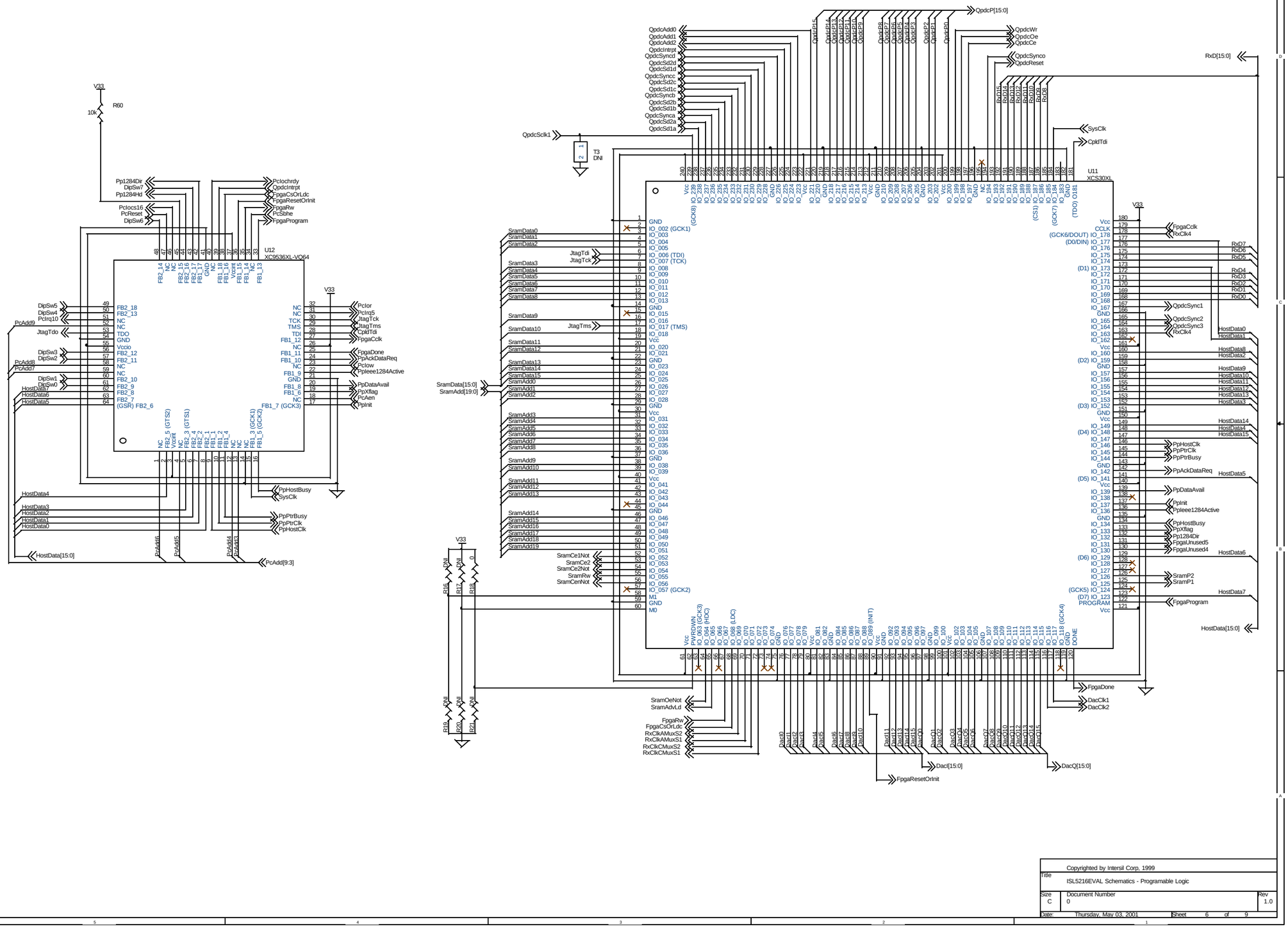
V33
R60
10k
U12
XC9536XL-VQ64
U11
XCS30XL
T3
DNI
QpdcP[15:0]
RxD[15:0]
HostData[15:0]
SramData[15:0]
SramAdd[19:0]
PpHostBusy
SysClk
PpPtrBusy
PpPtrClk
PpHostClk
SramCe1Not
SramCe2
SramCe2Not
SramRw
SramCenNot
SramOeNot
SramAdvLd
FpgaRw
FpgaCsOrLdc
RxClkAMuxS2
RxClkAMuxS1
RxClkCMuxS2
RxClkCMuxS1
FpgaResetOrInit
FpgaDone
DacClk1
DacClk2
DacI[15:0]
DacQ[15:0]
PcAdd[9:3]
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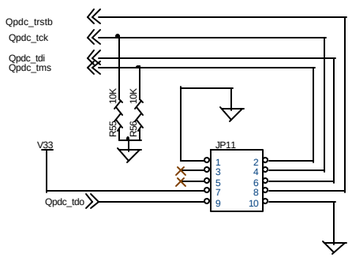
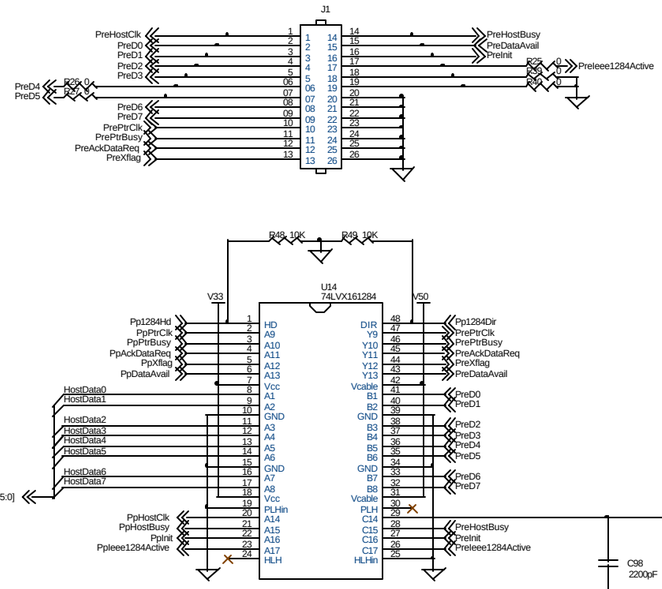
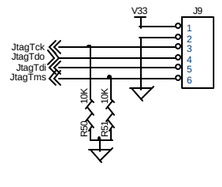
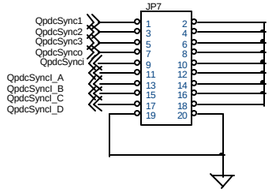
JTAG Header for ISL5216





C98 should be placed between U14 and TP3, basically to have ground connected together with C78





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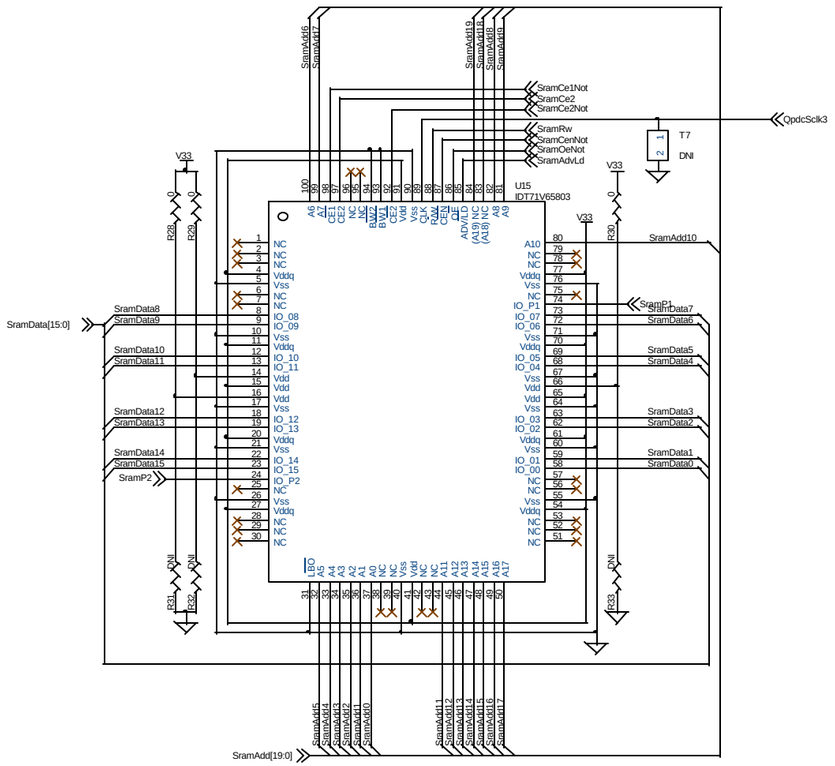

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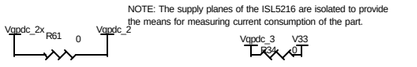
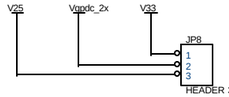
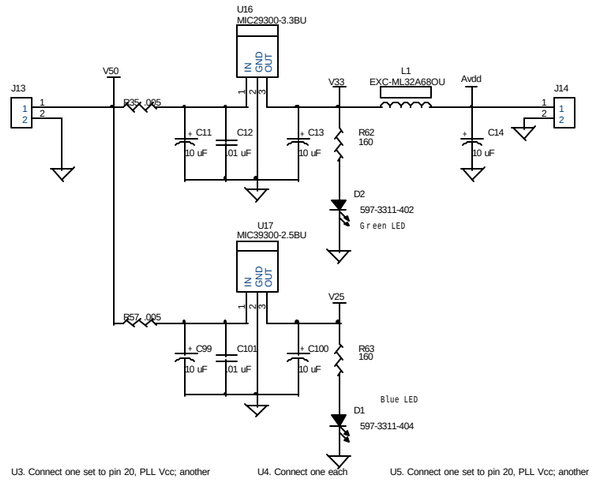


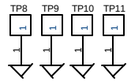
NOTE: The supply planes of the ISL5216 are isolated to provide the means for measuring current consumption of the part.

NOTE: When HSP50216 installed on board, use V33 plane for supply.
When ISL5216 installed on board, use V25 plane for supply.

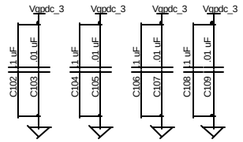


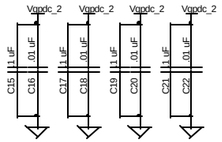
NOTE: This header should NOT be installed on the board. Instead, a zero Ohm resistor, or a piece of wire will go between the supply plane and Vqpdc_2, depending if ISL5216 or HSP50216 are on board.



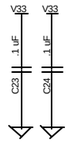


U1. Place sets on each side of the part

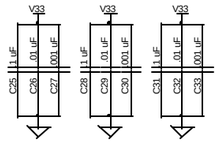




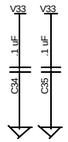
U2. Connect one each to Vcc pins 7 and 31.



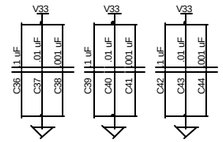
U3. Connect one set to pin 20, PLL Vcc; another to pin 12, LVDS Vcc and the last to pin 36, Vcc



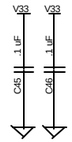
U4. Connect one each to Vcc pins 7 and 31.



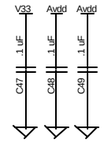
U5. Connect one set to pin 20, PLL Vcc; another to pin 12, LVDS Vcc and the last to pin 36, Vcc



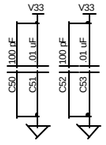
U6. Connect one each to Vcc pins 7 and 31.



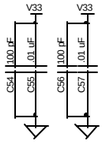
U7. Connect one to Dvdd pin 10 and one each to Avdd pin 13 and 24.



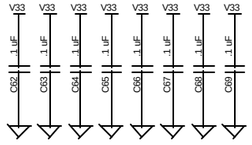
U8. Connect one set to Vdd pin 4 and another to Vdd pin 13. Connect the caps between the pin and the via. Ground each cap with at least one via.



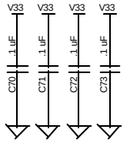
U9. Connect one set to Vdd pin 4 and another to Vdd pin 13. Connect the caps between the pin and the via. Ground each cap with at least one via.



U11. Connect one each to Vcc pins 19, 40, 80, 101, 140, 161, 201 and 222

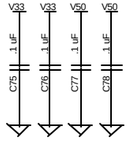


U12. Connect one each to pins 3, 26, 37 and 55.

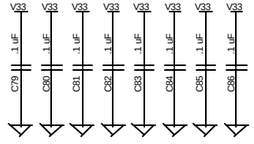


U13. Connect to Vcc near R37 and pin 2

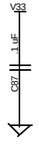
U14. Connect one each to Vcc pins 7 and 18 and one each to Vcable pins 31 and 42.



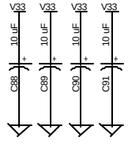
U18. Connect one each to Vdd pins 15, 41, 65 and 91. Connect one each to Vddq pins 4, 27, 54 and 77



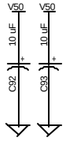
Y1. Connect to Vcc pin 4.



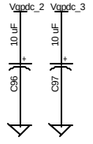
Distibute evenly around V33 supply plane



Distibute evenly around V50 supply plane



Distibute evenly around Vqpdc supply plane



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