VDE Prüfbericht / *VDE Test Report*

Prüfbericht Nr. *Report No.* ..... :	240201-AS6-1
VDE-Aktenzeichen *VDE File No.* ..... :	5007383-4970-0007/240201
Ausstellungsdatum *Date of issue* ..... :	2017-07-28
Labor *Laboratory* ..... :	**VDE** Prüf- und Zertifizierungsinstitut GmbH ***VDE** Testing and Certification Institute*
Adresse *Address* ..... :	Merianstrasse 28 63069 Offenbach/Main; Germany
Prüfort / Adresse *Testing location/ address* ..... :	**VDE** Prüf- und Zertifizierungsinstitut GmbH ***VDE** Testing and Certification Institute* Merianstrasse 28 63069 Offenbach/Main; Germany
Genehmigungsinhaber *Applicant's name* ..... :	Renesas Electronics Europe GmbH
Genehmigungsinhaber Adresse *Applicant's address* ..... :	Karl-Hammerschmidt-Straße 42; 85609 Aschheim-Dornach; Germany
Angewandte Norm(en) *Applied standard(s)* ..... :	DIN EN 60335-1 (VDE 0700-1):2012-10; EN 60335-1:2012 DIN EN 60335-1 Ber.1 (VDE 0700-1 Ber.1):2014-04 EN 60335-1:2012/AC:2014 EN 60335-1:2012/A11:2014 DIN EN 60730-1 (VDE 0631-1):2012-10; EN 60730-1:2011 IEC 60335-1:2010 IEC 60335-1:2010/AMD1:2013 IEC 60335-1:2010/AMD2:2015 IEC 60730-1:2010 IEC 60730-1:2010/AMD1:2015
Art des Prüflings *Test item description* ..... :	Self-Diagnostic Routines for Micro controller Families S1; S3; S5 and S7
Warenzeichen *Trade Mark* ..... :	N/A

Typenbezeichnungen(en)
Type reference(s) ..... :

S1		S3		S5		S7	
cpu_test.c	1.x	cpu_test.c	1.x	cpu_test.c	1.x	cpu_test.c	1.x
CPU_Test_Control.asm	1.x	CPU_Test_Control.asm	1.x	CPU_Test_Control.asm	1.x	CPU_Test_Control.asm	1.x
cpu_test_coupling.c	1.x	cpu_test_coupling.c	1.x	cpu_test_coupling.c	1.x	cpu_test_coupling.c	1.x
CPU_Test_General_High.asm	1.x	CPU_Test_General_High.asm	1.x	CPU_Test_General_High.asm	1.x	CPU_Test_General_High.asm	1.x
CPU_Test_General_Low.asm	1.x	CPU_Test_General_Low.asm	1.x	CPU_Test_General_Low.asm	1.x	CPU_Test_General_Low.asm	1.x
N/A	---	fpu_control.asm	1.x	fpu_control.asm	1.x	fpu_control.asm	1.x
N/A	---	fpu_exten.asm	1.x	fpu_exten.asm	1.x	fpu_exten.asm	1.x
N/A	---	fpu_test_coupling.c	1.x	fpu_test_coupling.c	1.x	fpu_test_coupling.c	1.x
N/A	---	TestFPUCouplingEnd.asm	1.x	TestFPUCouplingEnd.asm	1.x	TestFPUCouplingEnd.asm	1.x
N/A	---	TestFPUCouplingStart_A.asm	1.x	TestFPUCouplingStart_A.asm	1.x	TestFPUCouplingStart_A.asm	1.x
N/A	---	TestFPUCouplingStart_B.asm	1.x	TestFPUCouplingStart_B.asm	1.x	TestFPUCouplingStart_B.asm	1.x
TestGPRsCouplingEnd.asm	1.x	TestGPRsCouplingEnd.asm	1.x	TestGPRsCouplingEnd.asm	1.x	TestGPRsCouplingEnd.asm	1.x
TestGPRsCouplingStart_A.asm	1.x	TestGPRsCouplingStart_A.asm	1.x	TestGPRsCouplingStart_A.asm	1.x	TestGPRsCouplingStart_A.asm	1.x
TestGPRsCouplingStart_B.asm	1.x	TestGPRsCouplingStart_B.asm	1.x	TestGPRsCouplingStart_B.asm	1.x	TestGPRsCouplingStart_B.asm	1.x
N/A	---	TestFPUCouplingS0_S3_A.asm	1.x	TestFPUCouplingS0_S3_A.asm	1.x	TestFPUCouplingS0_S3_A.asm	1.x
N/A	---	TestFPUCouplingS0_S3_B.asm	1.x	TestFPUCouplingS0_S3_B.asm	1.x	TestFPUCouplingS0_S3_B.asm	1.x
N/A	---	TestFPUCouplingS4_S7_A.asm	1.x	TestFPUCouplingS4_S7_A.asm	1.x	TestFPUCouplingS4_S7_A.asm	1.x

N/A	---	TestFPUCouplingS4_S7_B.asm	1.x	TestFPUCouplingS4_S7_B.asm	1.x	TestFPUCouplingS4_S7_B.asm	1.x
N/A	---	TestFPUCouplingS8_S11_A.asm	1.x	TestFPUCouplingS8_S11_A.asm	1.x	TestFPUCouplingS8_S11_A.asm	1.x
N/A	---	TestFPUCouplingS8_S11_B.asm	1.x	TestFPUCouplingS8_S11_B.asm	1.x	TestFPUCouplingS8_S11_B.asm	1.x
N/A	---	TestFPUCouplingS12_S15_A.asm	1.x	TestFPUCouplingS12_S15_A.asm	1.x	TestFPUCouplingS12_S15_A.asm	1.x
N/A	---	TestFPUCouplingS12_S15_B.asm	1.x	TestFPUCouplingS12_S15_B.asm	1.x	TestFPUCouplingS12_S15_B.asm	1.x
N/A	---	TestFPUCouplingS16_S19_A.asm	1.x	TestFPUCouplingS16_S19_A.asm	1.x	TestFPUCouplingS16_S19_A.asm	1.x
N/A	---	TestFPUCouplingS16_S19_B.asm	1.x	TestFPUCouplingS16_S19_B.asm	1.x	TestFPUCouplingS16_S19_B.asm	1.x
N/A	---	TestFPUCouplingS20_S23_A.asm	1.x	TestFPUCouplingS20_S23_A.asm	1.x	TestFPUCouplingS20_S23_A.asm	1.x
N/A	---	TestFPUCouplingS20_S23_B.asm	1.x	TestFPUCouplingS20_S23_B.asm	1.x	TestFPUCouplingS20_S23_B.asm	1.x
N/A	---	TestFPUCouplingS24_S27_A.asm	1.x	TestFPUCouplingS24_S27_A.asm	1.x	TestFPUCouplingS24_S27_A.asm	1.x
N/A	---	TestFPUCouplingS24_S27_B.asm	1.x	TestFPUCouplingS24_S27_B.asm	1.x	TestFPUCouplingS24_S27_B.asm	1.x
N/A	---	TestFPUCouplingS28_S31_A.asm	1.x	TestFPUCouplingS28_S31_A.asm	1.x	TestFPUCouplingS28_S31_A.asm	1.x
N/A	---	TestFPUCouplingS28_S31_B.asm	1.x	TestFPUCouplingS28_S31_B.asm	1.x	TestFPUCouplingS28_S31_B.asm	1.x
TestGPRsCouplingR0_A.asm	1.x	TestGPRsCouplingR0_A.asm	1.x	TestGPRsCouplingR0_A.asm	1.x	TestGPRsCouplingR0_A.asm	1.x
TestGPRsCouplingR0_B.asm	1.x	TestGPRsCouplingR0_B.asm	1.x	TestGPRsCouplingR0_B.asm	1.x	TestGPRsCouplingR0_B.asm	1.x

TestGPRsCouplingR1_R3_A.asm	1.x	TestGPRsCouplingR1_R3_A.asm	1.x	TestGPRsCouplingR1_R3_A.asm	1.x	TestGPRsCouplingR1_R3_A.asm	1.x
TestGPRsCouplingR1_R3_B.asm	1.x	TestGPRsCouplingR1_R3_B.asm	1.x	TestGPRsCouplingR1_R3_B.asm	1.x	TestGPRsCouplingR1_R3_B.asm	1.x
TestGPRsCouplingR4_R6_A.asm	1.x	TestGPRsCouplingR4_R6_A.asm	1.x	TestGPRsCouplingR4_R6_A.asm	1.x	TestGPRsCouplingR4_R6_A.asm	1.x
TestGPRsCouplingR4_R6_B.asm	1.x	TestGPRsCouplingR4_R6_B.asm	1.x	TestGPRsCouplingR4_R6_B.asm	1.x	TestGPRsCouplingR4_R6_B.asm	1.x
TestGPRsCouplingR7_R9_A.asm	1.x	TestGPRsCouplingR7_R9_A.asm	1.x	TestGPRsCouplingR7_R9_A.asm	1.x	TestGPRsCouplingR7_R9_A.asm	1.x
TestGPRsCouplingR7_R9_B.asm	1.x	TestGPRsCouplingR7_R9_B.asm	1.x	TestGPRsCouplingR7_R9_B.asm	1.x	TestGPRsCouplingR7_R9_B.asm	1.x
TestGPRsCouplingR10_R12_A.asm	1.x	TestGPRsCouplingR10_R12_A.asm	1.x	TestGPRsCouplingR10_R12_A.asm	1.x	TestGPRsCouplingR10_R12_A.asm	1.x
TestGPRsCouplingR10_R12_B.asm	1.x	TestGPRsCouplingR10_R12_B.asm	1.x	TestGPRsCouplingR10_R12_B.asm	1.x	TestGPRsCouplingR10_R12_B.asm	1.x
clock_monitor.c	1.x	clock_monitor.c	1.x	clock_monitor.c	1.x	clock_monitor.c	1.x
crc.c	1.x	crc.c	1.x	crc.c	1.x	crc.c	1.x
CRC_Verify.c	1.x	CRC_Verify.c	1.x	CRC_Verify.c	1.x	CRC_Verify.c	1.x
ramtest_march_c.c	1.x	ramtest_march_c.c	1.x	ramtest_march_c.c	1.x	ramtest_march_c.c	1.x
ramtest_march_c_HW.c	1.x	ramtest_march_c_HW.c	1.x	ramtest_march_c_HW.c	1.x	ramtest_march_c_HW.c	1.x
ramtest_march_HW.c	1.x	ramtest_march_HW.c	1.x	ramtest_march_HW.c	1.x	ramtest_march_HW.c	1.x
ramtest_march_x_wom.c	1.x	ramtest_march_x_wom.c	1.x	ramtest_march_x_wom.c	1.x	ramtest_march_x_wom.c	1.x
ramtest_march_x_wom_HW.c	1.x	ramtest_march_x_wom_HW.c	1.x	ramtest_march_x_wom_HW.c	1.x	ramtest_march_x_wom_HW.c	1.x
ramtest_stack.c	1.x	ramtest_stack.c	1.x	ramtest_stack.c	1.x	ramtest_stack.c	1.x
test_adc14.c	1.x	test_adc14.c	1.x	test_adc12.c	1.x	test_adc12.c	1.x

Supplementary Information: If existing the executable code in files for each type of micro controller are identically. Differences are related to commends only. The routines for S7 had been tested under VDE file reference 5007383-4970-0007/223766. Retesting for additional types of micro controllers not needed.	
Bemessungsdaten *Ratings ..... :*	N/A

Zustand des Prüfmusters *Test sample condition* ..... :	☒	Unbeschädigtes Prüfmuster *Non-damaged sample*
	Bemerkung / *Remark:*	*/*
Wareneingang Prüfmuster *Sample entry date* ..... :	2017-07-21	
Datum der Durchführung der Prüfungen *Date (s) of performance of tests*..... :	2017-07-21 to 2017-07-28	

Geprüft und ausgestellt von: *Tested by*..... :		
Name / *Name,* Unterschrift / *Signature* ..... :	J. Schildbach (Autorisierung des Prüfberichtes *Authorization of test report*)	
Funktion / *Function*..... :	Prüfingenieur / Testing engineer	
Überprüft von / *Verified by*..... :		
Name / *Name,* Unterschrift / *Signature* ..... :	P. Fuhl (reviewer)	
Funktion / *Function*..... :	Reviewer	

Fertigungsstätten *Factory(ies)*..... :	Renesas Electronics Europe GmbH; Karl-Hammerschmidt-Straße 42; 85609 Aschheim-Dornbach; Germany

Mögliche Prüfergebnisse *Possible test case verdicts:*	
Prüfung nicht anwendbar *Test case does not apply to the test object* :	*N/A*
Prüfung erfüllt (positiv) *Test object does meet the requirement*..... :	P *(Pass)*
Prüfung nicht erfüllt (negativ) *Test object does not meet the requirement* :	F *(Fail)*

Abschließendes Prüfergebnis ***Final Verdict:***	☒	**P**	☐	**F**
Bemerkung / *Remark*..... :	*/*			

Umgebungsbedingungen (falls relevant) *Environmental conditions (if applicable)*	Umgebungstemperatur *Ambient temperature*	Atmosphärischer Druck *Atmospheric pressure*	Relative Luftfeuchtigkeit *Relative humidity*
Nennwert / *Rated values* ..... :	15-35 °C	860-1060 hPa	30-60 %
Überprüfter Wert / *Verified values* ..... :	N/A	*Bereich* bestätigt von: Deutscher Wetterdienst *Range confirmed by:* *Deutscher Wetterdienst (Meteorological service)*	N/A

Durchgeführte Prüfungen / *Performed tests*			
Abschnitt *Clause*	Prüfanforderungen / *Requirement + Test*	Ergebnis – Anmerkung *Result – Remark*	Beurteilung Verdict
IEC 60335-1:2010			
R	**ANNEX R (NORMATIVE) SOFTWARE EVALUATION**		—
	Programmable electronic circuits requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2 validated in accordance with the requirements of this annex		P
R.1	Programmable electronic circuits using software		—
	Programmable electronic circuits requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2 constructed so that the software does not impair compliance with the requirements of this standard		P
R.2	Requirements for the architecture		—
	Programmable electronic circuits requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2 use measures to control and avoid software-related faults/errors in safety-related data and safety-related segments of the software		P
R.2.1.1	Programmable electronic circuits requiring software incorporating measures to control the fault/error conditions specified in table R.2 have one of the following structures:		—
	- single channel with periodic self-test and monitoring		N/A
	- dual channel (homogenous) with comparison		N/A
	- dual channel (diverse) with comparison		N/A
	Programmable electronic circuits requiring software incorporating measures to control the fault/error conditions specified in table R.1 have one of the following structures:		—
	- single channel with functional test		P
	- single channel with periodic self-test		P
	- dual channel without comparison		N/A
R.2.2	Measures to control faults/errors		—
R.2.2.1	When redundant memory with comparison is provided on two areas of the same component, the data in one area is stored in a different format from that in the other area		N/A

R.2.2.2	Programmable electronic circuits with functions requiring software incorporating measures to control the fault/error conditions specified in table R.2 and that use dual channel structures with comparison, have additional fault/error detection means for any fault/errors not detected by the comparison		N/A
R.2.2.3	For programmable electronic circuits with functions requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2, means are provided for the recognition and control of errors in transmissions to external safety-related data paths		P
R.2.2.4	For programmable electronic circuits with functions requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2, the programmable electronic circuits incorporate measures to address the fault/errors in safety-related segments and data indicated in table R.1 and R.2 as appropriate		P
R.2.2.5	For programmable electronic circuits with functions requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2, detection of a fault/error occur before compliance with clause 19 is impaired		P
R.2.2.6	The software is referenced to relevant parts of the operating sequence and the associated hardware functions		P
R.2.2.7	Labels used for memory locations are unique		P
R.2.2.8	The software is protected from user alteration of safety-related segments and data		P
R.2.2.9	Software and safety-related hardware under its control is initialized and terminates before compliance with clause 19 is impaired		P
R.3	Measures to avoid errors		—
R.3.1	General		—
	For programmable electronic circuits with functions requiring software incorporating measures to control the fault/error conditions specified in table R.1 or R.2, the following measures to avoid systematic fault in the software are applied		—
	Software that incorporates measures used to control the fault/error conditions specified in table R.2 is inherently acceptable for software required to control the fault/error conditions specified in table R.1		N/A
R.3.2	Specification		—
R.3.2.1	Software safety requirements:	Software Id: see table of Type references	P
	The specification of the software safety requirements includes the descriptions listed		P

R.3.2.2	Software architecture		—
R.3.2.2.1	The specification of the software architecture includes the aspects listed - techniques and measures to control software faults/errors (refer to R.2.2); - interactions between hardware and software; - partitioning into modules and their allocation to the specified safety functions; - hierarchy and call structure of the modules (control flow); - interrupt handling; - data flow and restrictions on data access; - architecture and storage of data; - time-based dependencies of sequences and data	Document ref. No: Available on request at manufacturer	P
R.3.2.2.2	The architecture specification is validated against the specification of the software safety requirements by static analysis		P
R.3.2.3	Module design and coding		—
R.3.2.3.1	Based on the architecture design, software is suitably refined into modules		P
	Software module design and coding is implemented in a way that is traceable to the software architecture and requirements		P
R.3.2.3.2	Software code is structured		P
R.3.2.3.3	Coded software is validated against the module specification by static analysis		P
	The module specification is validated against the architecture specification by static analysis		P
R.3.3.3	Software validation		—
	The software is validated with reference to the requirements of the software safety requirements specification		P
	Compliance is checked by simulation of:		—
	- input signals present during normal operation	Self-diagnostic routine only	N/A
	- anticipated occurrences		N/A
	- undesired conditions requiring system action		N/A

TABLE R.1 [e] – GENERAL FAULT/ERROR CONDITIONS						
Component [a]	Fault/error	Acceptable measures [b, c]	Definitions	Document reference for applied measure	Document reference for applied test	Ver-di ct
1 CPU						
1.1 Registers	Stuck at	Functional test, or periodic self-test using either: - static memory test, or - word protection with single bit redundancy	H.2.16.5 H.2.16.6 H.2.19.6 H.2.19.8.2	Documentation available on request at manufacturer		P
1.3 Programme counter	Stuck at	Functional test, or Periodic self-test, or Independent time-slot monitoring, or Logical monitoring of the programme sequence	H.2.16.5 H.2.16.6 H.2.18.10.4 H.2.18.10.2			N/A
2 Interrupt handling and execution	No interrupt or too frequent interrupt	Functional test, or time-slot monitoring	H.2.16.5 H.2.18.10.4			N/A
3 Clock	Wrong frequency (for quartz synchroniz ed clock: harmonics/ sub-harmo nics only)	Frequency monitoring, or time slot monitoring	H.2.18.10.1 H.2.18.10.4	Documentation available on request at manufacturer		P
4. Memory						
4.1 Invariable memory	All single bit faults	Periodic modified checksum, or multiple checksum, or word protection with single bit redundancy	H.2.19.3.1 H.2.19.3.2 H.2.19.8.2	Documentation available on request at manufacturer		P
4.2 Variable memory	DC fault	Periodic static memory test, or word protection with single bit redundancy	H.2.19.6 H.2.19.8.2	Documentation available on request at manufacturer		P
4.3 Addressing (relevant to variable and invariable memory)	Stuck at	Word protection with single bit redundancy including the address	H.2.19.8.2	Covered by 1.1; 3; 4.1; 4.2		P
5 Internal data path						

5.1 Data	Stuck at	Word protection with single bit redundancy	H.2.19.8.2			N/A
5.2 Addressing	Wrong address	Word protection with single bit redundancy including the address	H.2.19.8.2			N/A
6 External communication						
6.1 Data	Hamming distance 3	Word protection with multi-bit redundancy, or CRC – single work, or Transfer redundancy, or Protocol test	H.2.19.8.1 H.2.19.4.1 H.2.18.2.2 H.2.18.14			N/A
6.3 Timing	Wrong point in time	Time-slot monitoring, or scheduled transmission Time-slot and logical monitoring, or comparison of redundant communication channels by either: - reciprocal comparison - independent hardware comparator	H.2.18.10.4 H.2.18.18 H.2.18.10.3 H.2.18.15 H.2.18.3			N/A
	Wrong sequence	Logical monitoring, or time-slot monitoring, or Scheduled transmission	H.2.18.10.2 H.2.18.10.4 H.2.18.18			
7 Input/output periphery						
7.1 Digital I/O	Fault conditions specified in 19.11.2	Plausibility check	H.2.18.13			N/A
7.2 Analog I/O						
7.2.1 A/D and D/A-converter	Fault conditions specified in 19.11.2	Plausibility check	H.2.18.13	Documentation available on request at manufacturer		P
7.2.2 Analog multiplexer	Wrong addressing	Plausibility check	H.2.18.13			N/A
9 Custom chips [d] e.g. ASIC, GAL, gate array	Any output outside the static and dynamic functional specification	Periodic self-test	H.2.16.6			N/A
NOTE A Stuck-at fault model denotes a fault model representing an open circuit or a non-varying signal level. A DC fault model denotes a stuck-at fault model incorporating short circuit between signal lines.						

[a] For fault/error assessment, some components are divided into their sub-functions.
[b] For each sub-function in the table, the Table R.2 measure will cover the software fault/error.
[c] Where more than one measure is given for a sub-function, these are alternatives.
[d] To be divided as necessary by the manufacturer into sub-functions.
[e] Table R.1 is applied according to the requirements of R.1 to R.2.2.9 inclusive.

Supplementary information: */*
To 1.1 Registers: The routines include stuck-at and coupling failure detection. The user can set stuck-at detection only or stuck plus coupling failure detection.
To 1.3 Program Counter In the routines for register test 1.1 a small routine for testing of program counter is integrated. This routine does not cover completely the requirement of standard. It is a support for measures referenced in the table above.

Additional measures	Details	Reference	Verdict
Watch Dog test	Fail Trigger and Rest Source Monitoring	Documentation available on request at manufacturer	P
Stack Pointer Register and Stack Memory Test	Write-read-verify with pattern for register and March-C for memory		P

Additional hardware features	Protection	Reference	Verdict
Ram parity error detection	Stuck at or illegal modification	Documentation available on request at manufacturer	P
Invalid memory access detection function	- any access to undefined memory - write access to invariable memory (ROM) - instruction fetch from special predefined memory areas		P
Window Watch dog with independent clock	- Loss of clock of the arithmetic logical unit (ALU) or the complete micro controller - permanent execution of an undefined endless loop - permanent undefined code execution („runaway software“) - time slot monitoring		P
Port Output Enable	Set PWM outputs to High-Impedance when failure is indicated from external or detected by software		P
On Chip Temperature	Over Temperature for Silicon Device		P
Voltage Monitoring	Under voltage detection to avoid unstable operation		P

IEC 60730-1:2010			
Clause	Requirement + Test	Result - Remark	Verdict
H.6	Classification, additions		—
H.6.18	Class of control function (A, B,C)		—
H.7	Information in addition to Table 1 provided:		—
	66 - Software sequence documentation; clause: H.11.12.2.9; method: X		P
	67 - Program documentation; clause: H.11.12.2.9, H.11.12.2.12; method: X.....		P
	68 - Software fault analysis; clause: H.11.12, H.27.1.1.4; method: X.....		P
	69 - Software class(es) and structure; clause: H.11.12.2, H.11.12.3, H.27.1.2.2.1, H.27.1.2.3.1; method: D		P
	70 - Analytical measures and fault/error control techniques employed; clause: H.11.12.1.2, H.11.12.2.2, H.11.12.2.4; method: X.....		P
	71 - Software fault/error detection time(s) for controls with software Classes B or C; clause: H.2.17.10, H.11.12.2.6; method: X		P
	72 - Control response(s) in case of detected fault/error; clause: H.11.12.2.7; method: X		P
	93 – Maximum number of reset actions within a time period; clause H.11.12.4.3.6, H.11.12.4.3.4; method: D.....		N/A
	94 – Number of remote reset actions; clause H.17.1.4.3; method: X.....		N/A
	m – Controls with software classes B or C had information provided for safety-related segments of the software. Information on the non-safety related segments was sufficient to establish that they did not influence safety-related segments	B	P
	n – Software sequence was documented and, together with the operating sequence, included a description of the control system philosophy, the control flow, data flow and the timings		P

	o - Safety-related data and safety-related segments of the software sequence, the malfunction of which could result in non-compliance with the requirements of Clauses 17, 25, 26 and 27, are identified		P
	– Included the operating sequence		P
	– Software fault analysis was related to the hardware fault analysis in Clause H.27.....		P
	q - Programming documentation was supplied in a programming design language declared by the manufacturer		P
	r – Different software classes applied to different control functions		N/A
	s - Measures declared are chosen by manufacturer from the requirements of Clauses H.11.12.1.2 to H.11.12.2.4 inclusive		P
H.11	Constructional requirements		—
H.11.12	Controls using software		—
	Controls using software were so constructed that the software did not impair control compliance with the requirements of this standard		P
H.11.12.1	Requirements for the architecture		—
H.11.12.1.1	Control functions with software class B or C use measures to control and avoid software-related faults/errors in safety-related data and safety-related segments of the software, as detailed in H.11.12.1.2 to H.11.12.3 inclusive	B	P
H.11.12.1.2	Control functions with software class C have one of the following structures:		—
	– single channel with periodic self-test and monitoring (H.2.16.7)		N/A
	– dual channel (homogenous) with comparison (H.2.16.3)		N/A
	– dual channel (diverse) with comparison (H.2.16.2)		N/A
	Control functions with software class B have one of the following structures:		—
	– single channel with functional test (H.2.16.5)		P
	– single channel with periodic self-test (H.2.16.6)		P

	– dual channel without comparison (H.2.16.1)		N/A
H.11.12.1.3	Other structure permitted with equivalent level of safety to those in H.11.12.1.2.....		N/A
H.11.12.2	Measures to control faults/errors		—
H.11.12.2.1	Redundant memory with comparison provided on two areas of the same component: data stored in different formats		N/A
H.11.12.2.2	Software class C using dual channel structures with comparison: additional fault/error detection means		N/A
H.11.12.2.3	Software class B or C: means for recognition and control of errors in transmission to external safety-related data paths: Means took into account errors of data, addressing, transmission timing and sequence of protocol		P
H.11.12.2.4	Software class B or C: within the control, measures are taken to address the fault/errors in safety-related segments and data indicated in Table H.1 and identified in Table 1 requirement 68.		P
H.11.12.2.5	Measures others than those specified in H.11.12.2.4 utilized to satisfy the requirements listed in Table H.1		P
H.11.12.2.6	Software fault/error detection:		—
	– occur not later than declared time(s), Table 1, requirement 71		P
	– acceptability of declared time(s): evaluated during fault analysis of the control		P
H.11.12.2.7	For controls with functions, classified as Class B or C, detection of fault/error:		—
	– results in the response declared in Table 1, requirement 72		P
	– for Class C: independent means capable of performing this response provided		N/A
H.11.12.2.8	Class C, dual channel structure, loss of dual channel capability: deemed to be an error		N/A
H.11.12.2.9	Software referenced:		—

	– to relevant parts of the operating sequence		P
	– to the associated hardware functions		P
H.11.12.2.10	Labels used for memory locations are unique		P
H.11.12.2.11	Software protected from user alteration of safety-related segments and data		P
H.11.12.2.12	Software and safety-related hardware under its control is initialized to and terminates at a declared state, Table 1, requirement 66		P
H.11.12.3	Measures to avoid errors		—
H.11.12.3.1	For controls with software class B or C the measures shown in Figure H.1 to avoid systematic faults are applied		P
	Other methods utilized that incorporate disciplined and structured processes including design and test phases		P
H.11.12.3.2	Specification		—
H.11.12.3.2.1	Software safety requirements		—
H.11.12.3.2.1.1	The specification of the software safety requirements includes:		—
	• A description of each safety related function to be implemented, including its response time(s): - functions related to the application including their related software classes - functions related to the detection, annunciation and management of software or hardware faults		P
	• A description of interfaces between software and hardware		P
	• A description of interfaces between any safety and non-safety related functions		P
H.11.12.3.2.2	Software architecture		—
H.11.12.3.2.2.1	The description of software architecture include the following aspects:		—
	• Techniques and measures to control software faults/errors (refer to H.11.12.2)		P

	• Interactions between hardware and software		P
	• Partitioning into modules and their allocation to the specified safety functions		P
	• Hierarchy and call structure of the modules (control flow)		P
	• Interrupt handling		P
	• Data flow and restrictions on data access		P
	• Architecture and storage of data		P
	• Time based dependencies of sequences and data		P
H.11.12.3. 2.2.2	The architecture specification is verified against the specification of the software safety requirements by static analysis		P
H.11.12.3. 2.3	Module design and coding		—
H.11.12.3. 2.3.1	Software is suitably refined into modules. Software module design and coding are implemented in a way that is traceable to the software architecture and requirements. The module design specified:		P
	– function(s)		P
	– interfaces to other modules		P
	– data		P
H.11.12.3. 2.3.2	Software code is structured		P
H.11.12.3. 2.3.3	Coded software is verified against the module specification, and the module specification is verified against the architecture specification by static analysis		P
H.11.12.3. 2.4	Design and coding standards		P
	Program design and coding standards is used during software design and maintenance		P
	Coding standards :		—
	– specified programming practice		P
	– proscribed unsafe language features		P

	– specify procedures for source code documentation		P
	– specify data naming conventions		P
H.11.12.3.3	Testing		—
H.11.12.3.3.1	Module design (software system design, software module design and coding)		—
H.11.12.3.3.1.1	A test concept with suitable test cases is defined based on the module design specification.		P
H.11.12.3.3.1.2	Each software module is tested as specified within the test concept		P
H.11.12.3.3.1.3	Test cases, test data and test results are documented		P
H.11.12.3.3.1.4	Code verification of a software module by static means includes such techniques as software inspections, walk-throughs, static analysis and formal proof		P
	Code verification of a software module by dynamic means includes functional testing, white-box testing and statistical testing		P
H.11.12.3.3.2	Software integration testing		—
H.11.12.3.3.2.1	A test concept with suitable test cases is defined based on the architecture design specification		P
H.11.12.3.3.2.2	The software is tested as specified within the test concept		P
H.11.12.3.3.2.3	Test cases, test data and test results are documented		P
H.11.12.3.3.3	Software validation		—
H.11.12.3.3.3.1	A validation concept with suitable test cases is defined based on the software safety requirements specification		P
H.11.12.3.3.3.2	The software is validated with reference to the requirements of the software safety requirements specification as specified within the validation concept		P
	The software is exercised by simulation or stimulation of:		—

	• input signals present during normal operation		P
	• anticipated occurrences		N/A
	• undesired conditions requiring system action		N/A
H.11.12.3.3.3.4	Test cases, test data and test results are documented		P
H.11.12.3.4	Other Items		—
H.11.12.3.4.1	Equipment used for software design, verification and maintenance was qualified appropriately and demonstrated to be suitable for purpose in manifold applications		P
H.11.12.3.4.2	Management of software versions: All versions are uniquely identified for traceability		P
H.11.12.3.4.3	Software modification		—
H.11.12.3.4.3.1	Software modifications are based on a modification request which details the following:		P
	• the hazards which may be affected		P
	• the proposed change		P
	• the reasons for change		P
H.11.12.3.4.3.2	An analysis is carried out to determine the impact of the proposed modification on functional safety.		P
H.11.12.3.4.3.3	A detailed specification for the modification is generated including the necessary activities for verification and validation, such as a definition of suitable test cases		P
H.11.12.3.4.3.4	The modification is carried out as planned		P
H.11.12.3.4.3.5	The assessment of the modification is carried out based on the specified verification and validation activities.		P
H.11.12.3.4.3.6	All details of modification activities are documented		P
H.11.12.3.5	For class C control functions: One of the combinations (a–p) of analytical measures given in the columns of table H.9 is used during hardware development.....		P

H.11.12.4	Remotely actuated control functions		—
H.11.12.4.1.1	Data Exchange – General – Remotely actuated control functions are connected to separate, independent devices, which may themselves contain control functions or provide other information and any data exchange between these devices does not compromise the integrity of class B control function or class C control function.		N/A
H.11.12.4.1.2	Type of data - Message types for data exchange in a control function or functions are allocated to class A control function, class B control function or class C control function. The safety or protective relevance or influence, message types or data exchange are allocated only to class B control function or class C control functions, see Table H.10.		N/A
H.11.12.4.1.3.1	Communication of Safety Related Data – Transmission – Safety relevant data is transmitted authentically concerning:		N/A
	– data corruption		N/A
	– address corruption		N/A
	– wrong timing or sequence		N/A
	Data variation or corrupted data did not lead to an unsafe state		N/A
	Before transmitted data was used it was ensured that data corruption, address corruption and wrong timing or sequence are addressed using the measures as given in Annex H.		N/A
	The following failure modes are addressed:		—
	– permanent “auto-sending” or repetition,		N/A
	– interruption of data transfer		N/A
H.11.12.4.1.3.2	Access to data exchange - All types of access to class B control function or class C control function related data exchange systems is clearly restricted		N/A
	Adequate hardware/software measures are taken to ensure no unauthorized access to the control functions (class B and C; operating data, configuration parameters and/or software modules)		N/A

H.11.12.4.1.3.3	For class B and class C software revisions the requirements of H.11.12.3 and hardware configuration management are applied and the control maintains its protective functions		N/A
H.11.12.4.1.4	Remotely actuated control function operation have the duration or limits set before switching on except when automatic switching off is realized at the end of a cycle or the system is designed for permanent operation.		N/A
H.11.12.4.2	Priority of remotely actuated control functions over control functions does not lead to a hazardous condition.		N/A
H.11.12.4.3.1	Remote reset action is manually initiated.		N/A
	Reset functionality initiated by a hand-held device required at least two manual actions to activate		N/A
H.11.12.4.3.2	Reset functions are capable of resetting the system as intended		N/A
H.11.12.4.3.3	Unintended resets from safe state do not occur.		N/A
H.11.12.4.3.4	Any fault of the reset function does not cause the control or controlled function to result in a hazardous condition, and was evaluated for its Class B classification		N/A
H.11.12.4.3.5	For reset functions initiated by manual action not in visible sight of the appliance, the following additional requirements apply:		N/A
	– the actual status and relevant information of the process under control is visible to the user before, during and after the reset action;		N/A
	– the maximum number of reset actions within a time period is declared. Following this, any further reset is denied unless the appliance is physically checked		N/A
H.11.12.4.3.6	The reset function is evaluated on the final application.		N/A
	Manual switching of a thermostat or device with similar function that activates a reset is declared by the manufacturer and is suitable in the final application		N/A

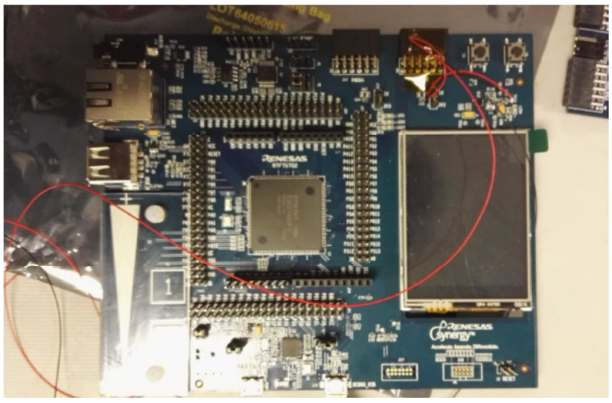
Ergänzende Information / *Supplementary information*:				
The self-diagnostic routines mentioned under I are foreseen for following measures of table R.1 / H.1 of.				
S1 File Name	S3 File Name	S5 File Name	S7 File Name	Measure
cpu_test.c	cpu_test.c	cpu_test.c	cpu_test.c	1.1 CPU Register
CPU_Test_Control.asm	CPU_Test_Control.asm	CPU_Test_Control.asm	CPU_Test_Control.asm	
cpu_test_coupling.c	cpu_test_coupling.c	cpu_test_coupling.c	cpu_test_coupling.c	
CPU_Test_General_High.asm	CPU_Test_General_High.asm	CPU_Test_General_High.asm	CPU_Test_General_High.asm	
CPU_Test_General_Low.asm	CPU_Test_General_Low.asm	CPU_Test_General_Low.asm	CPU_Test_General_Low.asm	
N/A	fpu_control.asm	fpu_control.asm	fpu_control.asm	
N/A	fpu_exten.asm	fpu_exten.asm	fpu_exten.asm	
N/A	fpu_test_coupling.c	fpu_test_coupling.c	fpu_test_coupling.c	
N/A	TestFPUCouplingEnd.asm	TestFPUCouplingEnd.asm	TestFPUCouplingEnd.asm	
N/A	TestFPUCouplingStart_A.asm	TestFPUCouplingStart_A.asm	TestFPUCouplingStart_A.asm	
N/A	TestFPUCouplingStart_B.asm	TestFPUCouplingStart_B.asm	TestFPUCouplingStart_B.asm	
TestGPRsCouplingEnd.asm	TestGPRsCouplingEnd.asm	TestGPRsCouplingEnd.asm	TestGPRsCouplingEnd.asm	
TestGPRsCouplingStart_A.asm	TestGPRsCouplingStart_A.asm	TestGPRsCouplingStart_A.asm	TestGPRsCouplingStart_A.asm	
TestGPRsCouplingStart_B.asm	TestGPRsCouplingStart_B.asm	TestGPRsCouplingStart_B.asm	TestGPRsCouplingStart_B.asm	
N/A	TestFPUCouplingS0_S3_A.asm	TestFPUCouplingS0_S3_A.asm	TestFPUCouplingS0_S3_A.asm	
N/A	TestFPUCouplingS0_S3_B.asm	TestFPUCouplingS0_S3_B.asm	TestFPUCouplingS0_S3_B.asm	
N/A	TestFPUCouplingS4_S7_A.asm	TestFPUCouplingS4_S7_A.asm	TestFPUCouplingS4_S7_A.asm	
N/A	TestFPUCouplingS4_S7_B.asm	TestFPUCouplingS4_S7_B.asm	TestFPUCouplingS4_S7_B.asm	
N/A	TestFPUCouplingS8_S11_A.asm	TestFPUCouplingS8_S11_A.asm	TestFPUCouplingS8_S11_A.asm	
N/A	TestFPUCouplingS8_S11_B.asm	TestFPUCouplingS8_S11_B.asm	TestFPUCouplingS8_S11_B.asm	

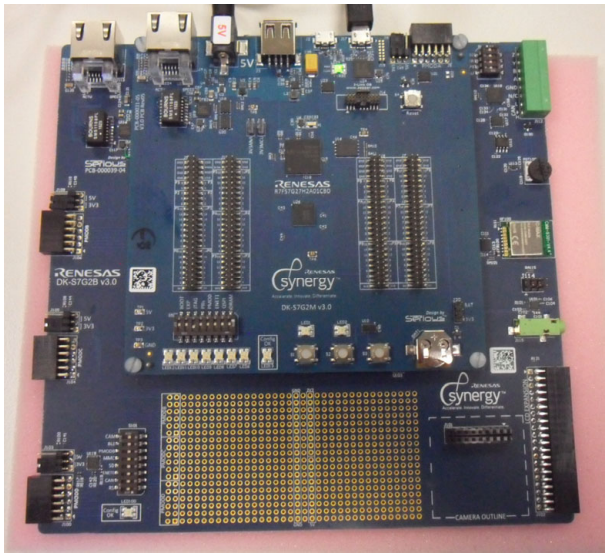
N/A	TestFPUCouplingS12_S15_A.asm	TestFPUCouplingS12_S15_A.asm	TestFPUCouplingS12_S15_A.asm	
N/A	TestFPUCouplingS12_S15_B.asm	TestFPUCouplingS12_S15_B.asm	TestFPUCouplingS12_S15_B.asm	
N/A	TestFPUCouplingS16_S19_A.asm	TestFPUCouplingS16_S19_A.asm	TestFPUCouplingS16_S19_A.asm	
N/A	TestFPUCouplingS16_S19_B.asm	TestFPUCouplingS16_S19_B.asm	TestFPUCouplingS16_S19_B.asm	
N/A	TestFPUCouplingS20_S23_A.asm	TestFPUCouplingS20_S23_A.asm	TestFPUCouplingS20_S23_A.asm	
N/A	TestFPUCouplingS20_S23_B.asm	TestFPUCouplingS20_S23_B.asm	TestFPUCouplingS20_S23_B.asm	
N/A	TestFPUCouplingS24_S27_A.asm	TestFPUCouplingS24_S27_A.asm	TestFPUCouplingS24_S27_A.asm	
N/A	TestFPUCouplingS24_S27_B.asm	TestFPUCouplingS24_S27_B.asm	TestFPUCouplingS24_S27_B.asm	
N/A	TestFPUCouplingS28_S31_A.asm	TestFPUCouplingS28_S31_A.asm	TestFPUCouplingS28_S31_A.asm	
N/A	TestFPUCouplingS28_S31_B.asm	TestFPUCouplingS28_S31_B.asm	TestFPUCouplingS28_S31_B.asm	
TestGPRsCouplingR0_A.asm	TestGPRsCouplingR0_A.asm	TestGPRsCouplingR0_A.asm	TestGPRsCouplingR0_A.asm	
TestGPRsCouplingR0_B.asm	TestGPRsCouplingR0_B.asm	TestGPRsCouplingR0_B.asm	TestGPRsCouplingR0_B.asm	
TestGPRsCouplingR1_R3_A.asm	TestGPRsCouplingR1_R3_A.asm	TestGPRsCouplingR1_R3_A.asm	TestGPRsCouplingR1_R3_A.asm	
TestGPRsCouplingR1_R3_B.asm	TestGPRsCouplingR1_R3_B.asm	TestGPRsCouplingR1_R3_B.asm	TestGPRsCouplingR1_R3_B.asm	
TestGPRsCouplingR4_R6_A.asm	TestGPRsCouplingR4_R6_A.asm	TestGPRsCouplingR4_R6_A.asm	TestGPRsCouplingR4_R6_A.asm	
TestGPRsCouplingR4_R6_B.asm	TestGPRsCouplingR4_R6_B.asm	TestGPRsCouplingR4_R6_B.asm	TestGPRsCouplingR4_R6_B.asm	
TestGPRsCouplingR7_R9_A.asm	TestGPRsCouplingR7_R9_A.asm	TestGPRsCouplingR7_R9_A.asm	TestGPRsCouplingR7_R9_A.asm	
TestGPRsCouplingR7_R9_B.asm	TestGPRsCouplingR7_R9_B.asm	TestGPRsCouplingR7_R9_B.asm	TestGPRsCouplingR7_R9_B.asm	
TestGPRsCouplingR10_R12_A.asm	TestGPRsCouplingR10_R12_A.asm	TestGPRsCouplingR10_R12_A.asm	TestGPRsCouplingR10_R12_A.asm	
TestGPRsCouplingR10_R12_B.asm	TestGPRsCouplingR10_R12_B.asm	TestGPRsCouplingR10_R12_B.asm	TestGPRsCouplingR10_R12_B.asm	
clock_monitor.c	clock_monitor.c	clock_monitor.c	clock_monitor.c	3. Clock
crc.c	crc.c	crc.c	crc.c	4.1 invariable memory
CRC_Verify.c	CRC_Verify.c	CRC_Verify.c	CRC_Verify.c	

ramtest_march_c.c	ramtest_march_c.c	ramtest_march_c.c	ramtest_march_c.c	4.2 variable memory
ramtest_march_c_HW.c	ramtest_march_c_HW.c	ramtest_march_c_HW.c	ramtest_march_c_HW.c	
ramtest_march_HW.c	ramtest_march_HW.c	ramtest_march_HW.c	ramtest_march_HW.c	
ramtest_march_x_wom.c	ramtest_march_x_wom.c	ramtest_march_x_wom.c	ramtest_march_x_wom.c	
ramtest_march_x_wom_HW.c	ramtest_march_x_wom_HW.c	ramtest_march_x_wom_HW.c	ramtest_march_x_wom_HW.c	
test_adc14.c	test_adc14.c	test_adc12.c	test_adc12.c	7.2.1 A/D- and D/A-converter

Fotodokumentation / *Photo documentation*:

Test Setup for S7 (setup for S1; S3 and S5 nearly equal)





Prüf- und Messmittel / *Testing and measuring equipment*: for S7 (tools for S1; S3 and S5 nearly equal)	
Editor:	IAR Embedded Workbenchfor ARM, v. 7.40 IAR Embedded Workbench Common Components, v. 7.2
Compiler/Linker:	IAR Embedded Workbenchfor ARM, v. 7.40 IAR Embedded Workbench Common Components, v. 7.2
Debugger:	IAR Embedded Workbenchfor ARM, v. 7.40 IAR Embedded Workbench Common Components, v. 7.2
Hardware:	Renesas DK-S7G2 Development Kit for Synergy S7

Messunsicherheit (optional nach Abschnitt 5.10.3.1.c der IEC 17025) *Uncertainty of measurement (optional according to sub-clause 5.10.3.1.c of IEC 17025)*:
N/A

END OF TEST REPORT