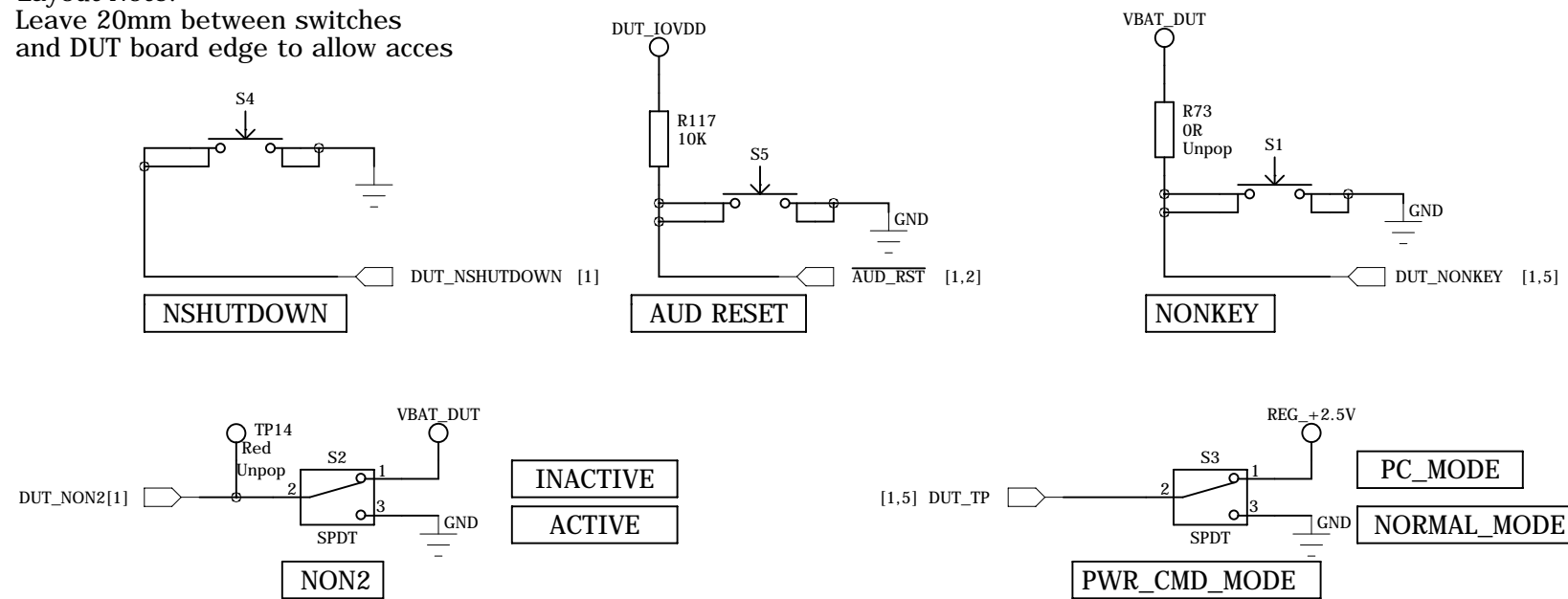
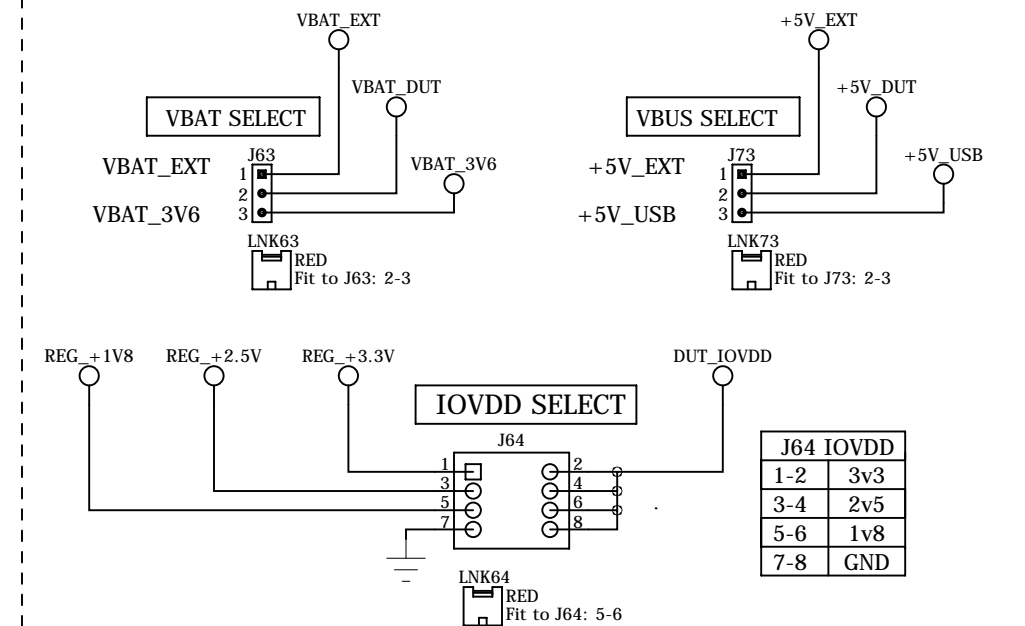


DUT INTERCONNECT HEADERS

Layout Note:  
Leave 20mm between switches  
and DUT board edge to allow access



DUT SWITCHES

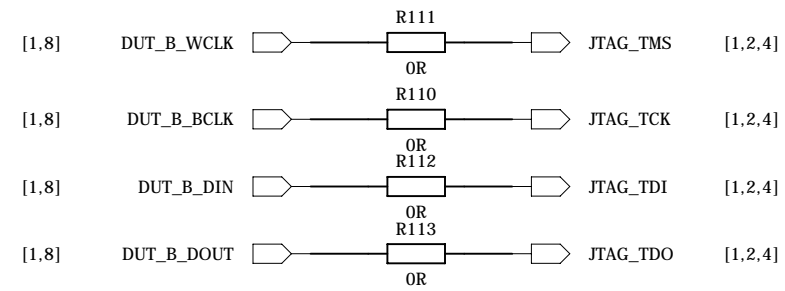
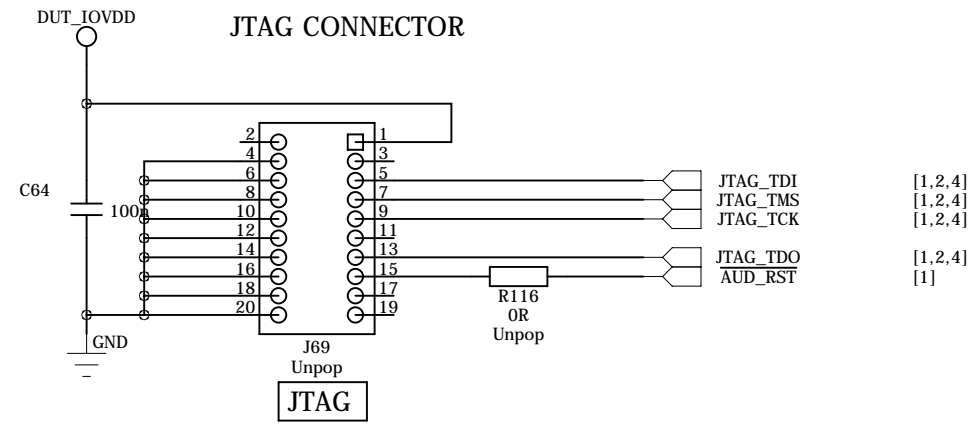


DUT SUPPLY SELECT

SCHMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

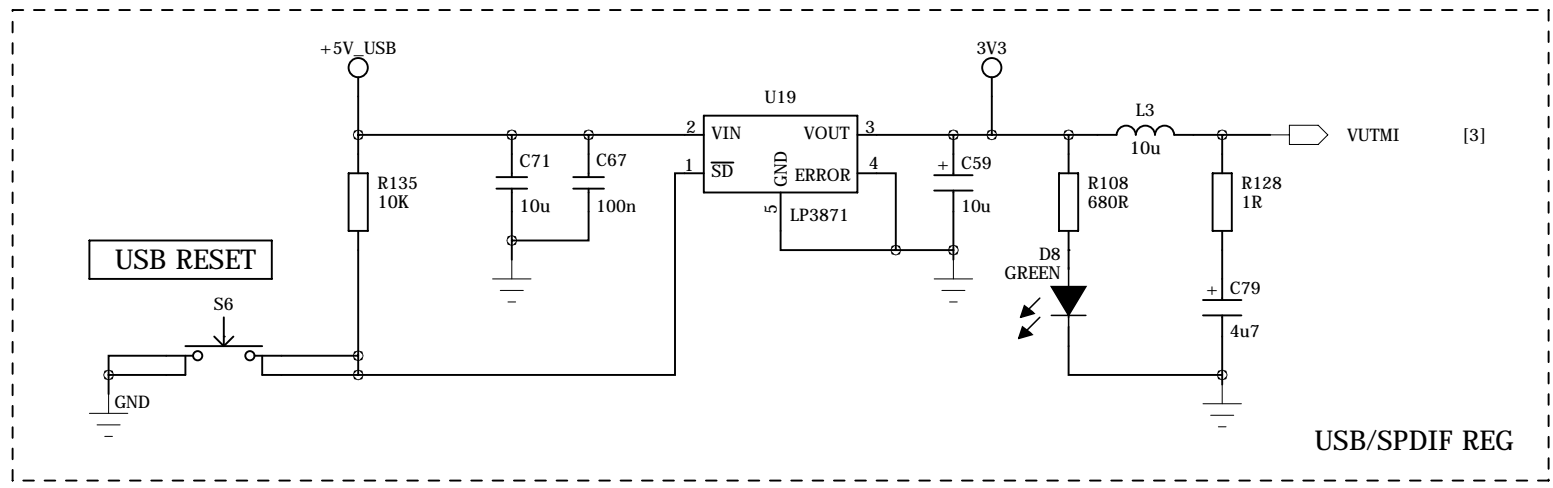
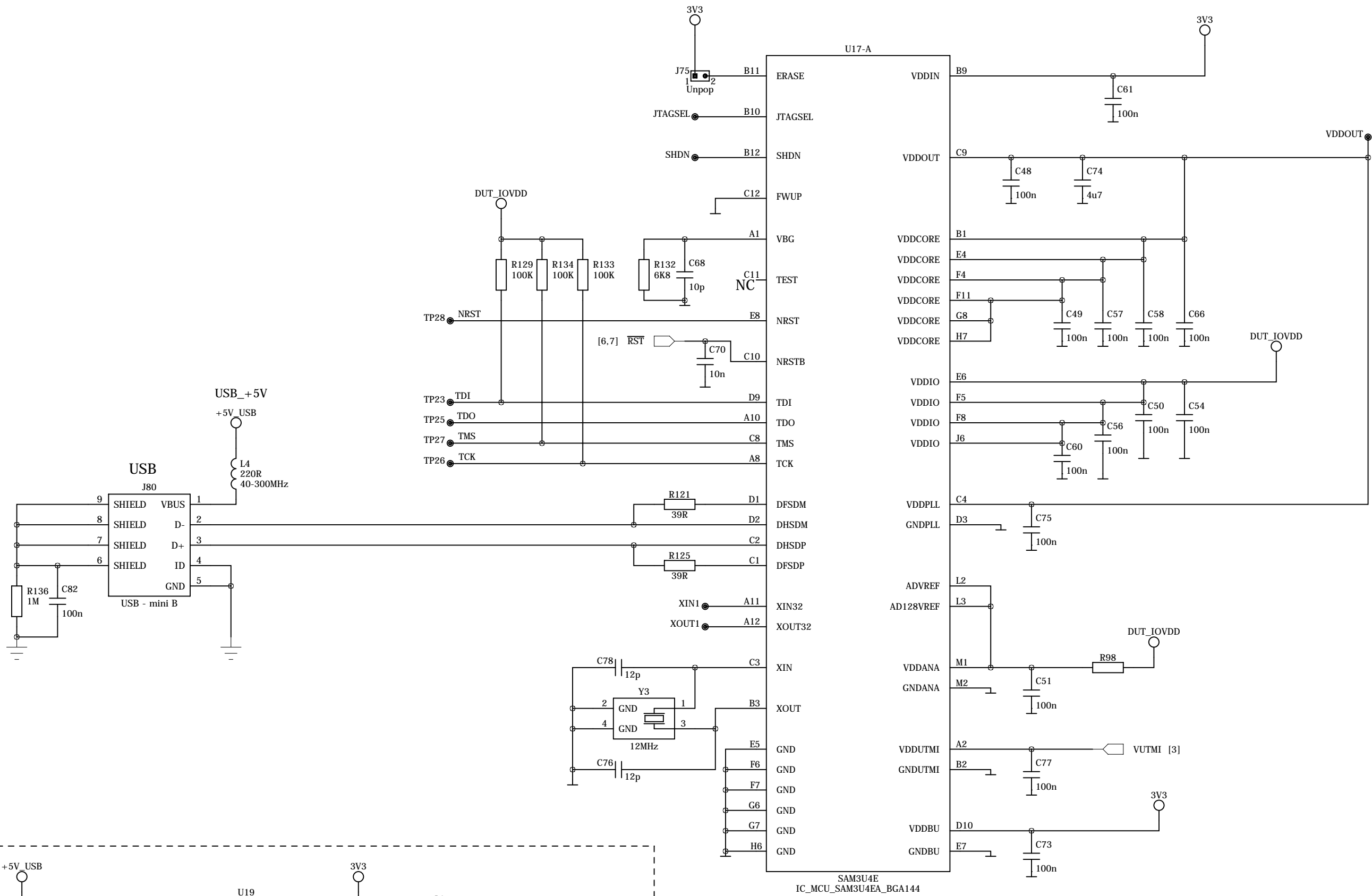
CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: DUT_HEADERS	PAGE: 1 OF 16





CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: <b>BL/BT</b>	DATED: 23/04/2013	DRAWING NO: <b>44-179-170-01-B</b>	REV: <b>C</b>
RESPONSIBLE: <b>BT</b>	DATED: 23/04/2013	SHEET NAME: <b>JTAG</b>	PAGE: <b>2 OF 16</b>



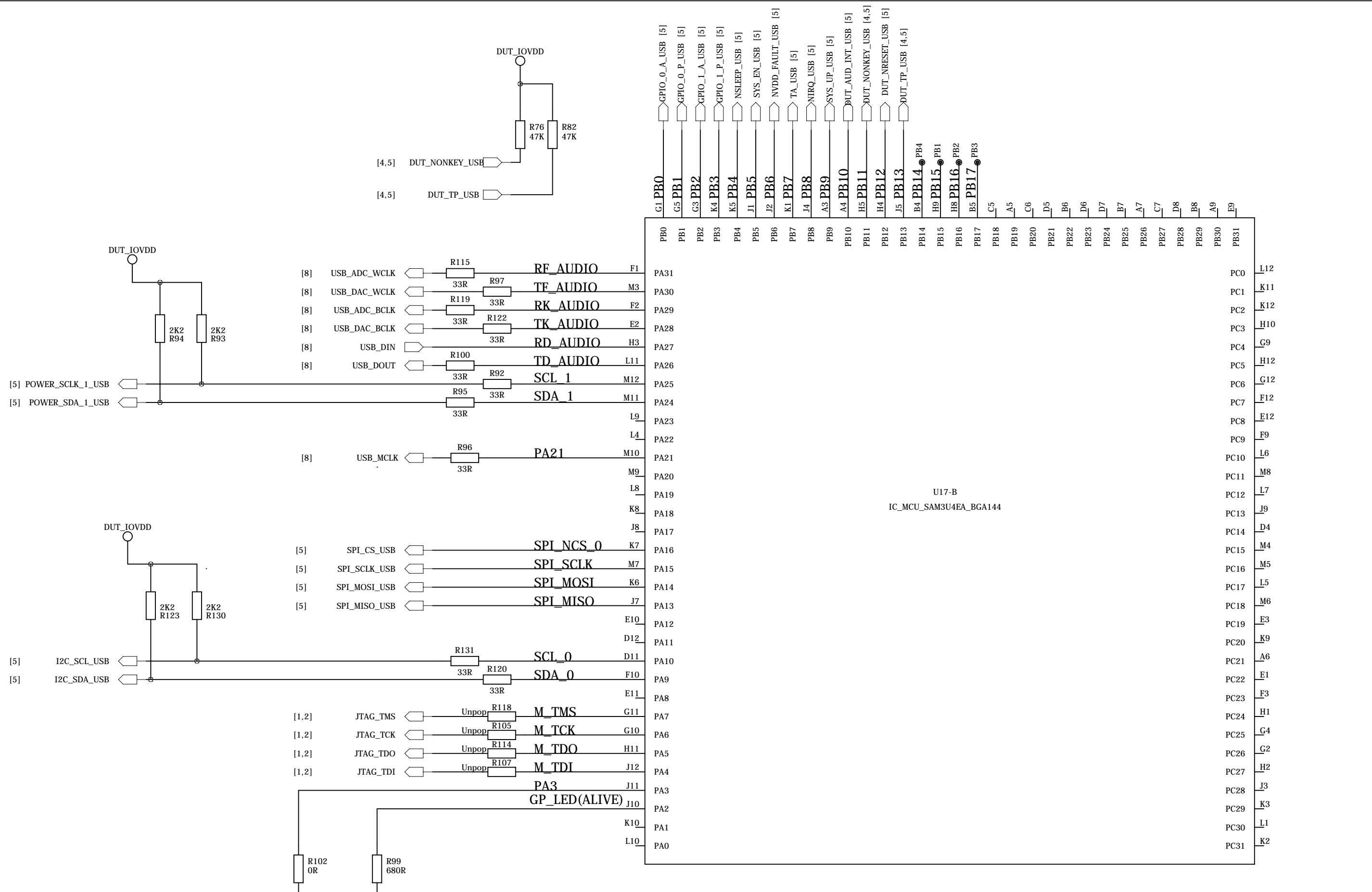


CONFIDENTIAL INFORMATION

PREPARED: BL/BT	DATED: 23/04/2013
RESPONSIBLE: BT	DATED: 23/04/2013

TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
DRAWING NO: 44-179-170-01-B	REV: C
SHEET NAME: USB_IF	





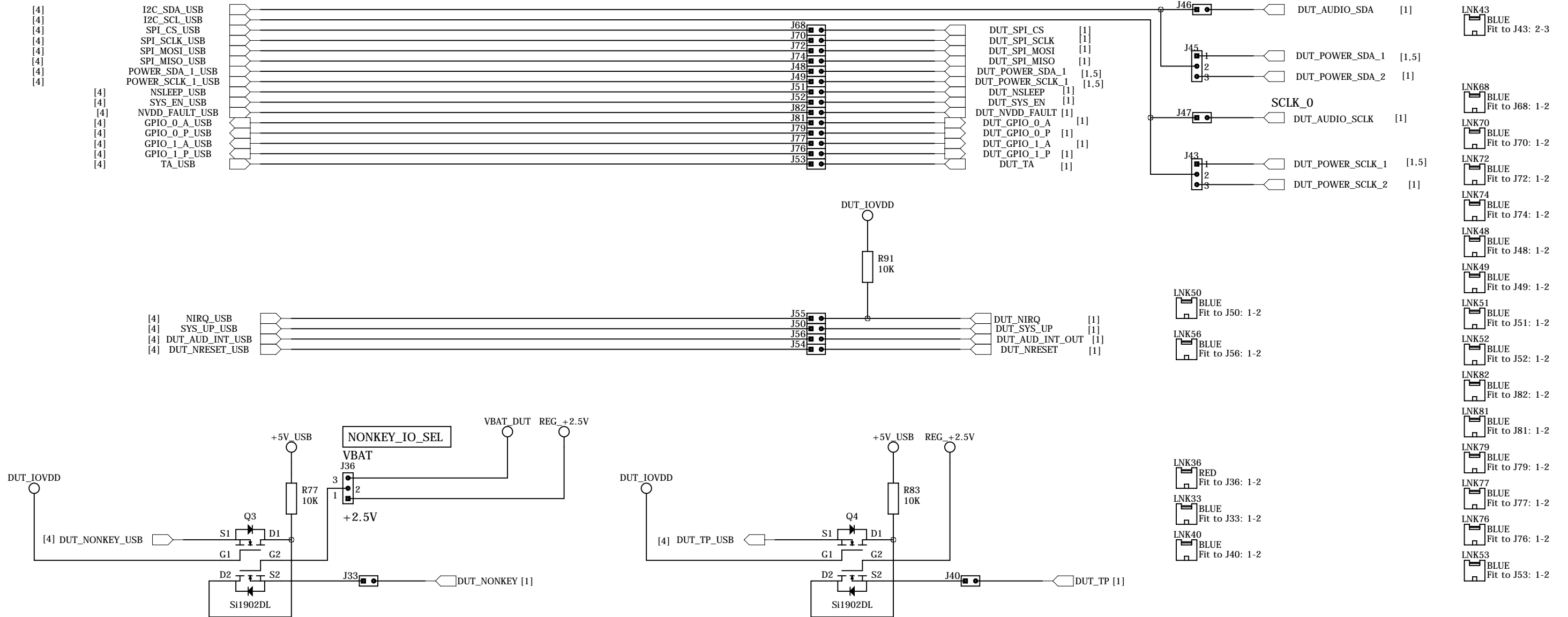
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G5	PB1	>	GPIO_0_P_USB [5]	PA30	PC1	K11
G3	PB2	>	GPIO_1_A_USB [5]	PA29	PC2	K12
K4	PB3	>	GPIO_1_P_USB [5]	PA28	PC3	H10
K5	PB4	>	NSLEEP_USB [5]	PA27	PC4	G9
J1	PB5	>	SYS_EN_USB [5]	PA26	PC5	H12
J2	PB6	>	NVDD_FAULT_USB [5]	PA25	PC6	H12
K1	PB7	>	TA_USB [5]	PA24	PC7	F12
J4	PB8	>	NIRQ_USB [5]	PA23	PC8	E12
A3	PB9	>	SYS_UP_USB [5]	PA22	PC9	F9
A4	PB10	>	DUT_AUD_INT_USB [5]	PA21	PC10	L6
H5	PB11	>	DUT_NONKEY_USB [4,5]	PA20	PC11	M8
H4	PB12	>	DUT_NRESET_USB [5]	PA19	PC12	L7
J5	PB13	>	DUT_TP_USB [4,5]	PA18	PC13	J9
E4	PB14	>		PA17	PC14	D4
H9	PB15	>		PA16	PC15	M4
H8	PB16	>		PA15	PC16	M5
B5	PB17	>		PA14	PC17	L5
C5		>		PA13	PC18	M6
A5		>		PA12	PC19	E3
C6		>		PA11	PC20	K9
D5		>		PA10	PC21	A6
B6		>		PA9	PC22	E1
D6		>		PA8	PC23	F3
D7		>		PA7	PC24	H1
B7		>		PA6	PC25	G4
A7		>		PA5	PC26	G2
C7		>		PA4	PC27	H2
D8		>		PA3	PC28	J3
B8		>		PA2	PC29	K3
A9		>		PA1	PC30	L1
E9		>		PA0	PC31	K2

U17-B  
IC\_MCU\_SAM3U4EA\_BGA144

CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: USB_LEVEL_SHIFTER	PAGE: 4 OF 16



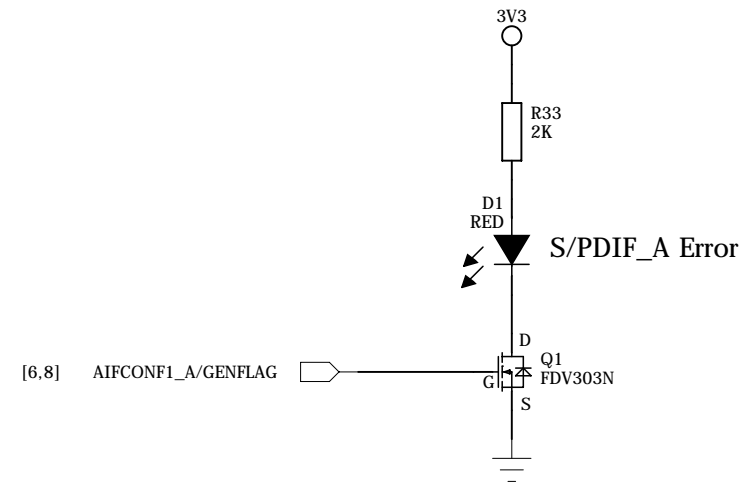
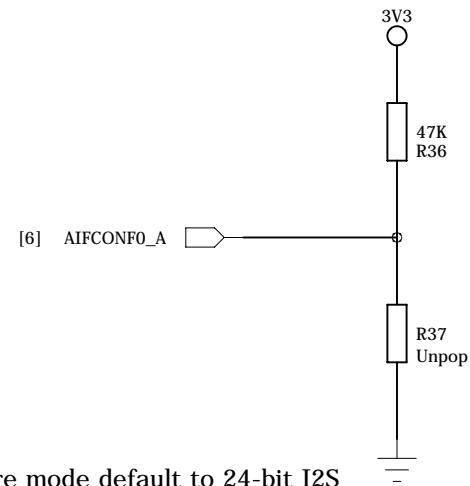
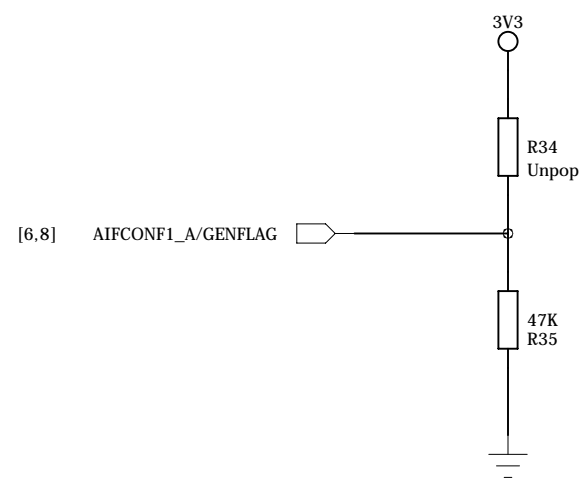
SAM3U - DUT I/F



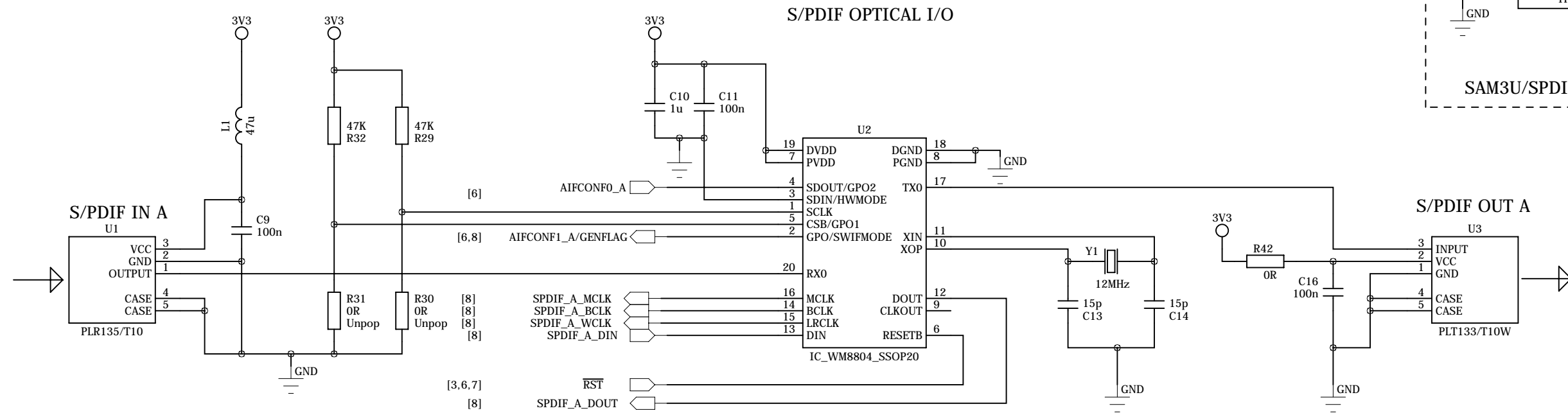
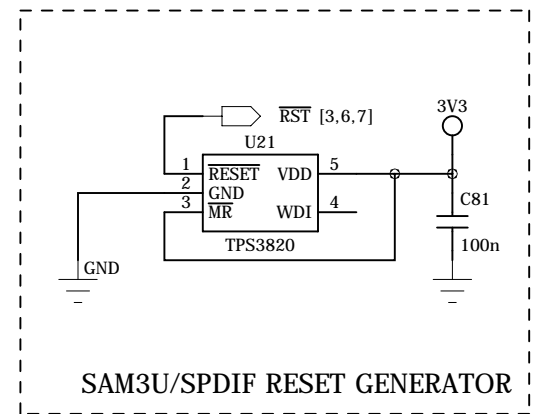
SCHMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: COMS_IF	PAGE: 5 OF 16

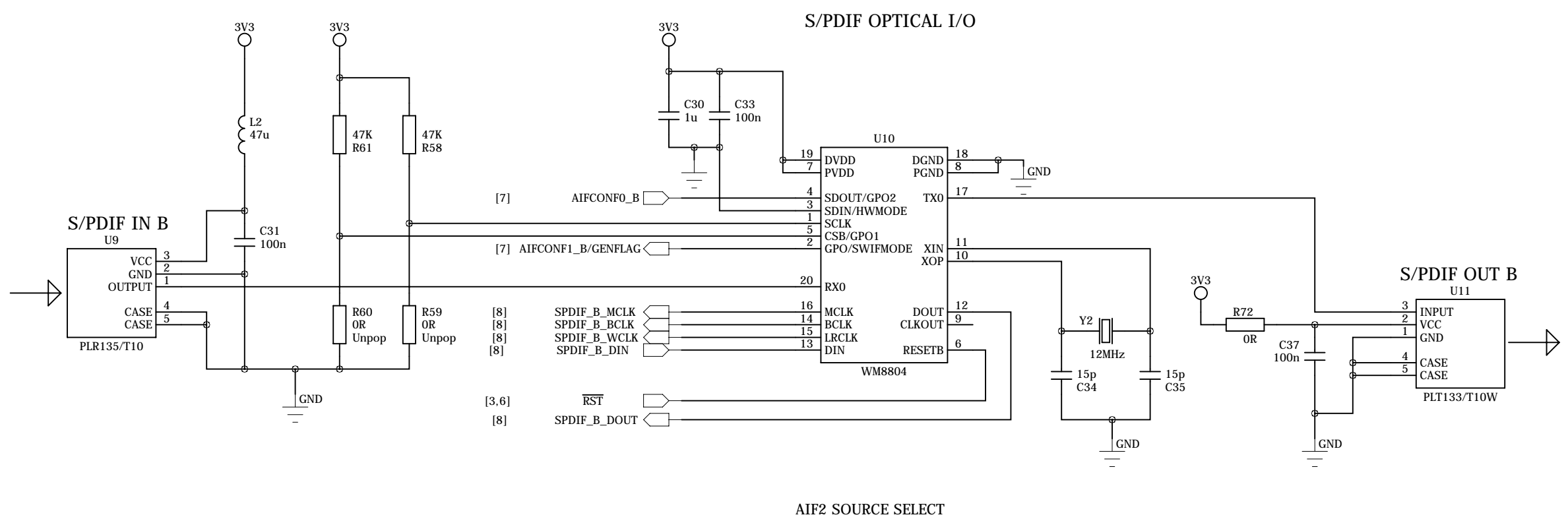
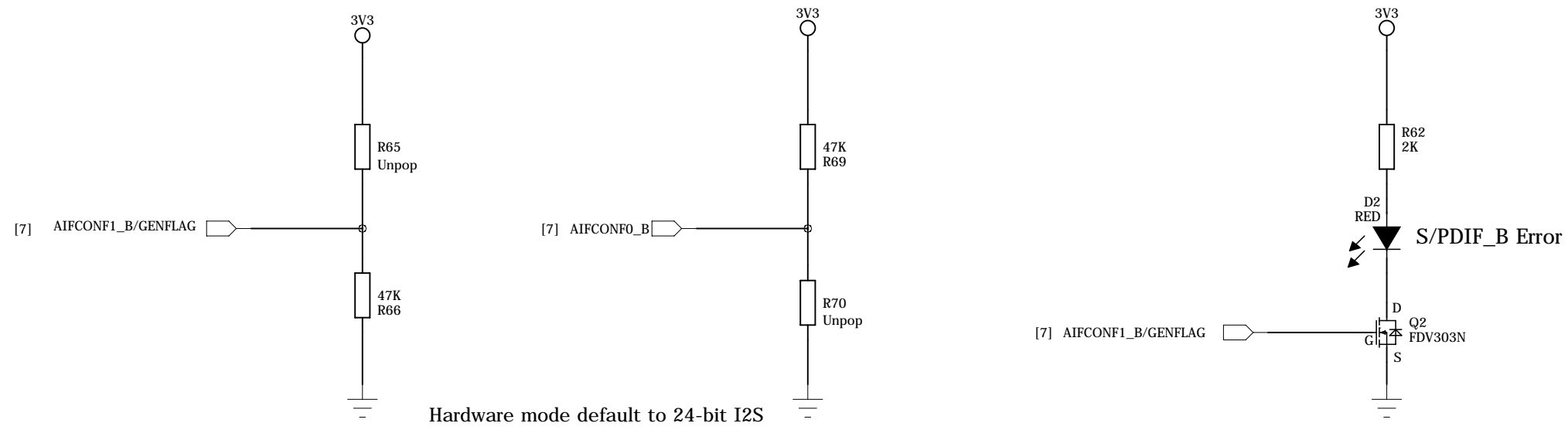




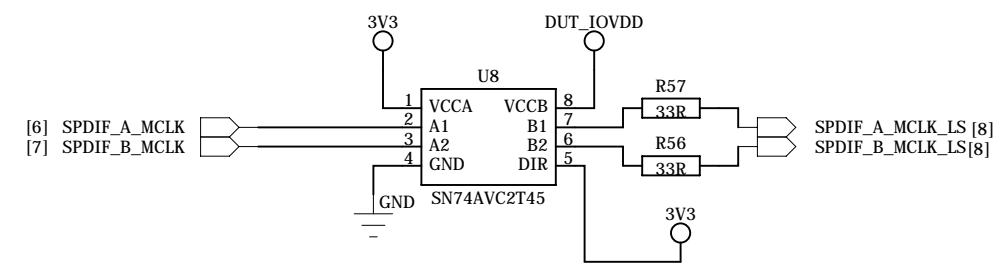
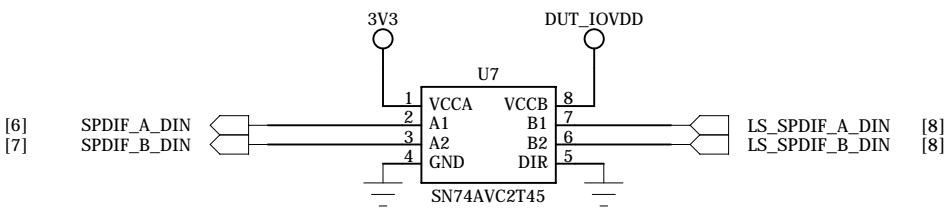
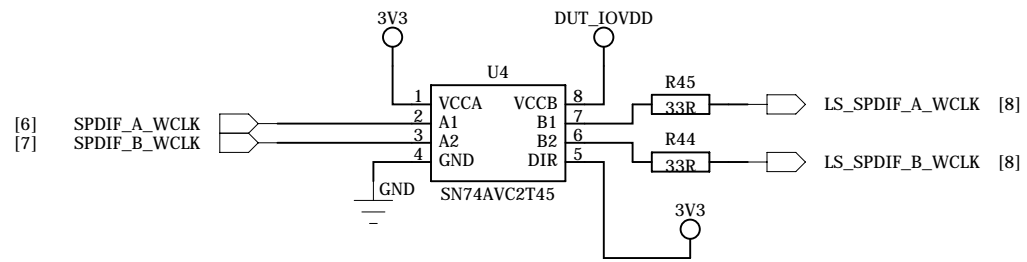
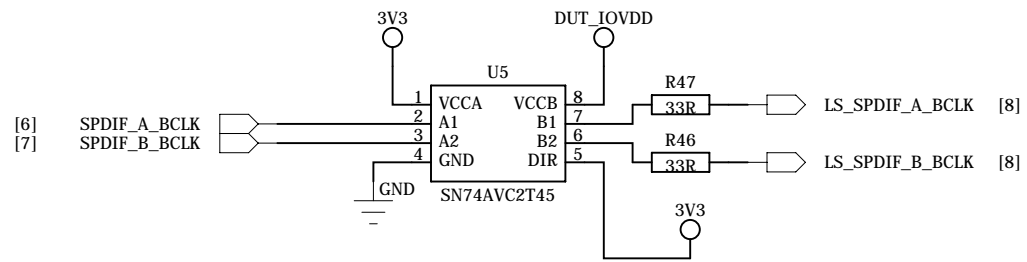
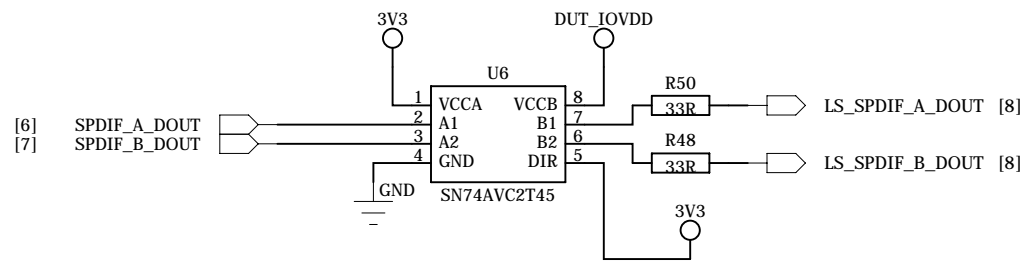
Hardware mode default to 24-bit I2S



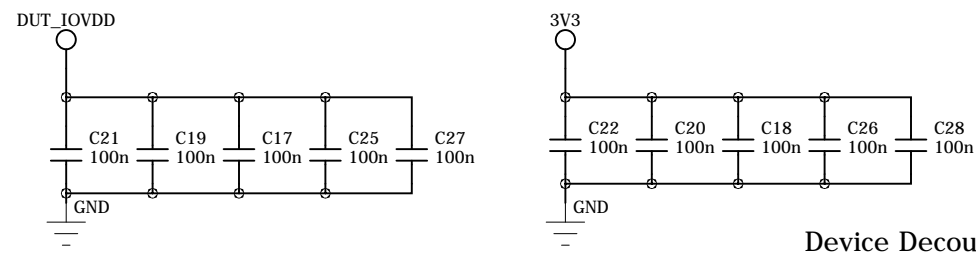
CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD		
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C	
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: S/PDIF_A	PAGE: 6 OF 16	



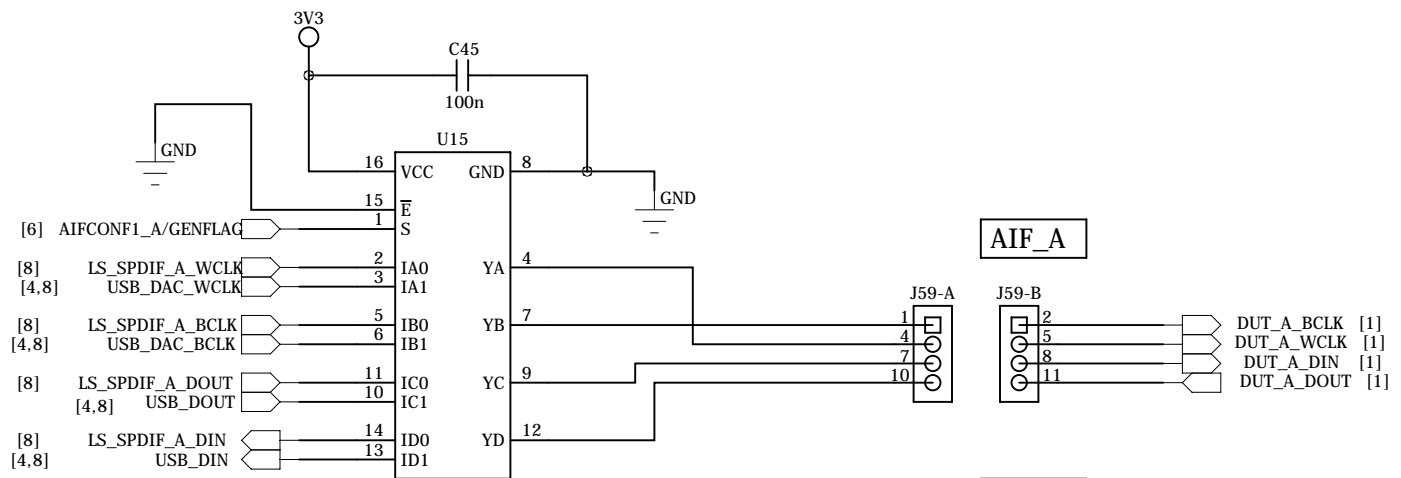
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PREPARED: <b>BL/BT</b>	DATED: 23/04/2013	DRAWING NO: <b>44-179-170-01-B</b>	REV: <b>C</b>	
RESPONSIBLE: <b>BT</b>	DATED: 23/04/2013	SHEET NAME: <b>S/PDIF_B</b>	PAGE: <b>7 OF 16</b>	



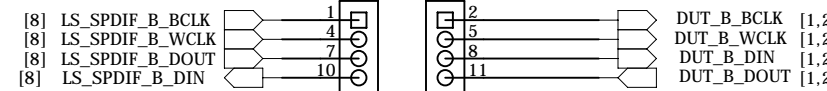
I2S VOLTAGE LEVEL TRANSLATION



Device Decoupling

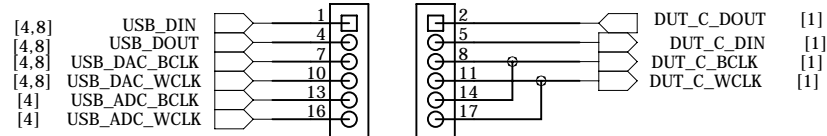


AIF\_A SELECT SWITCH

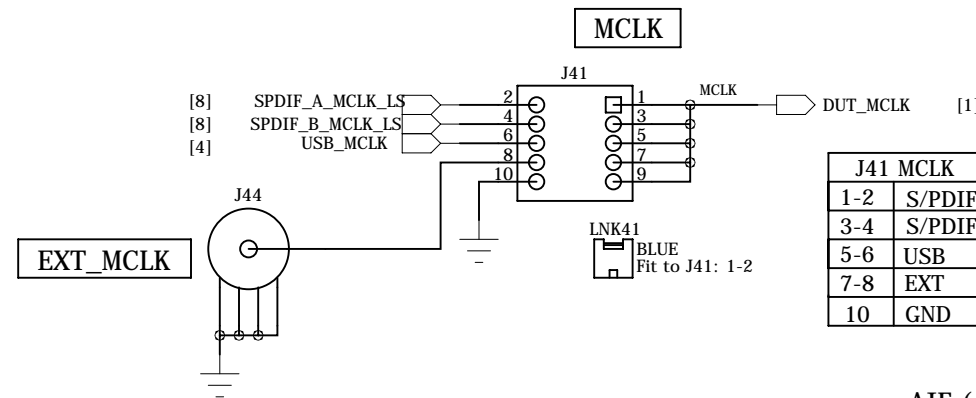


LNK59  
BLACK  
Fit to J59: A-B

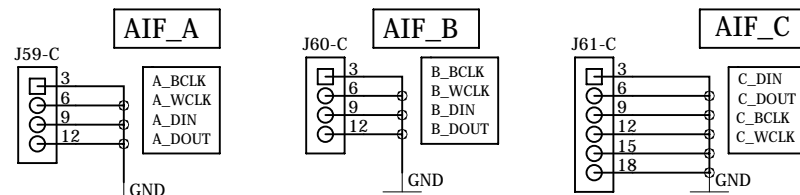
LNK60  
BLACK  
Fit to J60: A-B



LNK61  
BLACK  
Fit to J61: A-B



AIF (A/B/C) / MCLK HEADERS



AIF Header GND Connections

CONFIDENTIAL INFORMATION

PREPARED: BL/BT	DATED: 23/04/2013
RESPONSIBLE: BT	DATED: 23/04/2013

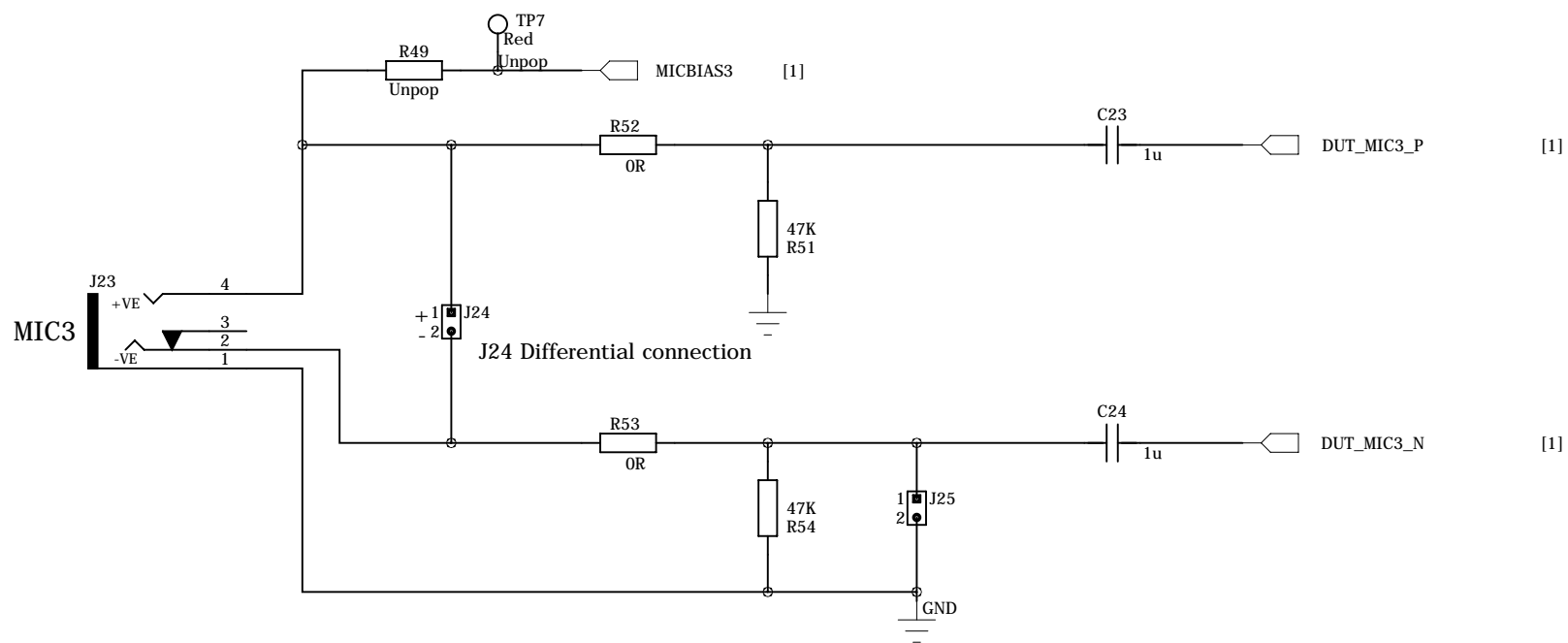
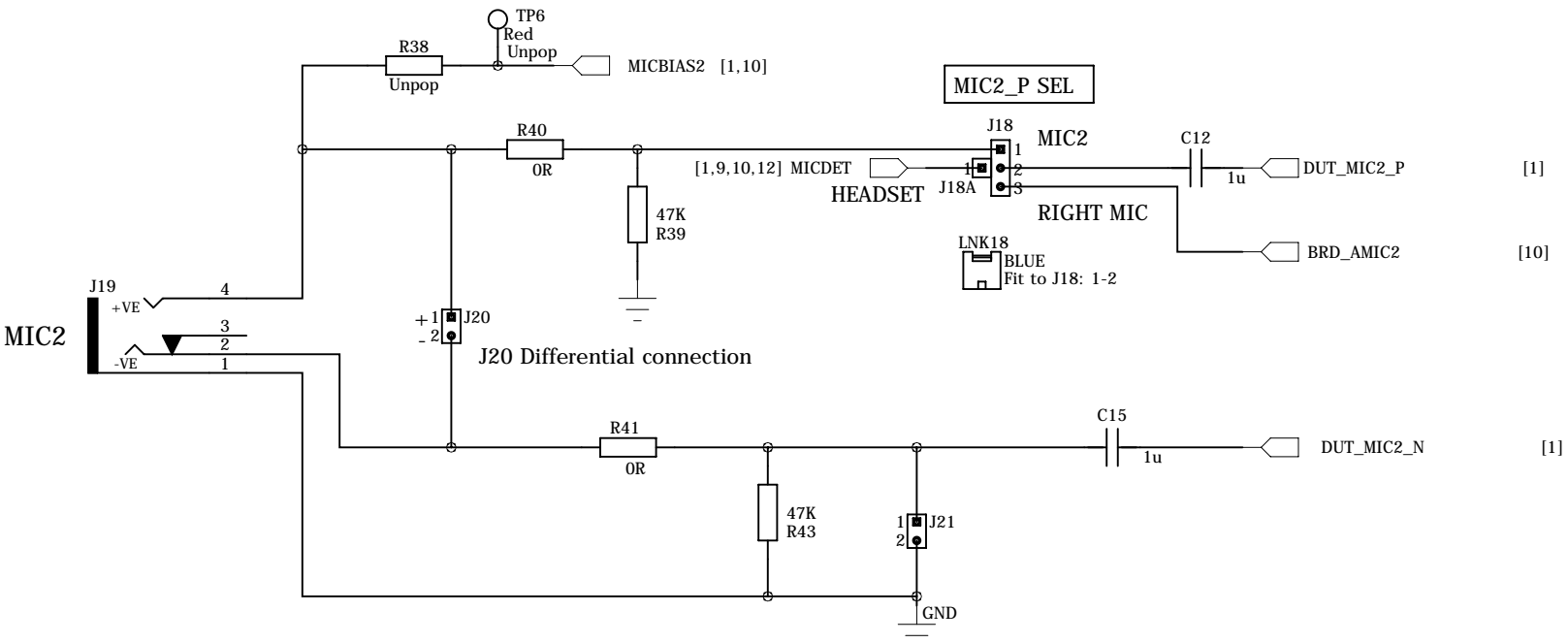
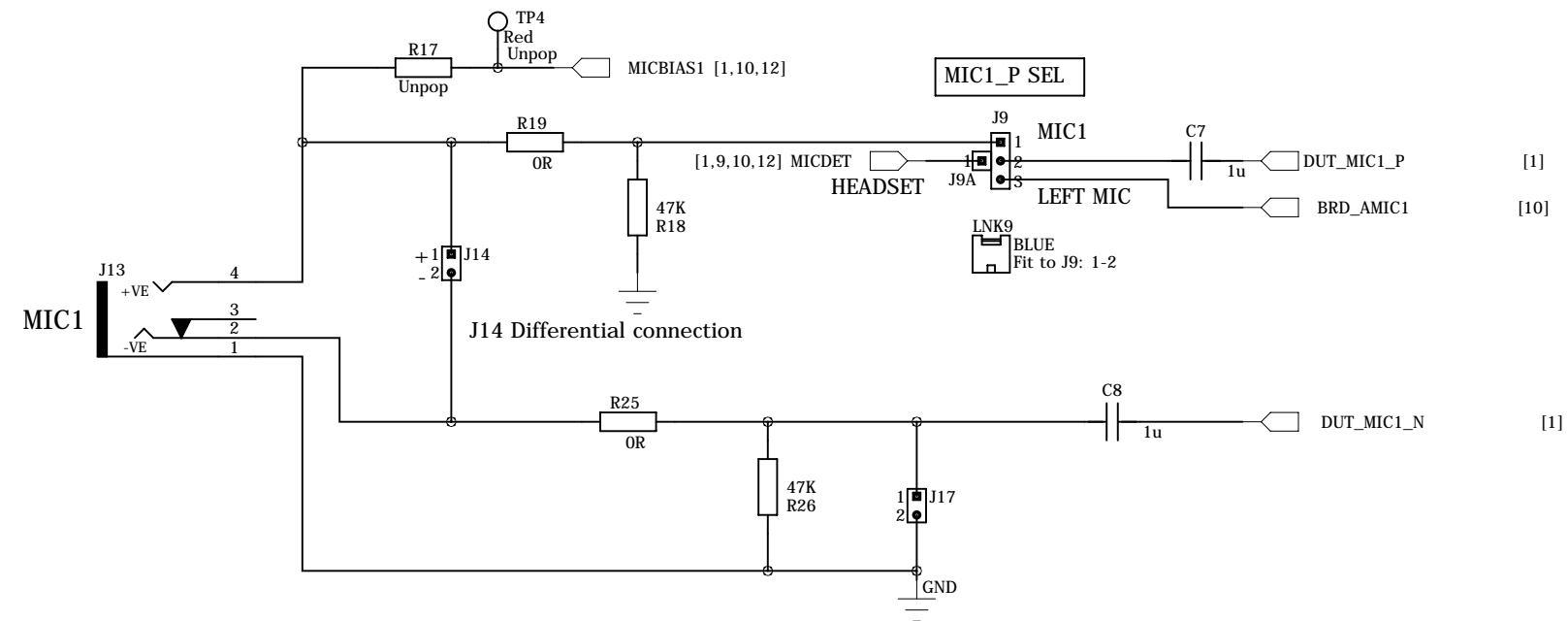
TITLE:  
AUDIO DSP PMIC CUSTOMER EVAL BOARD

DRAWING NO: 44-179-170-01-B	REV: C
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SHEET NAME: I2S_LEVEL_SHIFT	PAGE: 8 OF 16
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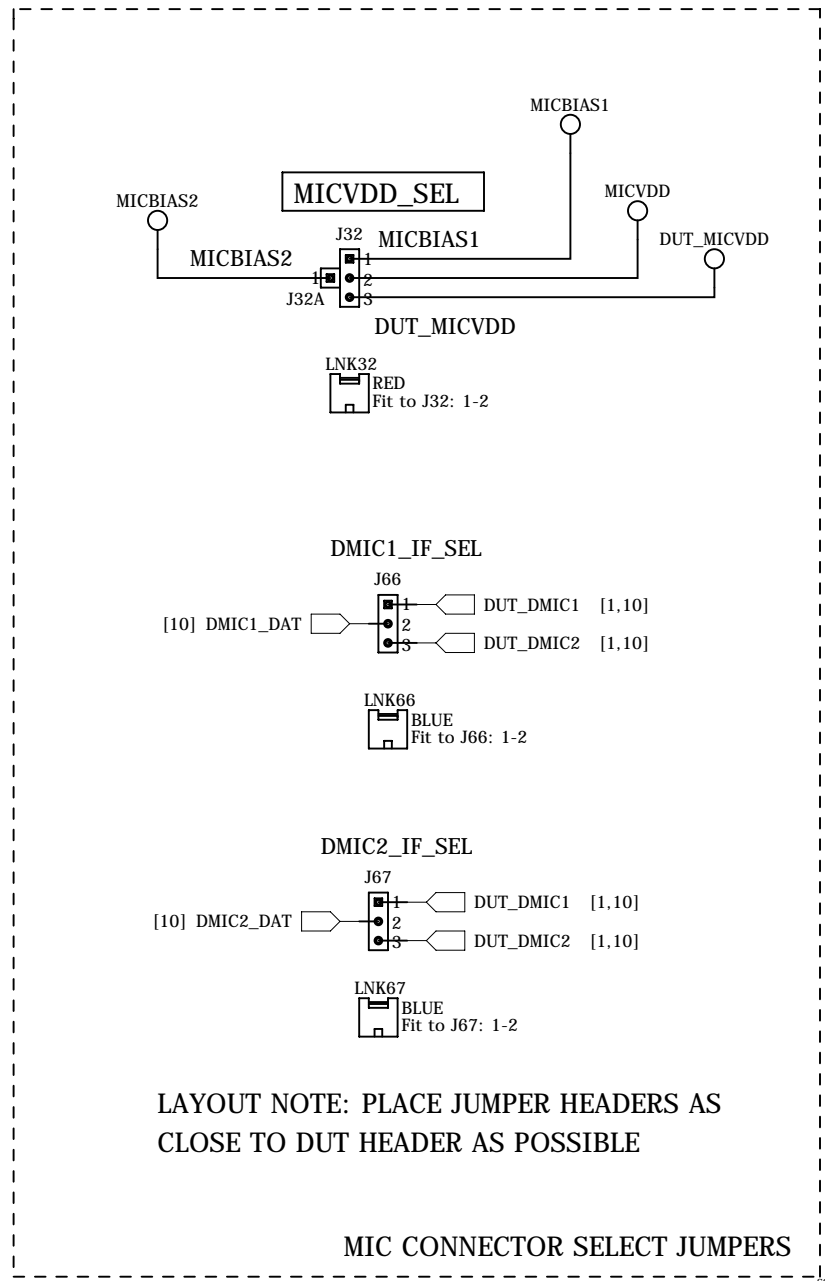
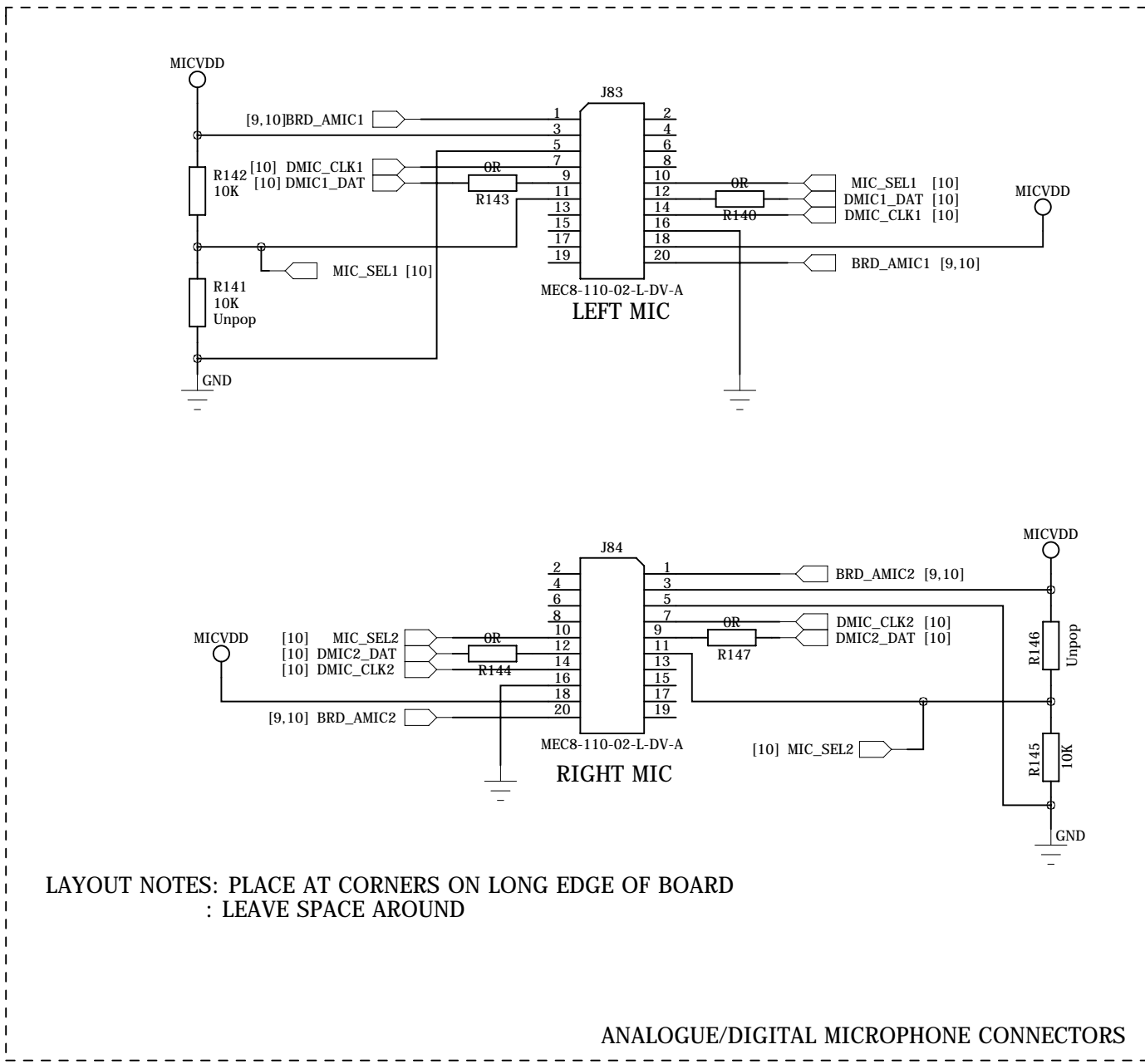
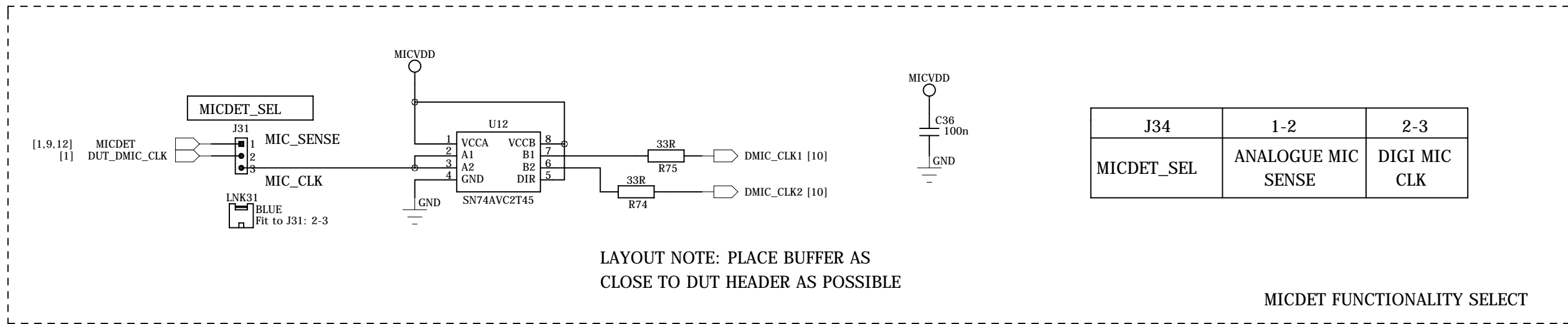


SCHMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03


CONFIDENTIAL INFORMATION

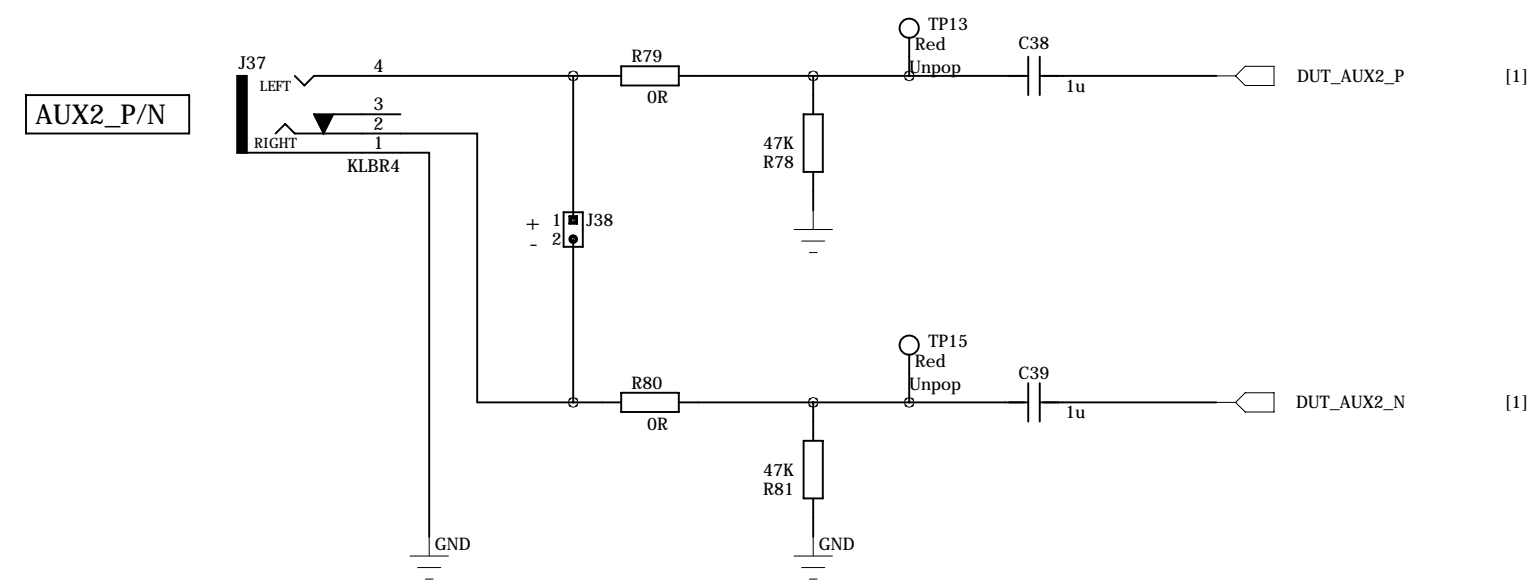
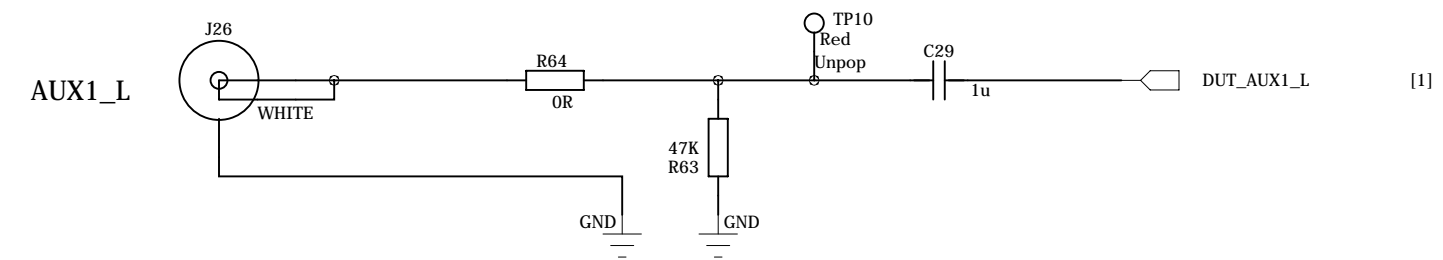
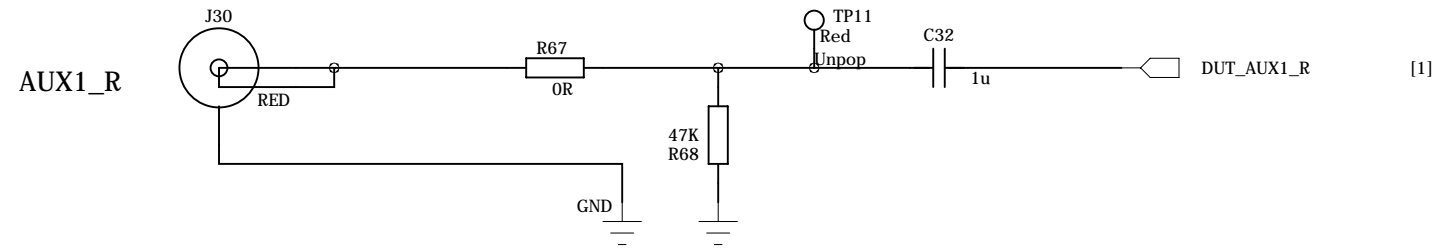
PREPARED: BL/BT	DATED: 23/04/2013
RESPONSIBLE: BT	DATED: 23/04/2013


TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
DRAWING NO: 44-179-170-01-B	REV: C
SHEET NAME: MIC_INPUT	

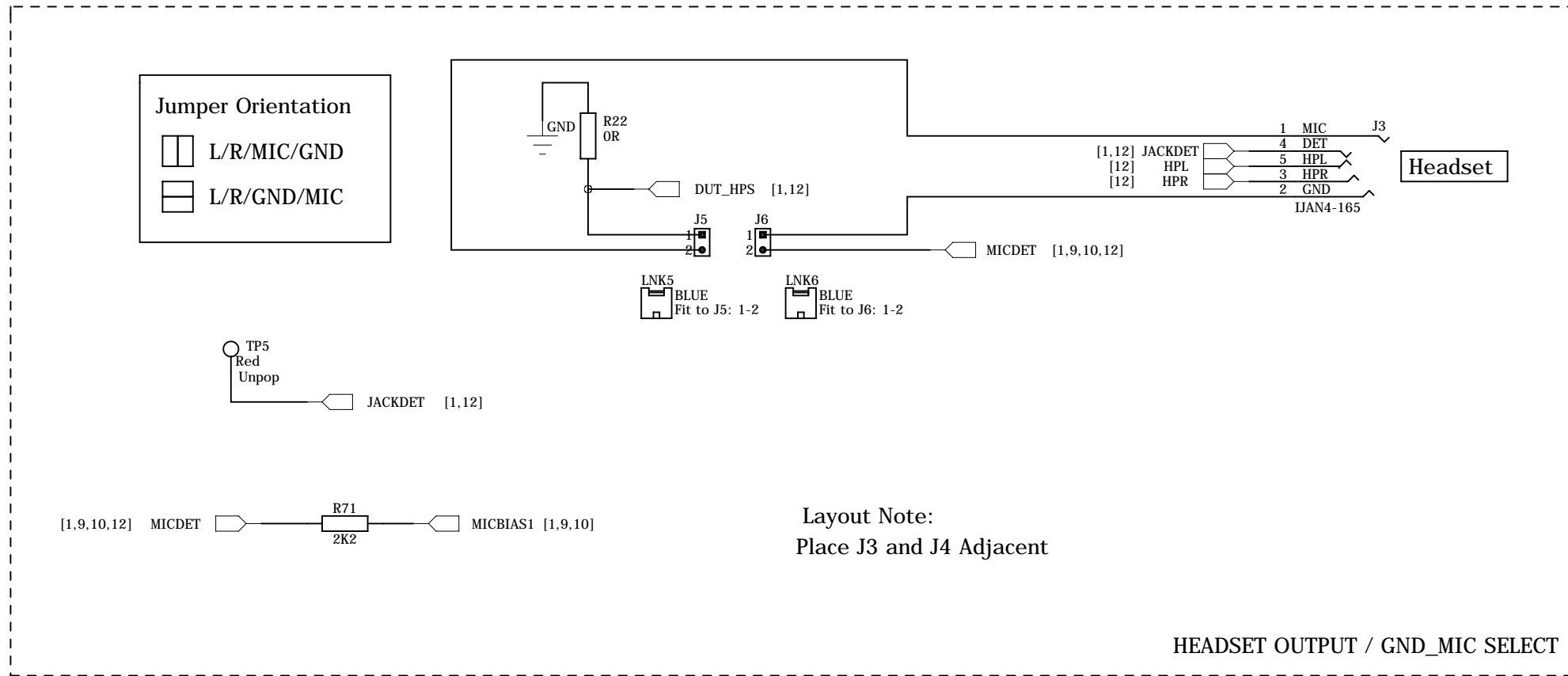
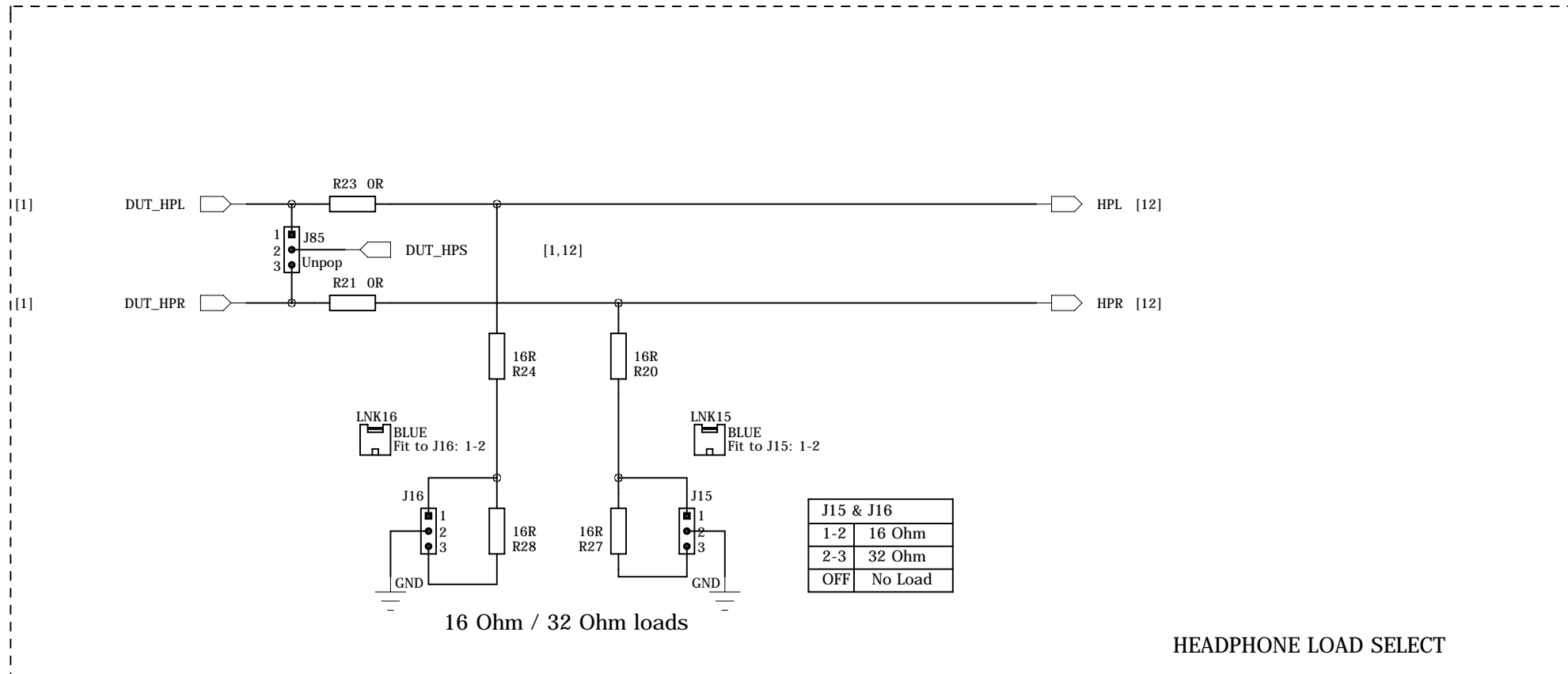


SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION		TITLE: <b>AUDIO DSP PMIC CUSTOMER EVAL BOARD</b>		
PREPARED: <b>BL/BT</b>	DATED: 23/04/2013	DRAWING NO: <b>44-179-170-01-B</b>	REV: <b>C</b>	
RESPONSIBLE: <b>BT</b>	DATED: 23/04/2013	SHEET NAME: <b>MIC_CONNECTORS</b>		PAGE: <b>10 OF 16</b>



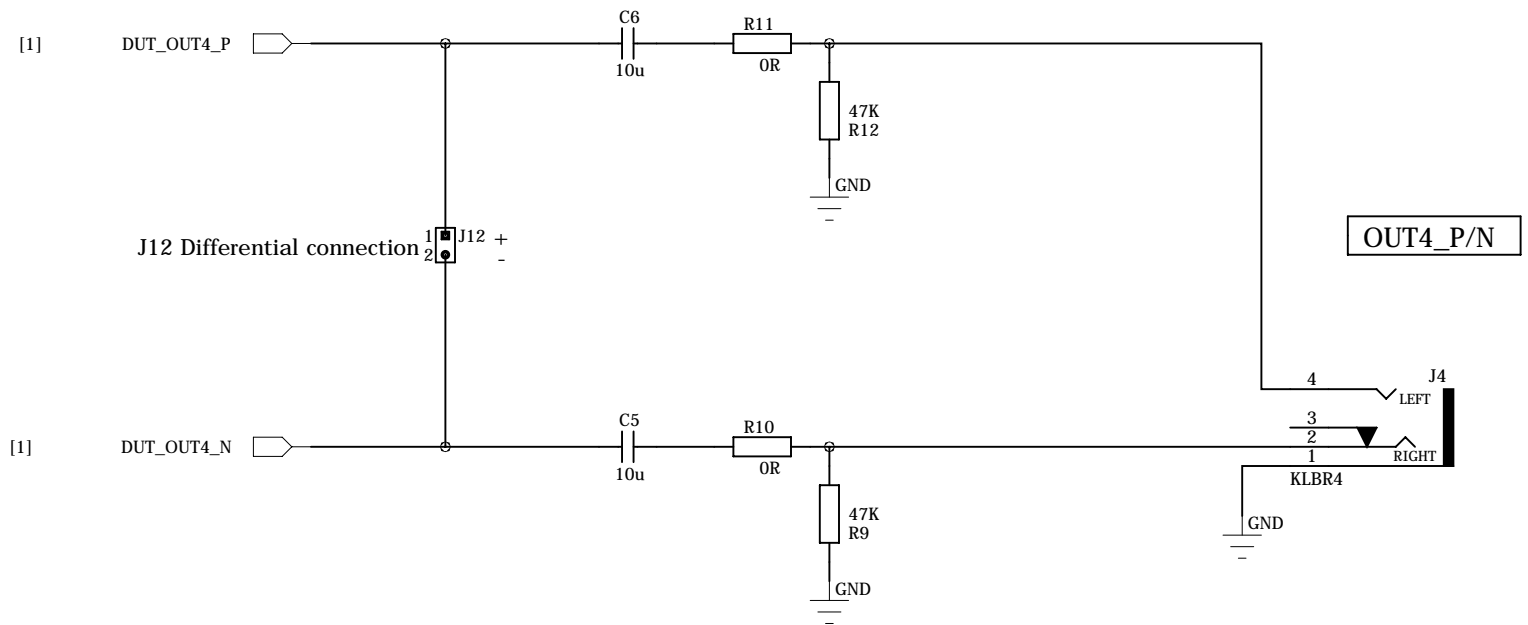
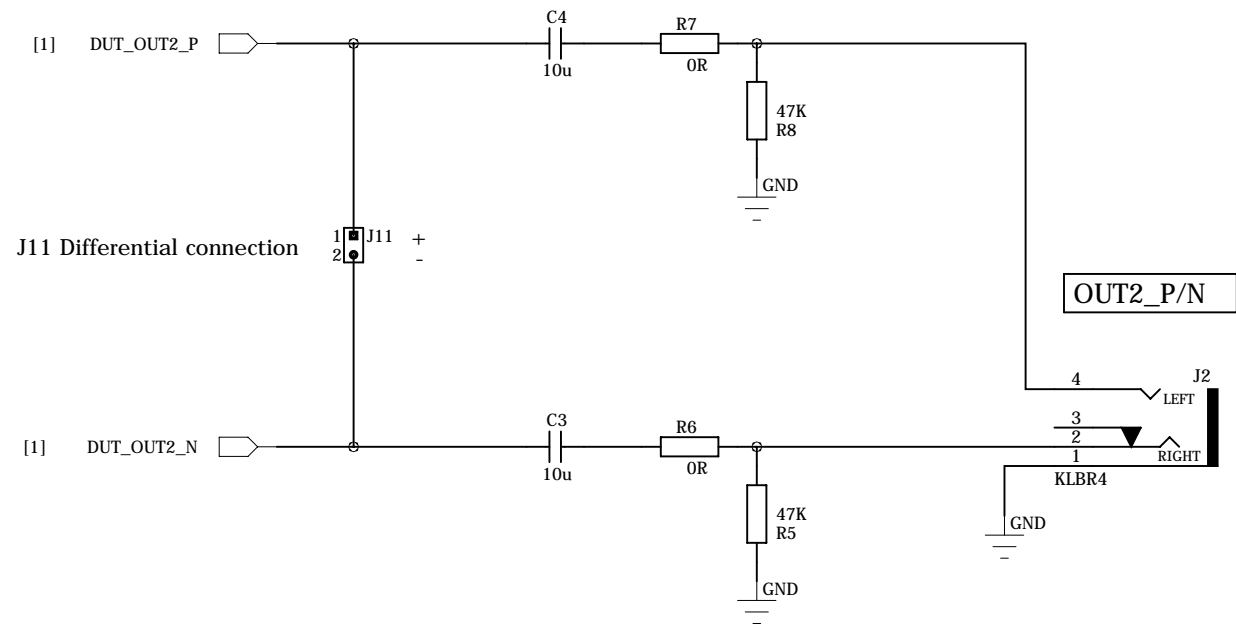
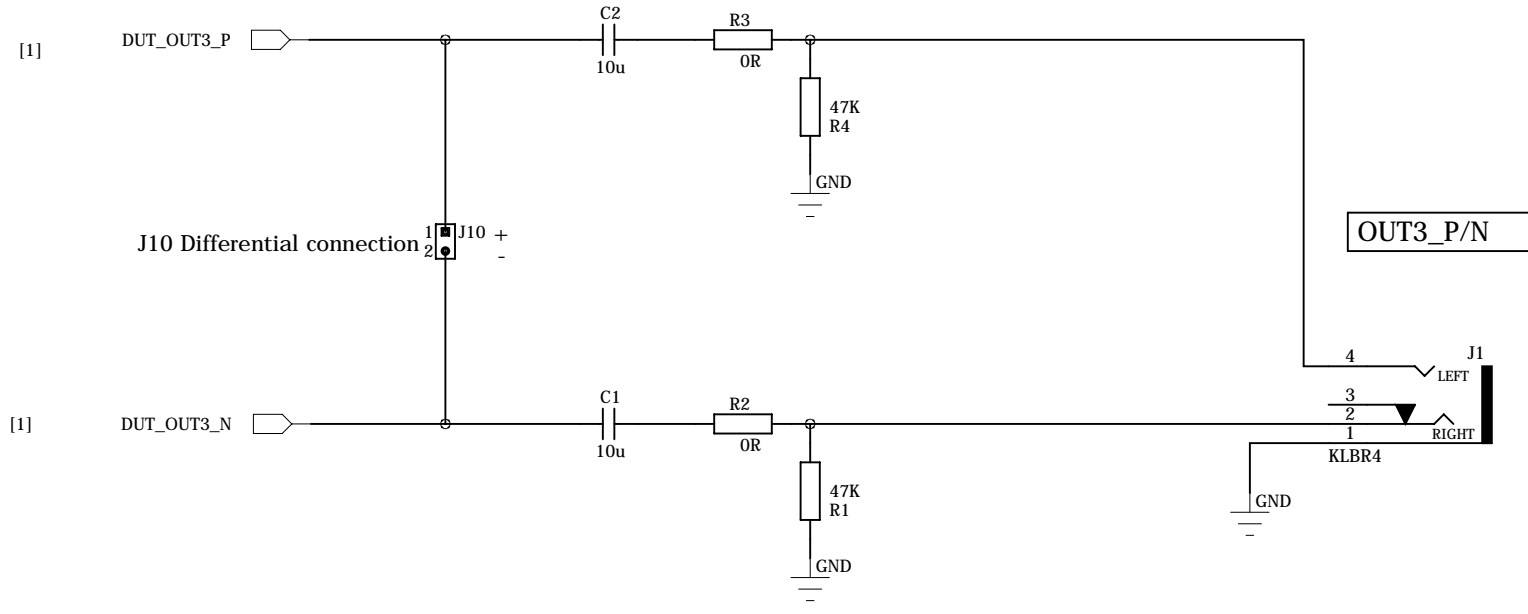
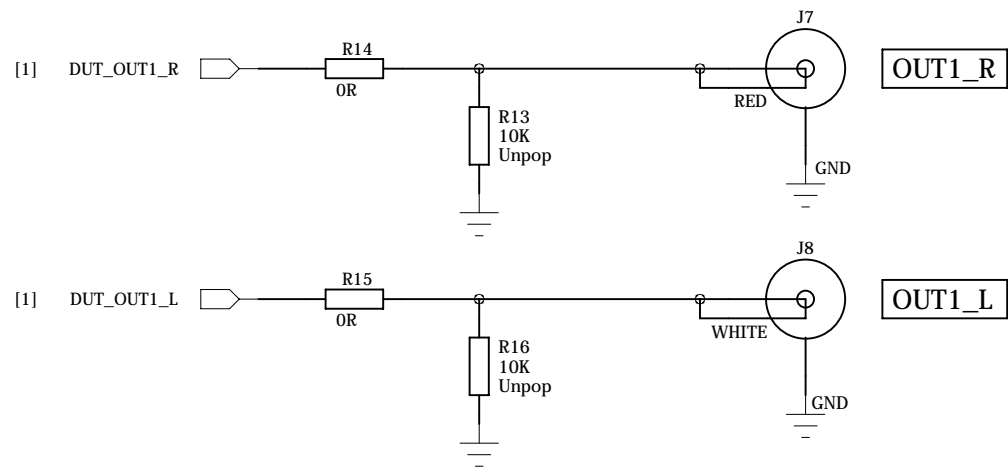
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PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C	
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: AUX_INPUT		PAGE: 11 OF 16



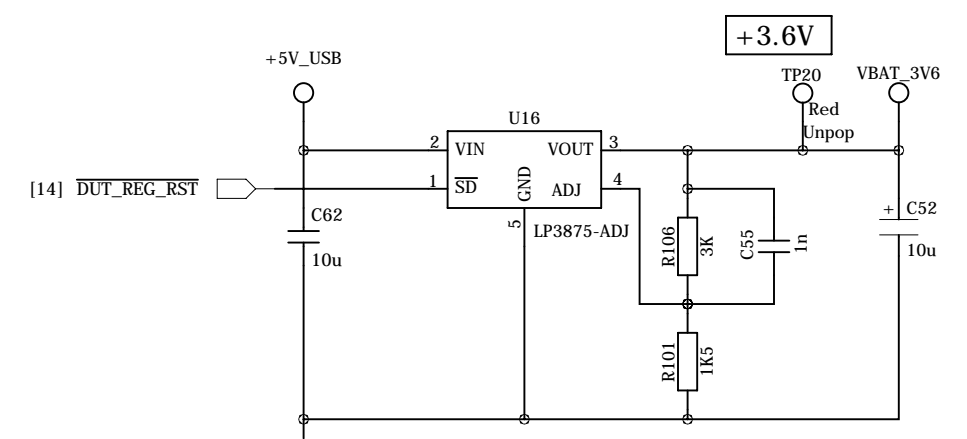
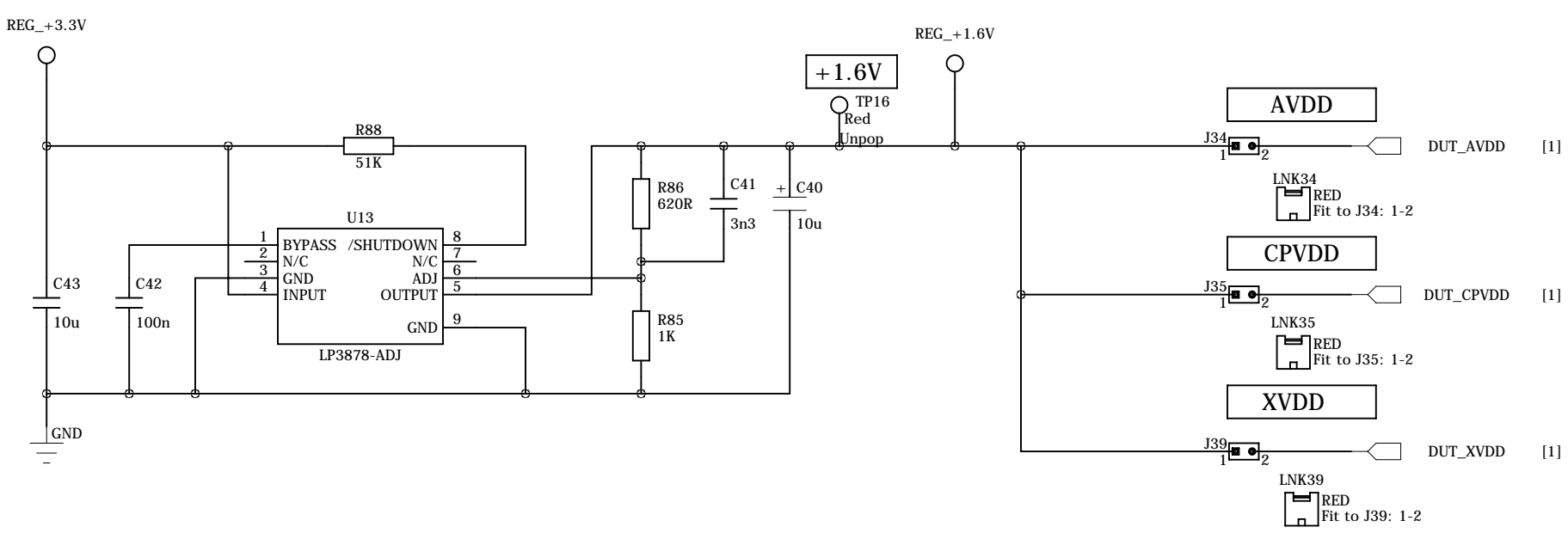
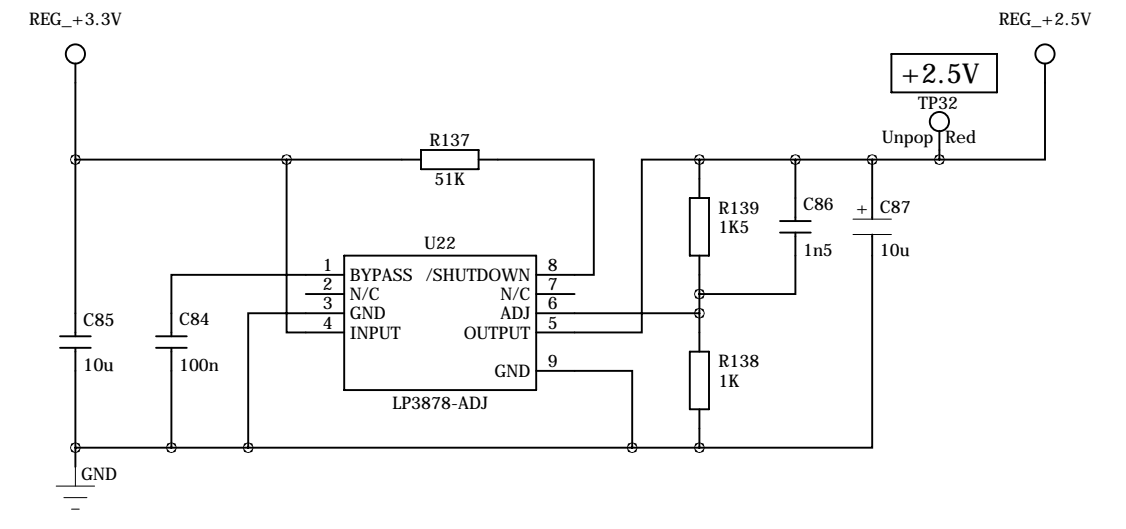
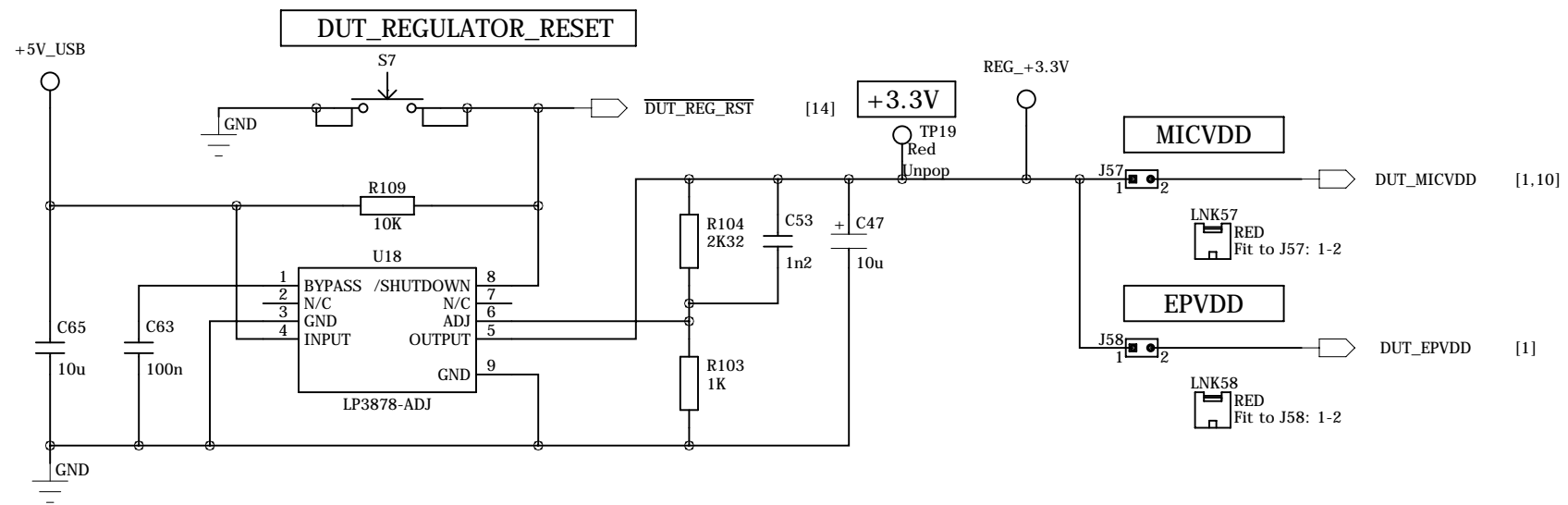
SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: HEADPHONE_HS	PAGE: 12 OF 16



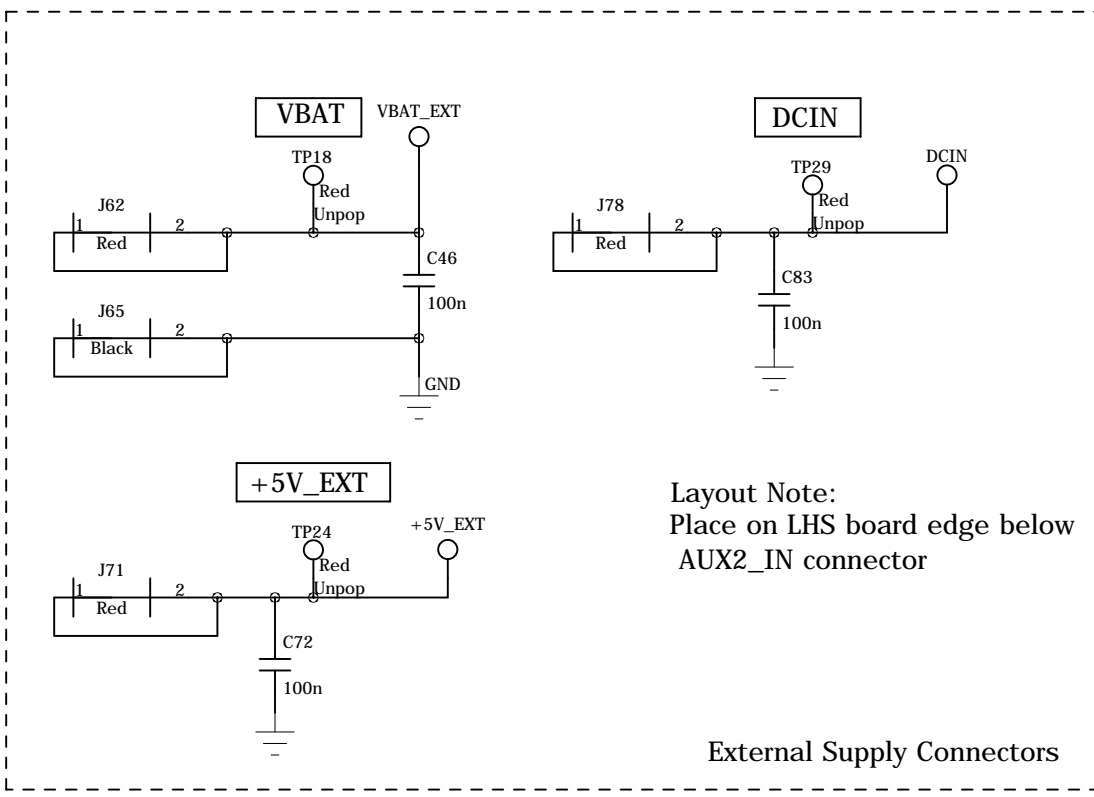
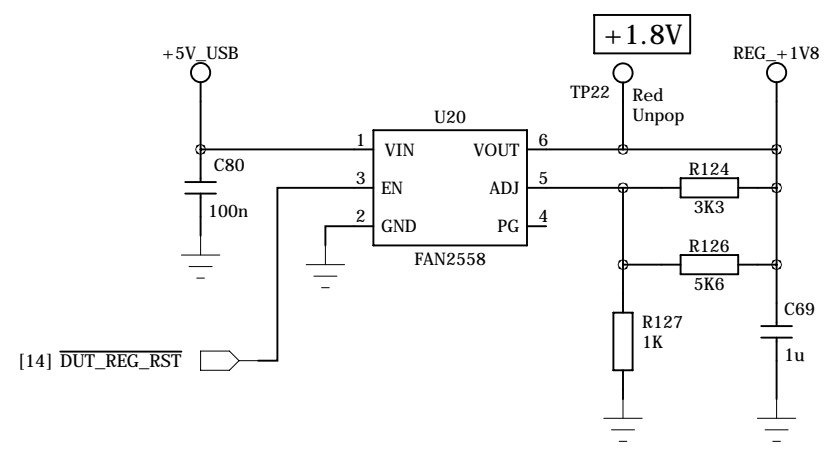


CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD		
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C	
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: LINE_OUTPUT		PAGE: 13 OF 16



Layout Note:  
Place Reg Output Capacitor within 1cm of Reg on traces directly to output and GND pins.

Design Note:  
Output Cap (including any p//l connected caps) ESR must be between 0.1 and 10 Ohms



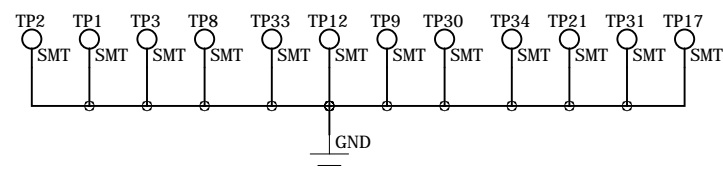
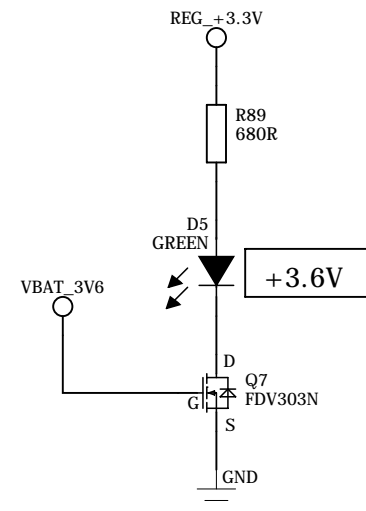
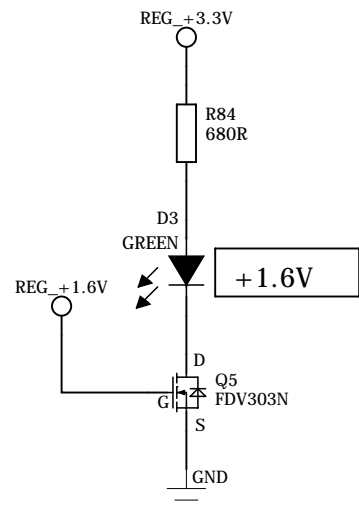
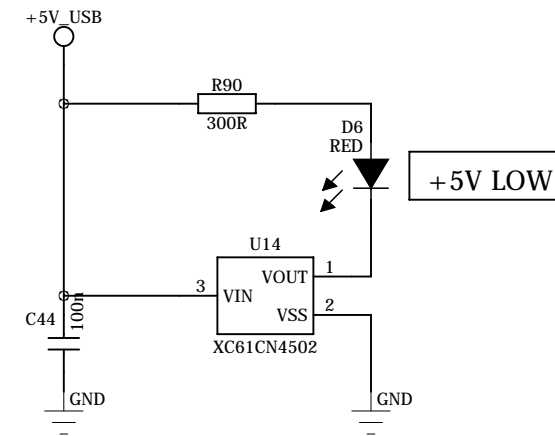
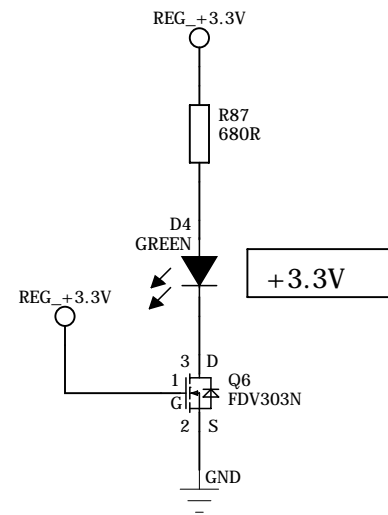
Layout Note:  
Place on LHS board edge below AUX2\_IN connector

External Supply Connectors

CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: POWER_SUPPLY	PAGE: 14 OF 16




LAYOUT NOTE: ALIGN LEDS IN ROW

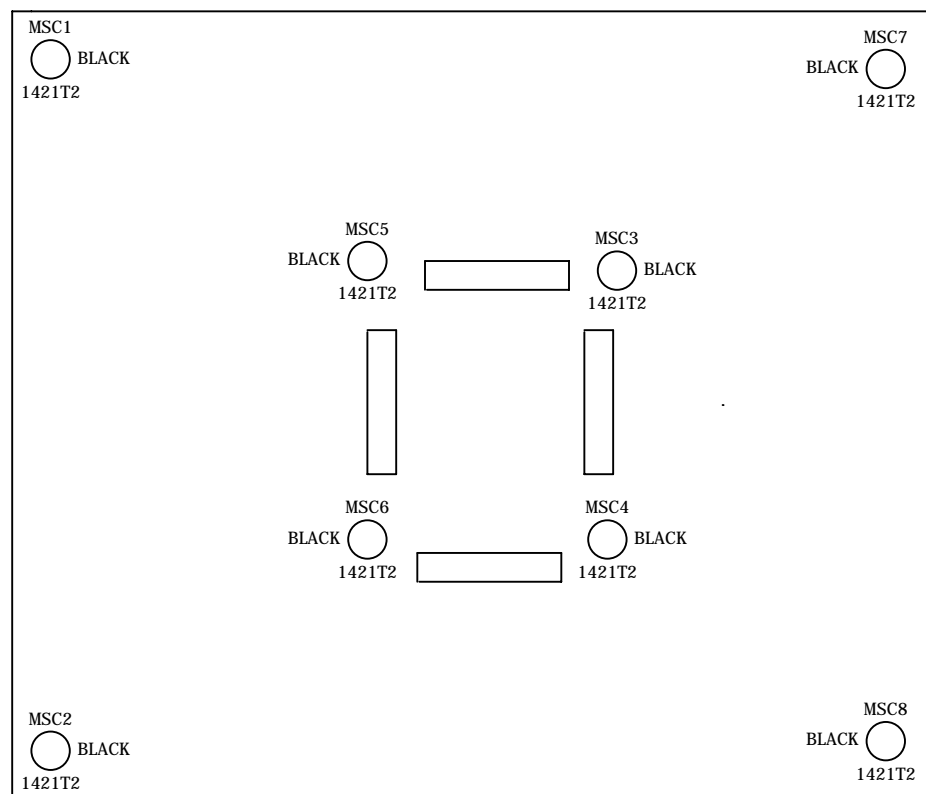


LAYOUT NOTE: SPREAD GND CONNECTORS EVENLY THROUGHOUT BOARD

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD		
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C	
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: POWER_LEDS		PAGE: 15OF 16

REV	DATE	ENGINEER	NOTES
C	28/03/2013	BL/BT	J85 (unpop 1x3 header) added.



Leave at least 20mm spacing around daughter-board header connectors  
 Rubber Feet in corners, four close to centre of the board  
 The diagram shows a suggested placement of the interfaces to this evaluation board

SCHEMATIC TEMPLATE REV PA2 (November 30, 2011) DIALOG DOCUMENT NUMBER 31-902-03

CONFIDENTIAL INFORMATION		TITLE: AUDIO DSP PMIC CUSTOMER EVAL BOARD	
PREPARED: BL/BT	DATED: 23/04/2013	DRAWING NO: 44-179-170-01-B	REV: C
RESPONSIBLE: BT	DATED: 23/04/2013	SHEET NAME: REVISION	PAGE: 16 OF 16

