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1 Introduction

The ZSSC3018 Sensor Signal Conditioner ICs is available in a RoHS-compliant QFN24 package (4mm x 4mm). This document provides details for package dimensions, pin assignments and layout, footprint, landing pattern, board connections, package marking, and thermal resistance.

2 QFN24 (4x4mm) Package Marking

Table 2.1 QFN24 Package Marking

Top Side		Comments
1 st Line	3018B	3018B = Product name
2 nd Line	YYWW	YY = Year (e.g., 15 for 2015, 16 for 2016, ...); WW = Workweek (e.g., 15)
3 rd Line	XXXXX	Last five digits of IDT lot number

3 ZSSC3018 Pin Assignments and Layout

Figure 3.1 shows the pin assignments of the QFN24 (4x4mm) package. This pin layout enables implementation of the recommended printed circuit board (PCB) design. See section 5 for specific dimensions.

Figure 3.1 Pin Layout for the ZSSC3018 QFN24 Package (4mm x 4mm)

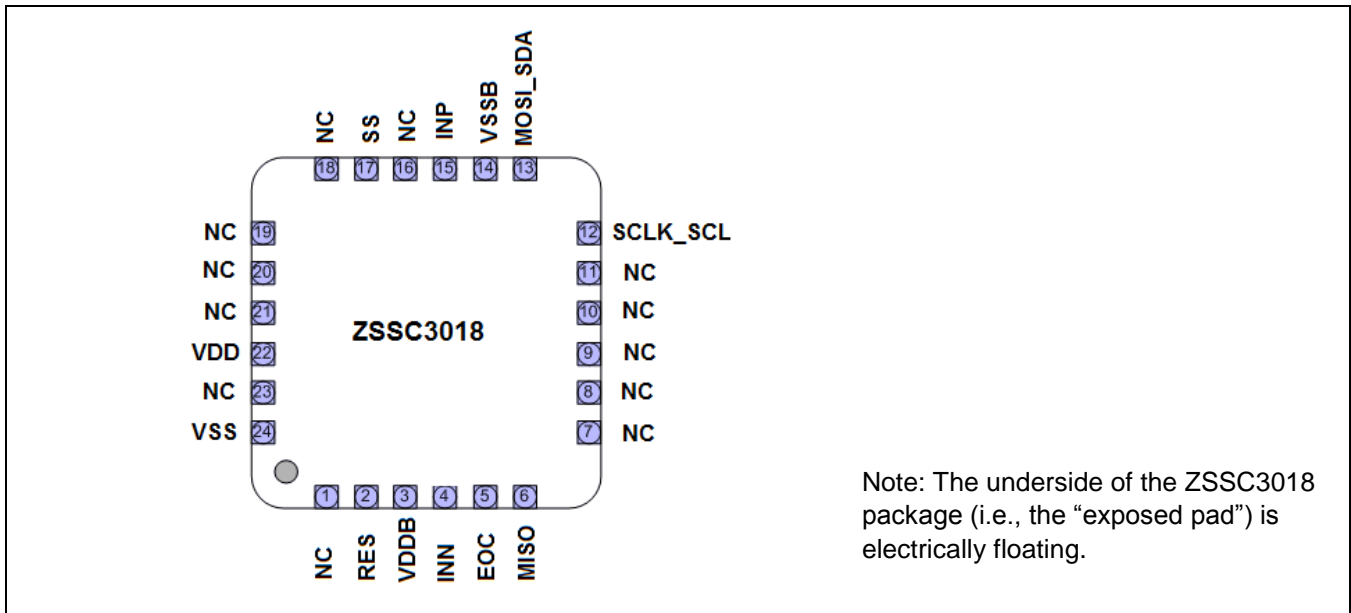


Table 3.1 ZSSC3018 Pin Assignments PQFN24

Note: In the following table, “n.c.” stands for not connected / no connection required / not bonded.

Pin No.	Name	Direction	Type	Description
1	test1	-	-	Do not connect.
2	RES	In	Digital	ZSSC3018 reset (low active, internal pull-up).
3	VDDB	Out	Analog	Positive external bridge-sensor supply.
4	INN	In	Analog	Negative sensor signal (or sensor ground for absolute voltage-source sensors).
5	EOC	Out	Digital	End of conversion or interrupt output.
6	MISO	Out	Digital	Data output for SPI.
7	test7	-	-	Do not connect.
8	n.c.	-	-	-
9	n.c.	-	-	-
10	n.c.	-	-	-
11	n.c.	-	-	-
12	SCLK_SCL	In	Digital	Clock input for SPI/I ² C.
13	MOSI_SDA	In/Out	Digital	Data input for SPI; data in/out for I ² C.
14	VSSB	Out	Analog	Negative external bridge-sensor supply (sensor ground).
15	INP	In	Analog	Positive sensor signal.
16	test16	-	-	Do not connect.
17	SS	In	Digital	Slave select for SPI.
18	test18	-	-	Do not connect.
19	test19	-	-	Do not connect.
20	n.c.	-	-	-
21	n.c.	-	-	-
22	VDD	In	Supply	IC positive supply voltage for the ZSSC3018.
23	n.c.	-	-	-
24	VSS	In	Supply	Ground reference voltage signal.
25	Exposed pad	-	-	Do not connect electrically.

4 Thermal Resistance Value for the ZSSC3018 QFN24 Package

The QFN24 (4x4mm) package has a junction-to-ambient θ_{JA} of 31.8 °C/W.

θ_{JA} has been simulated in accordance to following JEDEC-standards:

- Test Board Design as per JESD51-7.
- Natural Convection Test Conditions as per JESD51-2.

Table 4.1 ZSSC3018 Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance – junction to ambient	θ_{JA}	31.8	°C/W

5 QFN24 (4x4mm) Package Dimensions

Figure 5.1 and Table 5.1 show the package drawing and parameters for the ZSSC3018 QFN24 (4x4mm) package based on JEDEC MO-220. Dimensions are in millimeters.

Figure 5.1 Package Dimensions for the ZSSC3018 QFN24 Package

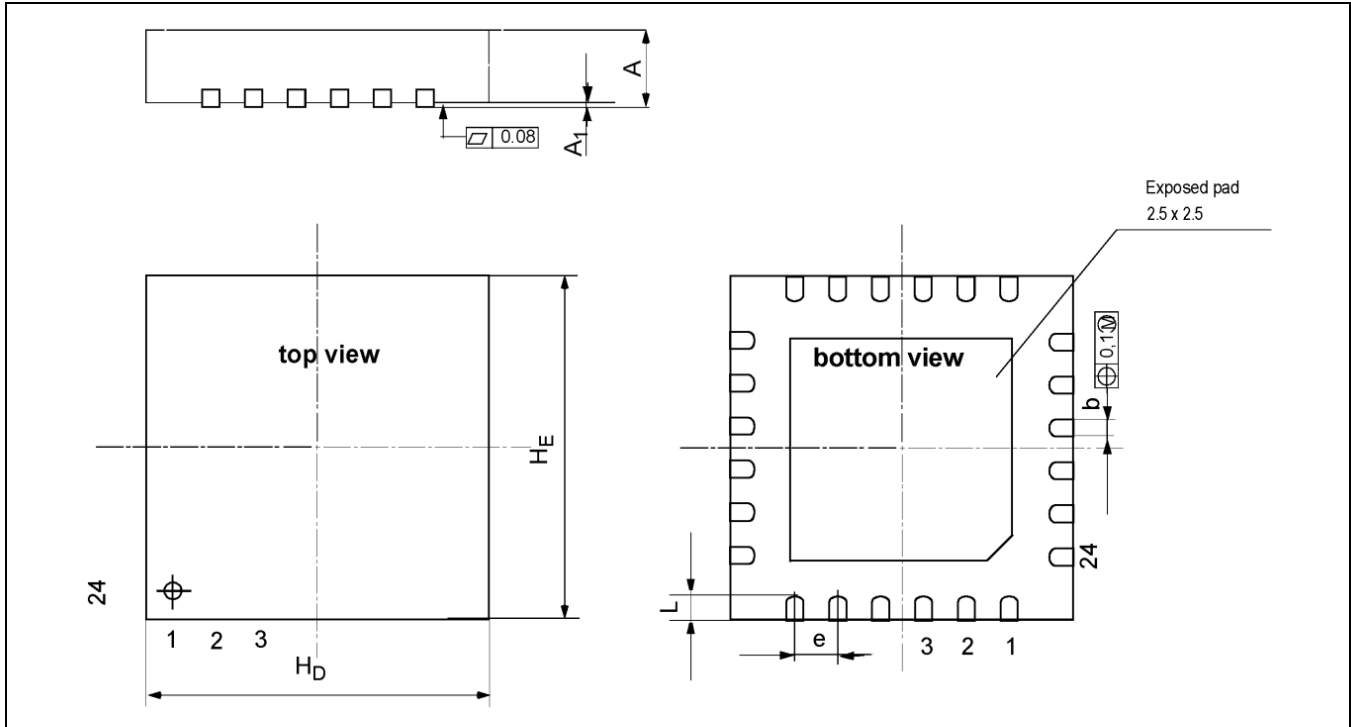


Table 5.1 QFN24 Dimensions (4mm x 4mm)

Dimension Limit	MIN	NOM	MAX
A	0.80		0.90
A ₁	0.00		0.05
b	0.20		0.30
e		0.50	
H _D	3.90		4.10
H _E	3.90		4.10
L	0.30		0.50

6 ZSSC3018 Footprint and Landing Pattern

Figure 6.1 illustrates a recommended footprint for PCB designs using the ZSSC3018 QFN24 package.

- The exposed area of the landing pattern is 0.25mm from the unit edge.
- The stencil opening excess is approximately 0.2mm from the landing pattern.

IDT also provides electronic data on its website (www.IDT.com/zssc3018).

Figure 6.1 Recommended Footprint for ZSSC3018 QFN24 Package

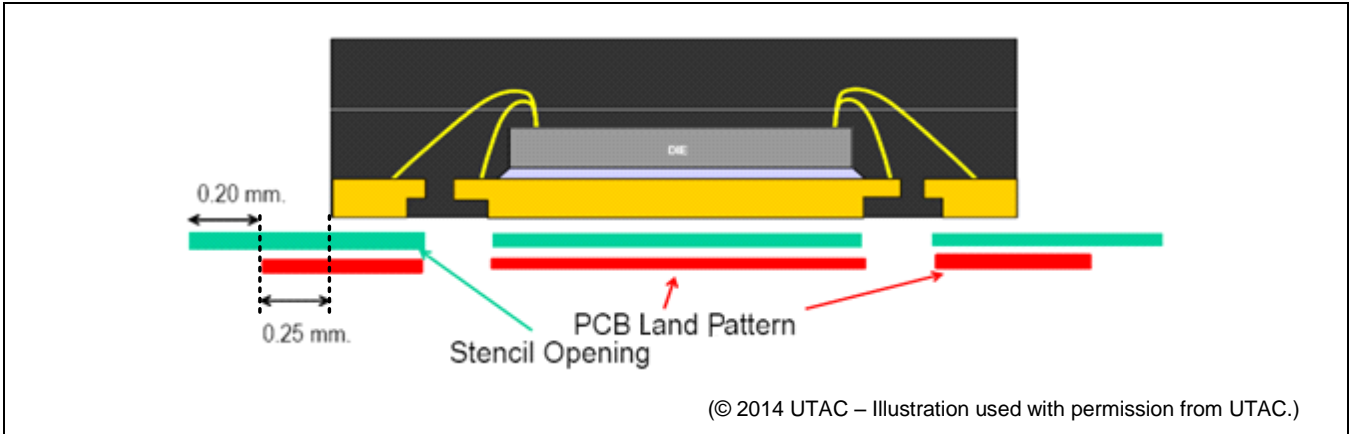
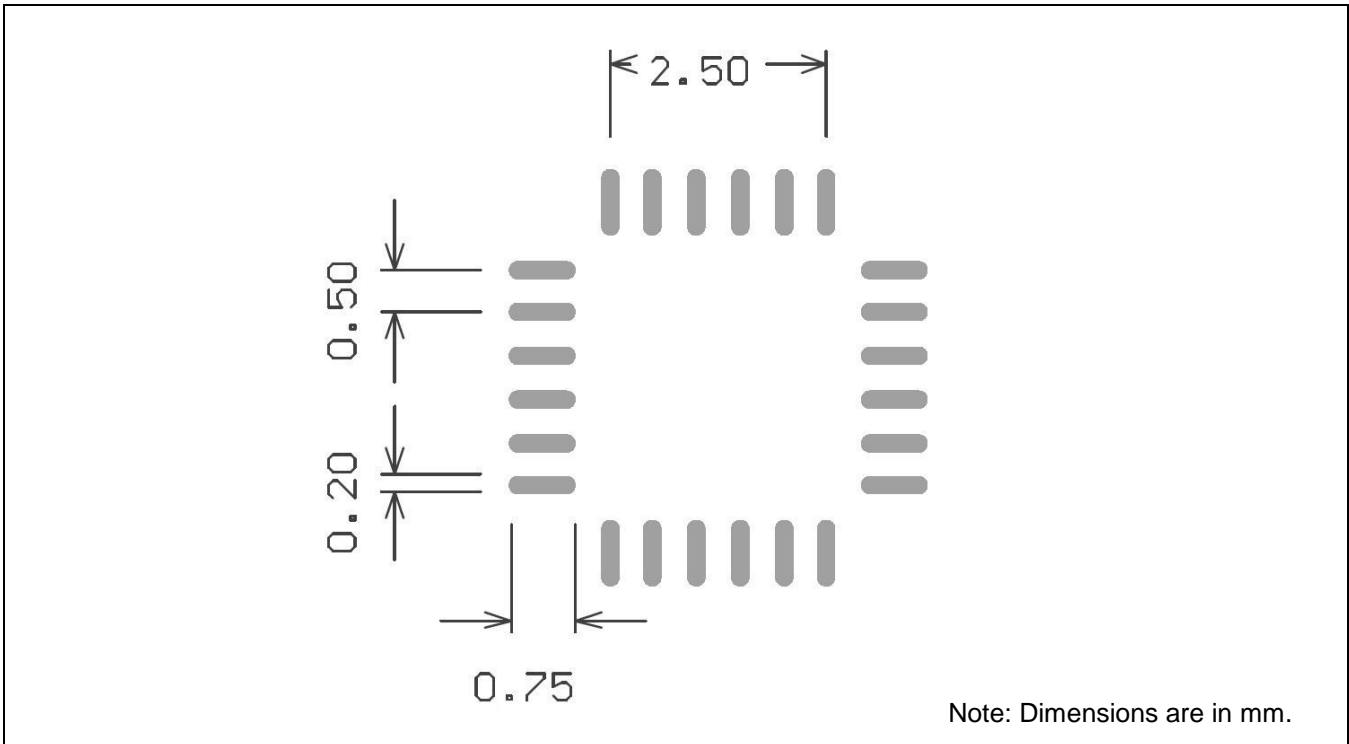


Figure 6.2 illustrates the recommended landing pattern for the ZSSC3018 QFN24 package.

Figure 6.2 Recommended Landing Pattern for ZSSC3018 QFN24 Package



7 Related Documents

Document
ZSSC3018 Data Sheet
ZSSC3018 Evaluation Kit Description

Visit the ZSSC3018 product page at www.IDT.com/ZSSC3018 or contact your nearest sales office for ordering information or the latest version of these documents.

8 Glossary

Term	Description
PCB	Printed Circuit Board
QFN	Quad Flat No Leads Package
SSC	Sensor Signal Conditioner

9 Document Revision History

Revision	Date	Description
160601	June 1, 2016	First release.

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