RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A051A/E	Rev.	1.00	
Title	Changes to Data Hold Time in Electrical Characteristics of Groups RX610, RX62G, RX621, RX62T, RX630, RX63N, and RX6		Information Category	Technical Notification			
		Lot No.		RX610 Group User's Ma Rev.1.20 (R01UH0032		dware	
Applicable Product	RX610 Group, RX62G Group, RX62N Group, RX621 Group, RX62T Group, RX630 Group, RX63N Group, RX631 Group	All	Reference Document	RX62G Group User's M Rev.1.00 (R01UH0321 RX62N Group, RX621 C Manual: Hardware Rev (R01UH0033EJ0130) RX62T Group User's Ma Rev.1.30 (R01UH0034 RX630 Group User's Ma Rev.1.50 (R01UH0040 RX63N Group, RX631 C Manual: Hardware Rev (R01UH0041EJ0160)	EJ0100) Group Use (1.30 anual: Hai EJ0130) anual: Hai EJ0150) Group Use	er's rdware rdware	

This document describes changes to the data hold time in Electrical Characteristics of RX610, RX62G, RX62N, RX621,

RX62T, RX630, RX63N, and RX631 MCUs. Changes are underlined in the list below.



RENESAS TECHNICAL UPDATE TN-RX*-A051A/E

• RX610 Group ROM (Flash Memory for Code Storage) Characteristics

Refer to Table 29.11 in RX610 Group User's Manual: Hardware Rev.1.20

Before change

ROM (Flash Memory for Code Storage) Characteristics

Conditions: V_{CC} = PLLV_{CC} = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = PLLV_{SS} = V_{REFL} = 0 V

Operating temperature range during programming/erasing:

 T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256	_	2	12	ms	PCLK = 50 MHz
	8 Kbytes	tрвк	_	45	100	ms	N _{PEC} ≤ 100
	256 bytes	t P256	_	2.4	14.4	ms	PCLK = 50 MHz
	8 Kbytes	tрвк	_	54	120	ms	NPEC > 100
Erasure time	8 Kbytes	tевк	_	50	120	ms	PCLK = 50 MHz
	64 Kbytes	te64K	—	400	875	ms	N _{PEC} ≤ 100
	128 Kbytes	t E128K	_	800	1750	ms	
	8 Kbytes	tевк	_	60	144	ms	PCLK = 50 MHz
	64 Kbytes	te64K	_	480	1050	ms	N _{PEC} > 100
	128 Kbytes	t E128K	_	960	2100	ms	
Rewrite/erase cycle*1		NPEC	1000* ²	_		Times	
Suspend delay time duri	ng writing	t SPD	_	_	120	μs	Figure 29.29
First suspend delay time suspend priority mode)	during erasing (in	tsesd1	_	_	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	—	—	1.7	ms	_
Suspend delay time during erasing (in erasure priority mode)		tseed	—	—	1.7	ms	_
Data hold time* ³		TDRP	10	_	_	Year	

Notes: 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: V_{CC} = PLLV_{CC} = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = PLLV_{SS} = V_{REFL} = 0 V

Operating temperature range during programming/erasing:

 $T_a = -20$ to +85°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle* ¹	NPEC	1000	_	_	Times	
Data hold time	Tdrp	<u>30*2</u>	—	—	Year	<u>Ta = +85°C</u>

Notes: 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

2. This value is based on the result of the reliability test.

ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: V_{CC} = PLLV_{CC} = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = PLLV_{SS} = V_{REFL} = 0 V

Operating temperature range during programming/erasing:

 $T_a = -20$ to +85°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256		2	12	ms	PCLK = 50 MHz
	8 Kbytes	tрвк	_	45	100	ms	N _{PEC} ≤ 100
	256 bytes	t P256		2.4	14.4	ms	PCLK = 50 MHz
	8 Kbytes	tрвк	_	54	120	ms	NPEC > 100
Erasure time	8 Kbytes	tesk		50	120	ms	PCLK = 50 MHz
	64 Kbytes	te64K	_	400	875	ms	N _{PEC} ≤ 100
	128 Kbytes	t E128K	_	800	1750	ms	
	8 Kbytes	tевк	_	60	144	ms	PCLK = 50 MHz
	64 Kbytes	te64K	_	480	1050	ms	N _{PEC} > 100
	128 Kbytes	t Е128К	_	960	2100	ms	
Suspend delay time dur	ring writing	t SPD	_	_	120	μs	Figure 29.29
First suspend delay time during erasing (in suspend priority mode)		tsesd1	_	—	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	_	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		tseed	_	_	1.7	ms	



RENESAS TECHNICAL UPDATE TN-RX*-A051A/E

• RX610 Group Data Flash (Flash Memory for Data Storage) Characteristics

Refer to Table 29.12 in RX610 Group User's Manual: Hardware Rev.1.20

Before change

Data Flash (Flash Memory for Data Storage) Characteristics

Conditions: V_{CC} = PLLV_{CC} = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = PLLV_{SS} = V_{REFL} = 0 V

Operating temperature range during programming/erasing:

 T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	_	0.4	2	ms	PCLK = 50-MHz
	128 bytes	t DP128	—	1	5	ms	operation
Erasure time	8 Kbytes	tdesk	_	300	900	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	tdbc8	_	_	30	μs	PCLK = 50-MHz
	8 Kbytes	tdвсак	_		2.5	ms	operation
Rewrite/erase cycle*1		NDPEC	30000* ²		_	Times	
Suspend delay time dur	ing writing	t DSPD	_		120	μs	Figure 29.29
First suspend delay time suspend priority mode)	e during erasing (in	tDSESD1	_	_	120	μs	PCLK = 50-MHz operation
Second suspend delay time during erasing (in suspend priority mode)		tdsesd2	_	_	1.7	ms	_
Suspend delay time during erasing (in erasure priority mode)		tdseed	_	_	1.7	ms	
Data hold time ^{*3}		TDDRP	10		_	Year	

Notes: 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



Data Flash (Flash Memory for Data Storage) Characteristics (1)

Conditions: V_{CC} = PLLV_{CC} = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = PLLV_{SS} = V_{REFL} = 0 V

Operating temperature range during programming/erasing:

 T_a = -20 to +85°C (regular specifications), T_a = -40 to +85°C (wide-range specifications)

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle* ¹	NDPEC	30000	_	_	Times	
Data hold time	TDDRP	<u>30*2</u>	—	—	Year	<u>T_a = +85°C</u>

Notes: 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 64 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

2. This value is based on the result of the reliability test.

Data Flash (Flash Memory for Data Storage) Characteristics (2)

Conditions: V_{CC} = PLLV_{CC} = AV_{CC} = 3.0 to 3.6 V, V_{REFH} = 3.0 V to AV_{CC}, V_{SS} = PLLV_{SS} = V_{REFL} = 0 V

Operating temperature range during programming/erasing:

 $T_a = -20$ to +85°C (regular specifications), $T_a = -40$ to +85°C (wide-range specifications)

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	_	0.4	2	ms	PCLK = 50-MHz operation
	128 bytes	t _{DP128}	_	1	5	ms	
Erasure time	8 Kbytes	tde8k	_	300	900	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	tdbc8	_	_	30	μs	PCLK = 50-MHz
	8 Kbytes	t двс8к	_	_	2.5	ms	operation
Suspend delay time dur	ing writing	t dspd	_	_	120	μs	Figure 29.29
First suspend delay time during erasing (in suspend priority mode)		tDSESD1	_	_	120	μs	PCLK = 50-MHz operation
Second suspend delay time during erasing (in suspend priority mode)		tdsesd2	_	_	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		tdseed	_	_	1.7	ms	



 RX62G Group ROM (Flash Memory for Code Storage) Characteristics Refer to Table 33.20 in RX62G Group User's Manual: Hardware Rev.1.00

Before change

ROM (Flash Memory for Code Storage) Characteristics

VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Temperature range for the programming/erasure operation: Ta = -40 to +85°C.

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256	_	2	12	ms	PCLK = 50 MHz
	4 Kbytes	tР4К	—	23	50	ms	N _{PEC} ≤ 100
	16 Kbytes	t Р16К	—	90	200	ms	
	256 bytes	t P256	—	2.4	14.4	ms	PCLK = 50 MHz
	4 Kbytes	t Р4К	—	27.6	60	ms	NPEC > 100
	16 Kbytes	t Р16К	—	108	240	ms	
Erasure time	ure time 4 Kbytes t _{E4K}	—	25	60	ms	PCLK = 50 MHz	
	16 Kbytes	t е16К	—	100	240	ms	N _{PEC} ≤ 100
	4 Kbytes	te₄ĸ	—	30	72	ms	PCLK = 50 MHz
	16 Kbytes	te16ĸ	—	120	288	ms	N _{PEC} > 100
Rewrite/erase cycle*1		NPEC	1000* ²	—	—	Times	
Suspend delay time during	g writing	t spd	—	—	120	μs	Figure 33.24
	First suspend delay time during erasing (in suspend priority mode)		-	-	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		tseed	—	—	1.7	ms	
Data hold time*3		TDRP	10	—	—	Year	

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



ROM (Flash Memory for Code Storage) Characteristics (1)

VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation: Ta = -40 to $+85^{\circ}C$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	NPEC	1000	_	_	Times	
Data hold time	Tdrp	<u>30*2</u>			Year	<u>Ta = +85°C</u>

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

ROM (Flash Memory for Code Storage) Characteristics (2)

VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation: Ta = -40 to +85°C

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256	—	2	12	ms	PCLK = 50 MHz
	4 Kbytes	t₽4ĸ	—	23	50	ms	N _{PEC} ≤ 100
	16 Kbytes	t Р16К	—	90	200	ms	PCLK = 50 MHz
	256 bytes	t P256	—	2.4	14.4	ms	Npec > 100
	4 Kbytes	t₽4ĸ	—	27.6	60	ms	
	16 Kbytes	t Р16К	—	108	240	ms	PCLK = 50 MHz
Erasure time	4 Kbytes	te₄ĸ	—	25	60	ms	N _{PEC} ≤ 100
	16 Kbytes	t Е16К	—	100	240	ms	PCLK = 50 MHz
	4 Kbytes	te₄ĸ	—	30	72	ms	N _{PEC} > 100
	16 Kbytes	te16к	—	120	288	ms	
Suspend delay time du	ring writing	tspd	—	—	120	μs	Figure 33.24
First suspend delay time during erasing (in suspend priority mode)		tsesd1	-	—	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	—	—	1.7	ms	
	Suspend delay time during erasing (in erasure priority mode)		—	—	1.7	ms	



RX62G Group Data Flash (Flash Memory for Data Storage) Characteristics

Refer to Table 33.21 in RX62G Group User's Manual: Hardware Rev.1.00

Before change

Data Flash (Flash Memory for Data Storage) Characteristics

VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Temperature range for the programming/erasure operation: Ta = -40 to $+85^{\circ}$ C.

ltem		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK =
	128 bytes	t DP128	—	1	5	ms	50 MHz
Erasure time	2 Kbytes	tde2k	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	tdbc8	—	—	30	μs	PCLK =
	2 Kbytes	tdbc2k	—	—	0.7	ms	50 MHz
Rewrite/erase cycle*1		NDPEC	30000* ²	—	—	Times	
Suspend delay time du	ring writing	t dspd	-	—	120	μs	Figure 33.24
First suspend delay tim (in suspend priority mo		tDSESD1	—	_	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tdsesd2	—	_	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		tdseed	—	_	1.7	ms	
Data hold time* ³		TDDRP	10	_	_	Year	

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



Data Flash (Flash Memory for Data Storage) Characteristics (1)

VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation: Ta = -40 to $+85^{\circ}C$.

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	NDPEC	30000	_	_	Times	
Data hold time	TDDRP	<u>30*2</u>		_	Year	<u>T_a = +85°C</u>

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

Data Flash (Flash Memory for Data Storage) Characteristics (2)

VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation: Ta = -40 to $+85^{\circ}C$.

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	_	0.4	2	ms	PCLK = 50 MHz
	128 bytes	tDP128	—	1	5	ms	
Erasure time	2 Kbytes	tde2k	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	tdbc8	—	_	30	μs	PCLK = 50 MHz
	2 Kbytes	tdвc2к	—	—	0.7	ms	
Suspend delay time du	ring writing	tdspd	—	_	120	μs	Figure 33.24
First suspend delay time during erasing (in suspend priority mode)		tDSESD1	-	—	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	-	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		tdseed	-	—	1.7	ms	



 RX62N Group, RX621 Group ROM (Flash Memory for Code Storage) Characteristics Refer to Table 41.25 in RX62N Group, RX621 Group User's Manual: Hardware Rev.1.30

Before change

ROM (Flash Memory for Code Storage) Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6V, VREFH = 2.7V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256	_	2	12	ms	PCLK = 50 MHz
	4 Kbytes	tр4к	_	23	50	ms	N _{PEC} ≤ 100
	16 Kbytes	t Р16К	—	90	200	ms	
	256 bytes	t P256	—	2.4	14.4	ms	PCLK = 50 MHz
	4 Kbytes	t₽4ĸ	_	27.6	60	ms	N _{PEC} > 100
	16 Kbytes	t р16К	—	108	240	ms	<u> </u>
Erasure time	4 Kbytes	te4ĸ	—	25	60	ms	PCLK = 50 MHz
	16 Kbytes	t E16К	—	100	240	ms	N _{PEC} ≤ 100
	4 Kbytes	te4ĸ	—	30	72	ms	PCLK = 50 MHz
	16 Kbytes	t E16К	—	120	288	ms	N _{PEC} > 100
Rewrite/erase cycle*1		NPEC	1000* ²	—	—	Times	
Suspend delay time durin	g writing	tspd	—	—	120	μs	Figure 41.67
First suspend delay time during erasing (in suspend priority mode)		tsesd1	—	—	120	μs	PCLK = 50-MHz operation
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	—	-	1.7	ms	oporation
Suspend delay time during erasing (in erasure priority mode)		tseed	—	—	1.7	ms	
Data hold time*3		TDRP	10	_	_	Year	

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6V, VREFH = 2.7V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	NPEC	1000	_	_	Times	
Data hold time	Tdrp	<u>30*2</u>	_	_	Year	<u>Ta = +85°C</u>

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

• ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = PLLVCC = AVCC = VCC USB = 2.7 to 3.6V, VREFH = 2.7V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0V

Temperature range for the programming/erasure operation: T_a = -40 to +85°C

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256	—	2	12	ms	PCLK = 50 MHz
	4 Kbytes	t Р4К	—	23	50	ms	N _{PEC} ≤ 100
	16 Kbytes	t P16K	—	90	200	ms	
	256 bytes	t P256	—	2.4	14.4	ms	PCLK = 50 MHz
	4 Kbytes	t Р4К	—	27.6	60	ms	N _{PEC} > 100
	16 Kbytes	t P16K	—	108	240	ms	
Erasure time	4 Kbytes	te₄ĸ	—	25	60	ms	PCLK = 50 MHz
	16 Kbytes	te16K	—	100	240	ms	N _{PEC} ≤ 100
	4 Kbytes	te4ĸ	—	30	72	ms	PCLK = 50 MHz
	16 Kbytes	te16K	—	120	288	ms	N _{PEC} > 100
Suspend delay time durin	g writing	t SPD	—	_	120	μs	Figure 41.67
First suspend delay time during erasing (in suspend priority mode)		tsesd1	—	—	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	_	—	1.7	ms	
Suspend delay time durin (in erasure priority mode)		tseed	-	—	1.7	ms	



RENESAS TECHNICAL UPDATE TN-RX*-A051A/E

 RX62N Group, RX621 Group Data Flash (Flash Memory for Data Storage) Characteristics Refer to Table 41.26 in RX62N Group, RX621 Group User's Manual: Hardware Rev.1.30

Before change

Data Flash (Flash Memory for Data Storage) Characteristics

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6V, VREFH = 2.7V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0V

Temperature range for the programming/erasure operation: Ta = -40 to +85°C

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK = 50-MHz
	128 bytes	t DP128	—	1	5	ms	operation
Erasure time	2 Kbytes	tde2k	-	70	250	ms	PCLK = 50-MHz operation
Blank check time	8 bytes	tdbc8	—	—	30	μs	PCLK = 50-MHz
	2 Kbytes	tdbc2k	—	_	0.7	ms	operation
Rewrite/erase cycle*1		NDPEC	30000* ²	—	_	Times	
Suspend delay time duri	ng writing	t DSPD	—	—	120	μs	Figure 41.67
First suspend delay time (in suspend priority mode		tDSESD1	—	-	120	μs	PCLK = 50-MHz operation
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	—	—	1.7	ms]
Suspend delay time duri (in erasure priority mode		tdseed	—	-	1.7	ms	
Data hold time*3		TDDRP	10	_	_	Year	

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



Data Flash (Flash Memory for Data Storage) Characteristics (1)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6V, VREFH = 2.7V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0V

Temperature range for the programming/erasure operation: Ta = -40 to +85°C

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	NDPEC	30000	_	_	Times	
Data hold time	TDDRP	<u>30*2</u>	_		Year	<u>T_a = +85°C</u>

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

Data Flash (Flash Memory for Data Storage) Characteristics (2)

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6V, VREFH = 2.7V to AVCC

VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0V

Temperature range for the programming/erasure operation: Ta = -40 to +85°C

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	_	0.4	2	ms	PCLK = 50 MHz
	128 bytes	t DP128	—	1	5	ms	
Erasure time	2 Kbytes	tde2k	—	70	250	ms	PCLK = 50 MHz
,	8 bytes	tdbc8	—	—	30	μs	PCLK = 50 MHz
	2 Kbytes	tdbc2k	—	_	0.7	ms	
Suspend delay time durin	g writing	t dspd	—	_	120	μs	Figure 41.67
First suspend delay time during erasing (in suspend priority mode)		tDSESD1	-	-	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	—	—	1.7	ms	
Suspend delay time durin (in erasure priority mode)		tdseed	—	—	1.7	ms	



 RX62T Group ROM (Flash Memory for Code Storage) Characteristics Refer to Table 33.19 in RX62T Group User's Manual: Hardware Rev.1.30

Before change

ROM (Flash Memory for Code Storage) Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = -40 to +85°C. Ta is the same under conditions 1 to 3.

ltem		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	256 bytes	t P256	_	2	12	ms	PCLK = 50 MHz
	4 Kbytes	t₽4ĸ	—	23	50	ms	N _{PEC} ≤ 100
	16 Kbytes	t Р16К	—	90	200	ms	
	256 bytes	t P256	—	2.4	14.4	ms	PCLK = 50 MHz
	4 Kbytes	t₽4ĸ	—	27.6	60	ms	N _{PEC} > 100
	16 Kbytes	t Р16К	—	108	240	ms	
Erasure time	4 Kbytes	te₄ĸ	—	25	60	ms	PCLK = 50 MHz
	16 Kbytes	te16ĸ	—	100	240	ms	N _{PEC} ≤ 100
	4 Kbytes	te₄ĸ	—	30	72	ms	PCLK = 50 MHz
	16 Kbytes	te16ĸ	—	120	288	ms	N _{PEC} > 100
Rewrite/erase cycle*1		NPEC	1000* ²	—	—	Times	
Suspend delay time durin	g writing	tspd	—	—	120	μs	Figure 33.24
First suspend delay time during erasing (in suspend priority mode) Second suspend delay time during erasing (in suspend priority mode)		tsesd1	—	—	120	μs	PCLK = 50 MHz
		tsesd2	-	—	1.7	ms	
Suspend delay time durin (in erasure priority mode)	0 0	tseed	—	_	1.7	ms	
Data hold time*3		TDRP	10	_	_	Year	

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



ROM (Flash Memory for Code Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = -40 to $+85^{\circ}$ C. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle* ¹	NPEC	1000	_	_	Times	
Data hold time	Tdrp	<u>30*2</u>			Year	<u>Ta = +85°C</u>

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = -40 to +85°C. Ta is the same under conditions 1 to 3. Тур. **Test Conditions** Item Symbol Min. Max. Unit Programming time 256 bytes 2 12 ms PCLK = 50 MHz tp256 4 Kbytes t₽4ĸ 23 50 ms N_{PEC} ≤ 100 16 Kbytes **t**P16K 90 200 ms _ 2.4 14.4 256 bytes **t**P256 ms PCLK = 50 MHz 4 Kbvtes 27.6 60 ms N_{PEC} > 100 t₽4ĸ 108 240 16 Kbytes **t**P16K ms Erasure time t_{E4K} _ PCLK = 50 MHz 4 Kbytes 25 60 ms te16K ____ 240 $N_{PEC} \le 100$ 16 Kbytes 100 ms t_{E4K} ____ 30 72 PCLK = 50 MHz 4 Kbytes ms t_{F16K} $N_{PEC} > 100$ 16 Kbytes 120 288 ms Suspend delay time during writing 120 Figure 33.24 tspd _ us First suspend delay time during erasing PCLK = 50 MHz 120 tsesd1 _ μs (in suspend priority mode) Second suspend delay time during erasing _ 1.7 tSESD2 ms (in suspend priority mode) Suspend delay time during erasing tseed 1.7 ms ____ (in erasure priority mode)



RX62T Group Data Flash (Flash Memory for Data Storage) Characteristics

Refer to Table 33.20 in RX62T Group User's Manual: Hardware Rev.1.30

Before change

Data Flash (Flash Memory for Data Storage) Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3. Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = -40 to +85°C. Ta is the same under conditions 1 to 3.

ltem		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK =
	128 bytes	t DP128	—	1	5	ms	50 MHz
Erasure time	2 Kbytes	tde2k	-	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	tdbc8	—	_	30	μs	PCLK =
	2 Kbytes	tdbc2k	—	_	0.7	ms	50 MHz
Rewrite/erase cycle*1		NDPEC	30000*2	_	—	Times	
Suspend delay time du	ring writing	t DSPD	—	_	120	μs	Figure 33.24
First suspend delay tim (in suspend priority mod		tDSESD1	-	-	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		tdseed	—	—	1.7	ms	
Data hold time* ³		TDDRP	10	_	—	Year	

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)



Data Flash (Flash Memory for Data Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = -40 to +85°C. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	NDPEC	30000	_	_	Times	
Data hold time	TDDRP	<u>30*2</u>	_		Year	<u>T_a = +85°C</u>

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address

for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

Data Flash (Flash Memory for Data Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3. Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = -40 to $+85^{\circ}$ C. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Programming time	8 bytes	tdps — 0.4 2	2	ms	PCLK = 50 MHz		
	128 bytes	tdp128	—	1	5	ms	
Erasure time	2 Kbytes	tde2k	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	tdbc8	—	_	30	μs	PCLK = 50 MHz
	2 Kbytes	tdbc2k	—	_	0.7	ms	
Suspend delay time du	ring writing	t dspd	—	_	120	μs	Figure 33.24
First suspend delay tim (in suspend priority mod		tDSESD1	—	—	120	μs	PCLK = 50 MHz
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	—	-	1.7	ms	
Suspend delay time du (in erasure priority mod		tdseed	-	—	1.7	ms	



RX630 Group, RX63N Group, RX631 Group ROM (Flash Memory for Code Storage) Characteristics

Refer to Table 45.29 in RX630 Group User's Manual: Hardware Rev.1.50 and Table 50.34 in RX63N Group, RX631 Group User's Manual: Hardware Rev.1.50

Before change

ROM (Flash Memory for Code Storage) Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = Topr

Item		Currents al	F	-CLK = 4 N	IHz	20 MH	1.1		
		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Programming time	128 bytes	t P128	—	2.8	28	_	1	10	ms
$N_{PEC} \le 100 \text{ hours}$	4 Kbytes	tР4К	_	63	140	_	23	50	ms
	16 Kbytes	t Р16К	—	252	560	—	90	200	ms
Programming time N _{PEC} > 100 hours	128 bytes	t P128	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t Р4К	—	75.6	168	_	27.6	60	ms
	16 Kbytes	t Р16К	—	302.4	672	—	108	240	ms
Erasure time $N_{PEC} \le 100$ hours	4 Kbytes	t _{E4K}	—	50	120	_	25	60	ms
	16 Kbytes	te16K	—	200	480	—	100	240	ms
Erasure time	4 Kbytes	t _{E4K}	—	60	144	_	30	72	ms
N _{PEC} > 100 hours	16 Kbytes	t∈16K	—	240	576	_	120	288	ms
Reprogram/erase cycle	e ^{*1}	NPEC	1000*2	—	_	1000*2	_	—	Times
Suspend delay time du	ring programming	tspd	—	_	400	_	_	120	μs
First suspend delay time during erasing (in suspend priority mode)		tsesd1	-	—	300	-	—	120	μs
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	—	_	1.7	-	-	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		tseed	—	—	1.7	-	-	1.7	ms
Data hold time ³		TDRP	10	—	—	10	_	—	Year
FCU reset time		t _{FCUR}	35	_	_	35	_	_	μs

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after reprogramming. (The guaranteed value is in the range from one to the minimum number.)



ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: $T_a = Topr$

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	NPEC	1000	_	_	Times	
Data hold time	Tdrp	<u>30*2</u>	_	_	Year	<u>Ta = +85°C</u>

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: $T_a = Topr$

Item		Currents al		FCLK = 4 N	1Hz	20 MI	Hz ≤ FCLK ≤	50 MHz	Unit
		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	
Programming time $N_{PEC} \le 100$ hours	128 bytes	t P128	—	2.8	28	—	1	10	ms
	4 Kbytes	t Р4К	—	63	140	—	23	50	ms
	16 Kbytes	t ₽16K	—	252	560	—	90	200	ms
Programming time N _{PEC} > 100 hours	128 bytes	t P128	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t₽4ĸ	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t Р16К	—	302.4	672	—	108	240	ms
Erasure time N _{PEC} ≤ 100 hours	4 Kbytes	te₄ĸ	—	50	120	—	25	60	ms
	16 Kbytes	t∈16K	—	200	480	—	100	240	ms
Erasure time	4 Kbytes	t _{E4K}	—	60	144	—	30	72	ms
N _{PEC} > 100 hours	16 Kbytes	te16K	—	240	576	—	120	288	ms
Suspend delay time du	iring programming	t SPD	—	_	400	—	_	120	μs
First suspend delay time during erasing (in suspend priority mode)		tsesd1	—	-	300	—	-	120	μs
Second suspend delay time during erasing (in suspend priority mode)		tsesd2	—	-	1.7	—	-	1.7	ms
Suspend delay time during erasing (in erasure priority mode)		tseed	—	—	1.7	—	-	1.7	ms
FCU reset time		t _{FCUR}	35	_	_	35	—	—	μs



• RX630 Group, RX63N Group, RX631 Group E² Flash Characteristics

Refer to Table 45.30 in RX630 Group User's Manual: Hardware Rev.1.50 and Table 50.35 in RX63N Group, RX631 Group User's Manual: Hardware Rev.1.50

Before change

E2 Flash Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: Ta = Topr

Item		Currente e l	FC	CLK = 4 MH	Ηz	20 MHz	50 MHz	1.1	
		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit
Programming time N _{PEC} ≤ 100 hours	2 bytes	t _{DP2}	—	0.7	6	-	0.25	2	ms
Programming time $N_{PEC} > 100$ hours	2 bytes	tdp2	_	0.7	6	_	0.25	2	ms
Erasure time $N_{PEC} \le 100$ hours	32 bytes	tde32	_	4	40	_	2	20	ms
Erasure time N _{PEC} > 100 hours	32 bytes	tde32	_	7	40	—	4	20	ms
Blank check time	2 bytes	tdbc2	_	—	100	—	—	30	μs
Reprogram/erase cycle ^{*1}		NDPEC	100000 *2	—	—	100000 *2	—	—	Times
Suspend delay time durin	g programming	t DSPD	—	_	250	—	_	120	μs
First suspend delay time during erasing (in suspend priority mode)		tDSESD1	—	_	250	—	_	120	μs
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	_	—	500	—	—	300	μs
Suspend delay time during erasing (in erasure priority mode)		toseed	_	—	500	—	—	300	μs
Data hold time ³		TDDRP	10	—	_	10	—	_	Year

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after reprogramming. (The guaranteed value is in the range from one to the minimum number.)



E2 Flash Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: Ta = Topr

Item	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Reprogram/erase cycle ^{*1}	NDPEC	100000	_	—	Times	
Data hold time	TDDRP	<u>30*2</u>		_	Year	<u>T_a = +85°C</u>

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This value is based on the result of the reliability test.

E2 Flash Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS USB = 0 V

Temperature range for the programming/erasure operation: Ta = Topr

Item		O wash at	FC	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			
		Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	
Programming time <u>N_{DPEC}</u> ≤ 100 hours	2 bytes	t _{DP2}	-	0.7	6	-	0.25	2	ms	
Programming time <u>N_{DPEC}</u> > 100 hours	2 bytes	tdp2	—	0.7	6	—	0.25	2	ms	
Erasure time <u>N_{DPEC}</u> ≤ 100 hours	32 bytes	t _{DE32}	—	4	40	—	2	20	ms	
Erasure time <u>N_{DPEC}</u> > 100 hours	32 bytes	tde32	—	7	40	—	4	20	ms	
Blank check time	2 bytes	tdbc2	—	_	100	—	-	30	μs	
Suspend delay time durin	g programming	t DSPD	—	—	250	—	—	120	μs	
First suspend delay time during erasing (in suspend priority mode)		tDSESD1	—	—	250	—	-	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		tDSESD2	—	—	500	—	_	300	μs	
Suspend delay time durir (in erasure priority mode)	0 0	tdseed	—	_	500	—	—	300	μs	

