I/O INTERFACE STANDARDS

APPLICATION NOTE AN-230

INTRODUCTION:

The vast growth experienced by the communication and semiconductor industry in the past decade was matched with an equal increase in the number interface standards. In the past, there was generally one or maybe two standard interfaces within a system. In today's systems, it is common to see three or more standard interfaces. This trend is driven by several factors: legacy/backwards compatible designs, complexity and size of newer systems, and different requirements for different sections of the system. This application note will provide a summary of the most common interface standards in use today and provide examples of how to correctly implement them.(1)

SINGLE-ENDED INTERFACE STANDARDS

Single-ended interfaces are very common for signaling at less than 300MHz. Their familiarity, ease of design, and ease of use make them highly attractive. Moreover, at lower frequencies, the advantages of a differential interface standard, such as common-mode noise rejection and faster rise/fall time, do not offset the cost of having two pins and two traces per signal.

Single-ended interfaces in use today include:

- **LVTTL and LVCMOS (JESD8-5, JESD8-B)**
- **SSTL (JESD8-8, JESD8-9B, JESD8-15)**
- **HSTL (JESD8-6)**

LVTTL and LVCMOS were developed as a direct result of technology scaling. With each reduction in device geometry, the associated voltage supply has also been reduced in order to maintain the same basic operational characteristics of the transistors. Since the 1980s, this industry has seen a rapid reduction of supply voltage from 1980's 3.5µ 5V technology to today's 0.13µ 1.2V technology. LVTTL and LVCMOS offer manufacturers a migration path as their designs evolve with the technology trend.

LVTTL and LVCMOS buffers are generally simple push-pull designs. One possible implementation is a simple CMOS inverter. The only parameters to meet are V_{IL}/V_{IH}, V_{OL}/V_{OH} and the current drive strengths, which makes this interface standard relatively easy to implement. The input and output specifications are in the following tables. Note that there are several different V_{DD} ranges and different specifications associated with each V_{DD} range. The specifications must be met over the entire range of V_{DD} values for which the parameters apply.

NOTE:
1. Refer to the official specification from the appropriate standards bodies for the complete specification.

INPUT SPECIFICATIONS FOR LVTTL AND LVCMOS

For V_{DD} = 3V to 3.6V

Symbol	Parameter	Min	Max	Unit
V_{IH}	High Level Input Voltage	2	V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3	0.8	V
I_{IN}	Input Current		±5	mA

For V_{DD} = 2.3V to 2.7V

Symbol	Parameter	Min	Max	Unit
V_{IH}	High Level Input Voltage	1.7	V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3	0.7	V
I_{IN}	Input Current		±15	mA

For V_{DD} = 1.8V to 2.7V

Symbol	Parameter	Min	Max	Unit
V_{IH}	High Level Input Voltage	0.7V_{DD}	V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3	0.2V_{DD}	V
I_{IN}	Input Current		±15	mA

OUTPUT SPECIFICATIONS FOR LVTTL AND LVCMOS

LVTTL : V_{DD} = 3V to 3.6V

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{OH}	High Level Output Voltage	I_{OH} = -2mA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OH} = 2mA		0.4	V

LVCMOS : V_{DD} = 3.0V to 3.6V

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{OH}	High Level Output Voltage	I_{OH} = -100µA	V_{DD} – 0.2		V
V_{OL}	Low Level Output Voltage	I_{OH} = 100µA		0.2	V

LVTTL / LVCMOS : V_{DD} = 2.3V to 2.7V

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{OH}	High Level Output Voltage	I_{OH} = -100µA	2.1		V
		I_{OH} = -1mA	2		
		I_{OH} = -2mA	1.7		
V_{OL}	Low Level Output Voltage	I_{OH} = 100µA		0.2	V
		I_{OH} = 1mA		0.4	
		I_{OH} = 2mA		0.7	

LVTTL / LVCMOS : V_{DD} = 1.8V to 2.7V

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{OH}	High Level Output Voltage	I_{OH} = -100µA	V_{DD} – 0.2		V
V_{OL}	Low Level Output Voltage	I_{OH} = 100µA		0.2	V

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Stub Series Terminated Logic (SSTL) comes in three different flavors: SSTL_18, SSTL_2, and SSTL_3. The three flavors were created to address the process technology trends. The SSTL family differs from the LVTTL and LVCMOS family in one very important aspect. SSTL assumes that transmission line termination is required. As such, SSTL has specifications for output impedance and different methods of termination. This difference is important for high-speed signaling because a properly terminated transmission line reduces reflections, reduces EMI emissions, improves settling time, and improves timing margins. LVTTL and LVCMOS signaling can also be terminated. However, because this assumption is not explicit in the specification, the user needs to be careful of the impact the termination resistors have on signal swing.

The design of the SSTL driver is not so much different than that of the LVTTL driver. A very typical implementation is a CMOS inverter. However, the design of the input buffer is vastly different.

The LVTTL input buffer is generally a CMOS inverter. This is an excellent implementation because of its simplicity and near zero-DC power consumption. However, it suffers from poor matching between the NMOS and PMOS transistors over voltage, temperature, and process. Because of this uncertainty in its threshold voltage and its poor voltage gain, this type of buffers requires a higher voltage swing to ensure reliable switching.

The SSTL input buffer is generally a differential pair. The differential pair offers better voltage gain and bandwidth and smaller variations in the threshold voltage. This makes reliable performance possible with small voltage swings. Figure 1 shows a general implementation of a LVTTL I/O versus an SSTL I/O.

The SSTL standard is rather involved and sophisticated. It would be cumbersome to try to replicate the specification in this short application note. The SSTL tables on the following page show the supply and input specifications. Note that SSTL has different output specifications for different classes of drivers. SSTL_3 and SSTL_2 define two classes of drivers that are targeted at different termination schemes. SSTL_18 does not have explicit definitions of classes. However, depending on the termination environment, the driver must be able to produce the appropriate voltage swing at the input buffer. The user is advised to consult the JEDEC publication for a complete discussion of this standard.

The AC parameters refer to the threshold voltage at which the receiver must change state when the signal crosses that voltage. The receiver will maintain the new logic state as long as the voltage stays beyond the DC parameters. The motivation for this distinction is to accommodate ringing in the system and still maintain predictable performance. This problem is common in memory subsystems.

High-Speed Transceiver Logic (HSTL) is yet another standard that was developed to address the process technology trend. HSTL is meant to be voltage scalable and technology independent. Like SSTL, HSTL uses differential amplifiers for the input. Similar to SSTL, HSTL calls out a specification for the output supply voltage and the device supply voltage and allowing those two voltages to be different. (Chronologically, HSTL proceeds SSTL by about a year.) A summary of the supply voltage and input specifications are in the following tables.

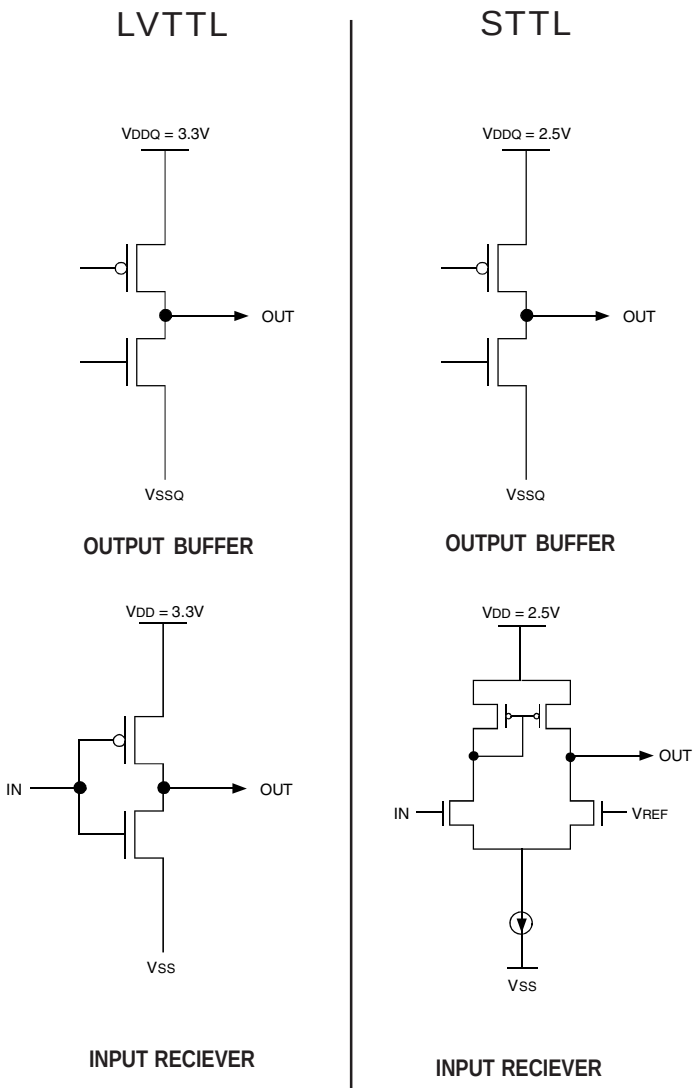

Figure 1 : I/O Implementation Examples

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SSTL SUPPLY VOLTAGE LEVELS

SSTL_3

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Device Supply Voltage	V_{DDQ}		N/A	V
V_{DDQ}	Output Supply Voltage	3	3.3	3.6	V
V_{REF}	Input Reference Voltage	1.3	1.5	1.7	V
V_{TT}	Termination Voltage	V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V

SSTL_2

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Device Supply Voltage	V_{DDQ}		N/A	V
V_{DDQ}	Output Supply Voltage	2.3	2.5	2.7	V
V_{REF}	Input Reference Voltage	1.13	1.25	1.38	V
V_{TT}	Termination Voltage	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V

SSTL_18

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDQ}	Output Supply Voltage	1.7	1.8	1.9	V
V_{REF}	Input Reference Voltage	833	900	969	mV
V_{TT}	Termination Voltage	V_{REF} – 40	V_{REF}	V_{REF} + 40	mV

HSTL SUPPLY VOLTAGE LEVELS

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Device Supply Voltage	N/A		N/A	V
V_{DDQ}	Output Supply Voltage	1.4	1.5	1.6	V
V_{REF}	Input Reference Voltage	0.68	0.75	0.9	V

SSTL INPUT SPECIFICATION

SSTL_3

Symbol	Parameter	Min	Max	Unit
V_{IH}(dc)	DC Input HIGH	V_{REF} + 0.2	V_{DDQ} + 0.3	V
V_{IL}(dc)	DC Input LOW	-0.3	V_{REF} - 0.2	V
V_{IH}(ac)	AC Input HIGH	V_{REF} + 0.4		V
V_{IL}(ac)	AC Input LOW		V_{REF} – 0.4	V

SSTL_2

Symbol	Parameter	Min	Max	Unit
V_{IH}(dc)	DC Input HIGH	V_{REF} + 0.15	V_{DDQ} + 0.3	V
V_{IL}(dc)	DC Input LOW	-0.3	V_{REF} - 0.15	V
V_{IH}(ac)	AC Input HIGH	V_{REF} + 0.31		V
V_{IL}(ac)	AC Input LOW		V_{REF} – 0.31	V

SSTL_18

Symbol	Parameter	Min	Max	Unit
V_{IH}(dc)	DC Input HIGH	V_{REF} + 125	V_{DDQ} + 300	mV
V_{IL}(dc)	DC Input LOW	-300	V_{REF} - 125	mV
V_{IH}(ac)	AC Input HIGH	V_{REF} + 250		mV
V_{IL}(ac)	AC Input LOW		V_{REF} – 250	mV

HSTL SINGLE-ENDED INPUT SPECIFICATION

Symbol	Parameter	Min	Max	Unit
V_{IH}(dc)	DC Input HIGH	V_{REF} + 0.1	V_{DDQ} + 0.3	V
V_{IL}(dc)	DC Input LOW	-0.3	V_{REF} - 0.1	V
V_{IH}(ac)	AC Input HIGH	V_{REF} + 0.2		V
V_{IL}(ac)	AC Input LOW		V_{REF} – 0.2	V

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DIFFERENTIAL SIGNALING INTERFACE STANDARDS

Several of the advantages to differential amplifiers have already been mentioned. The differential amplifier offers better voltage gain and bandwidth and smaller variations in the threshold voltage. This makes reliable performance possible with small voltage swings. The low voltage swing enables higher signaling rates. In addition, differential amplifiers only operate on the difference between the true and complement signals. Any signal that is common to the true and complement signals, such as noise, is rejected; this is called common-mode rejection. Thus, differential signaling offers better noise immunity. This is in contrast to single-ended signals that operate on absolute voltage levels. There are additional system level benefits to differential signaling, such as zero return current and minimal self-induced supply noise.

The two major disadvantages of differential signaling are the increase in pin and trace count and the need to match the true and complement traces on the PCB. It is interesting to note that the increase in pin and trace count is not 2 to 1 versus high-performance single-ended signaling because single-ended signaling requires a signal return for every 2-4 signal lines. The ratio is closer to 1.3 to 1.8.

Differential signaling "standards" in use today include current-mode logic (CML), positive-emitter coupled logic (PECL), low-voltage PECL (LVPECL), and low-voltage differential signaling (LVDS). Of these, only LVDS is a true standard – TIA/EIA-644. CML is a generic term used to refer to signaling that is based on a simple differential amplifier. PECL was developed by Motorola as a modification of their ECL (emitter-coupled logic) products. Efforts to standardize PECL were not fruitful. LVPECL was developed as a direct result of process technology and voltage scaling. It's important to note that because there is no formal standard for these three interfaces, interoperability should not be expected to be automatic. The user must ensure that the relevant parameters of the I/O buffers meet the requirements for interoperability.

CML input and output buffers are based on the differential amplifier (see figure 2). In the case of an output buffer, the goal is to steer the flow of current, I1, through either the R1 or R2. Suppose the voltage at $V_{IN}+$ is higher than the voltage at $V_{IN}-$ such that all the current, I1, is steered to flow through R1. The voltage at $V_{OUT}-$ is then $V_{DD} – (I1 * R1)$. The voltage at $V_{OUT}+$ is V_{DD}, since no current flows through R2. If the voltage at $V_{IN}-$ is higher than the voltage at $V_{IN}+$, then all the current flows through R2, resulting in $V_{OUT}+ = V_{DD} – (I1 * R2)$ and $V_{OUT}- = V_{DD}$.

Generally, R1 is the same value as R2. To match the characteristic impedance of a 50Ω transmission line, R1 and R2 are generally set at 50Ω. The peak-to-peak differential voltage swing is then $|V_{OUT}+ - V_{OUT}-| = I1 * R1$.

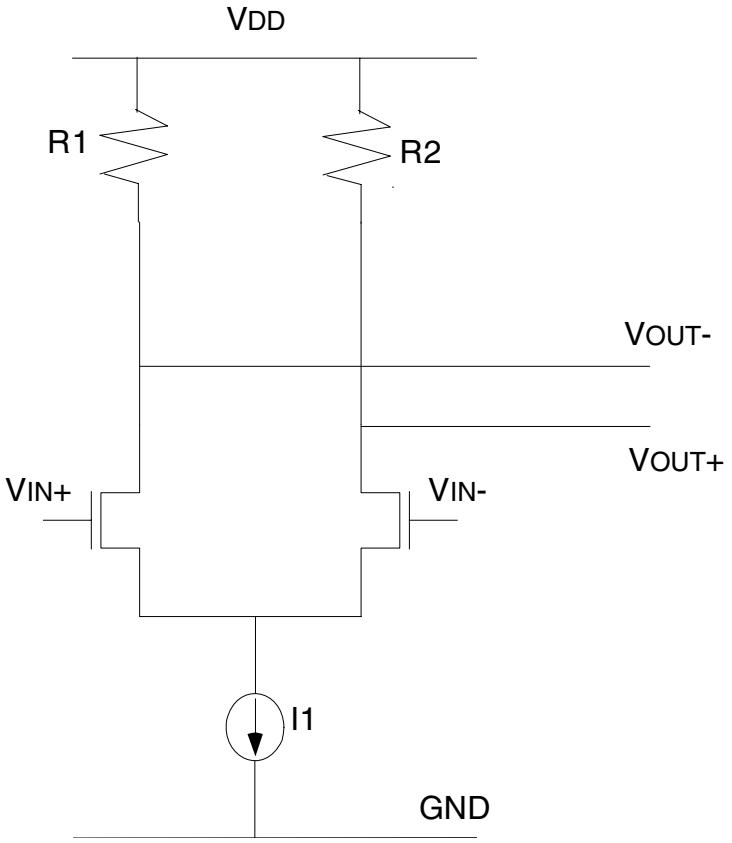

Figure 2 : CML I/O Buffer

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Different vendors will use a different value for I1, and thus the voltage swing may vary from one vendor to another. Though the resistors can also differ between vendors, it's unlikely in high- performance and high-speed devices. Another factor is the common-mode voltage. This is important if DC-coupling is the desired method of connecting to a receiver; DC-coupling reduces component count and cost. In this case, the user must ensure that the common-mode voltage at the output matches the common-mode voltage expected by the receiver. Common-mode voltage is not a problem if AC-coupling is used.

PECL input buffers are generally simple differential amplifiers as is the case with CML input buffers. PECL output buffers are differential amplifiers followed by a common-source amplifier. The output is open-source, as shown in figure 3. The user needs to add external resistors to ground to complete the circuit. Just like CML, the output voltage swing of PECL and LVPECL drivers vary from vendor to vendor. It depends not only on the value of the external resistors, but also on the gate voltages of the common-source amplifiers. And like CML, PECL and LVPECL need the same consideration regarding the common-mode voltage, voltage swing, and interoperability. The difference between CML and PECL (and LVPECL) drivers, namely the addition of the common-source amplifiers in PECL drivers, gives PECL a slight advantage in certain applications. Common-source amplifiers are excellent drivers because they have low output impedance; this allows them to drive heavier loads. The use of the external resistor, which may or may not be advantageous, gives the user a certain amount of control over output swing, power consumption, and termination scheme.

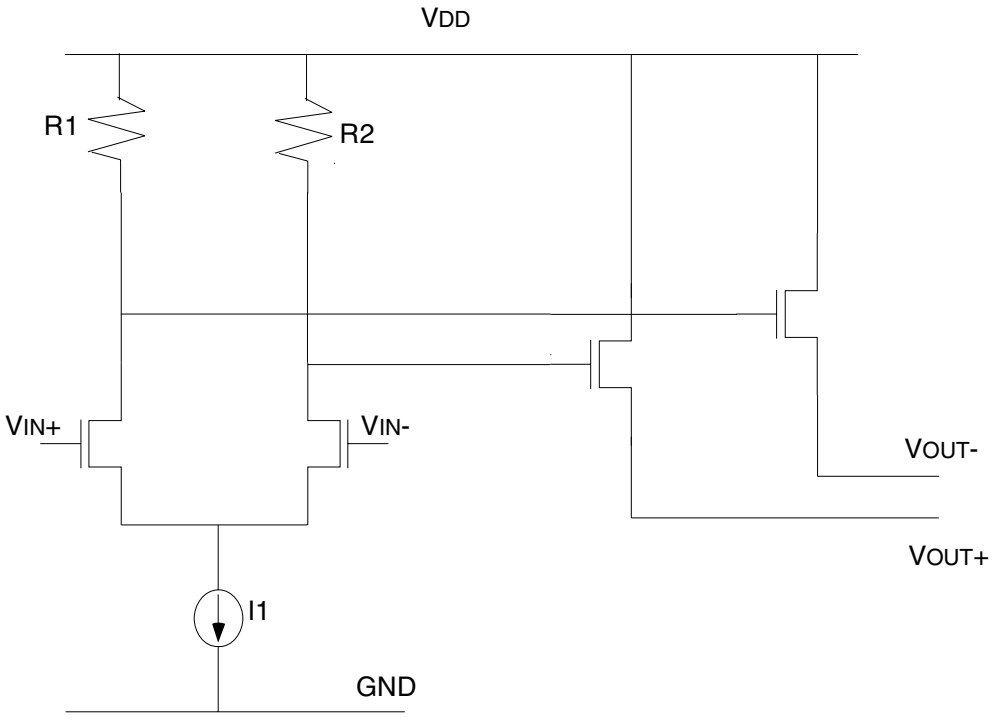

Figure 3 : PECL Output Buffer

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LVDS input buffers are generally simple differential amplifiers. The output buffer is an H-bridge design vastly different than CML or PECL (see figure 4). Current is steered through one of the transistors on the top into the load and back through the transistor on the bottom. The load is generally a 100Ω termination resistor placed across VOUT+ and VOUT-; note that the load is an essential part of this circuit. A voltage is developed across the load and this is sensed by the input buffer.

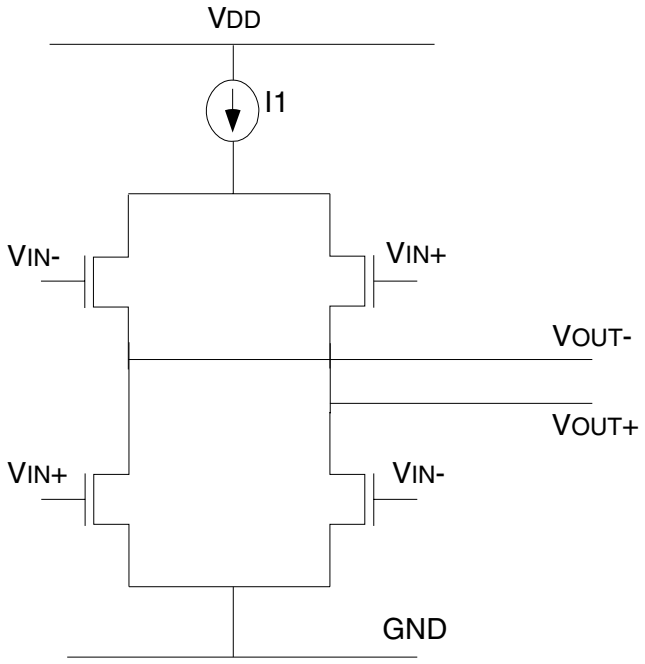

Figure 4 : LVDS Output Buffer

LVDS is an official standard and as such, there are strict specifications on the various parameters that are important for interoperability. The next LVDS table gives a brief summary of the critical parameters. Note that LVDS outputs can be DC-coupled to LVDS inputs because of the tight control over common-mode voltage. The elimination of the external AC-coupling capacitor will become more and more critical as the number of I/Os continue to increase, the pitch of package pins continue to decrease, and PCB real estate becomes even more of a premium.

SUMMARY OF LVDS PARAMETERS

Symbol	Parameter	Min	Max	Unit
V_{OD}	Differential Output Voltage	247	454	mV
V_{OS}	Offset or Common-Mode Voltage	1.125	1.375	V
ΔV_{OD}	|Change of V_{OD}|		50	|mV|
ΔV_{OS}	|Change of V_{OS}|		50	|mV|
V_{TH}	Threshold Voltage		±100	mV
V_{IN}	Input Voltage Range	0	2.4	V

EXAMPLES OF INTERFACING DIFFERENT STANDARDS

With system complexity growing, having two, three, or even four interface standards on a single board is not uncommon. This section will show some examples of how to connect output buffers of one standard to input buffers of another standard.

A common question is interoperability between standards from the same family. For example, can a SSTL_2 driver be connected to a SSTL_18 receiver? What about a SSTL_3 driver driving a SSTL_18 receiver? The AC voltage swings are obviously not a problem when moving from the 3.3V or 2.5V SSTL family to the 1.8V family, assuming the V_{REF} and V_{TT} levels are adjusted accordingly. The potential problem is with the DC voltage, in particular, the maximum V_{IH}.

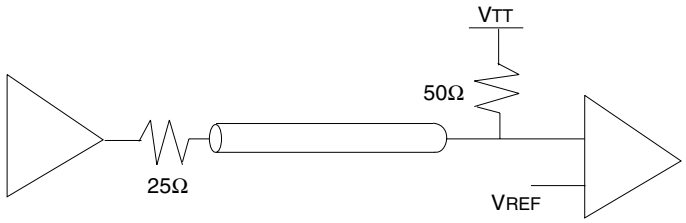

Figure 5 : Typical SSTL Class I Environment

Figure 5 shows a typical SSTL Class I environment. The maximum V_{IH} for all three families is V_{DDQ} + 300mV. For SSTL_18, the worst case value is V_{DDQ}(min) + 300mV = 2V. SSTL receivers are high-impedance, so all of the current will go to and come from V_{TT}. For SSTL_18, the V_{TT}(max) = 969mV + 40mV = 1.009V. If there is 1V across the 50Ω resistor, then the V_{IH} specification will be violated. This would require the driver to source 20mA, which is a definite possibility. Typical SSTL drivers will deliver 8-10mA, which would suggest that SSTL_2 and SSTL_3 drivers can drive SSTL_18 receivers.

What if the driver is able to source and sink more than 20mA? In this case, the termination scheme must be changed (see figure 6). The values of R1 and R2 must be found such that V_{IN} never exceeds 2V (for SSTL_18). A quick application of Kirchoff's current will yield the correct results. This is for a logic high. In general, the user should always double check the conditions for a logic low and ensure that those are within specification for the given resistor values.

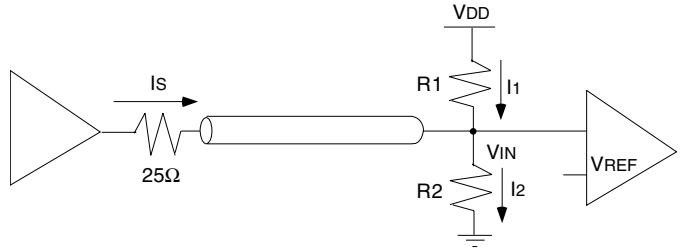

Figure 6 : Alternative Termination for SSTL

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The problem with this method of choosing the resistor values is that the signal might not swing symmetrically around V_{REF}. For example, if I_S = 25mA, V_{DD} = 3.3V, and V_{IN} is limited to a maximum of 2V, then R1 and R2 are 217Ω and 65Ω, respectively. The relevant equations are:

$$\frac{V_{DD} - V_{IN(MAX)}}{R1} + I_S = \frac{V_{IN(MAX)}}{R2}$$

$$R1 \parallel R2 = 50\Omega$$

The signal at V_{IN} would swing from 0V to 2V. Noise margin is sacrificed if V_{REF} is set to 0.9V (for SSTL_18). Moreover, duty-cycle distortion might also be induced because of the offset in V_{REF} from symmetry. The user must make these considerations and make the appropriate calculations based on the exact termination scheme and the capabilities of the driver and receiver in order to ensure bulletproof interoperability.

The above discussion can more generally be applied to interfacing single-ended drivers to receivers that are based on differential amplifiers. One side of the receiver should be tied to some V_{REF} and the other side should be connected to the single-ended driver. Some examples are:

- LVTTL → SSTL/HSTL
- LVTTL → LVPECL/CML
- LVTTL → LVDS
- SSTL/HSTL → LVPECL/CML
- SSTL/HSTL → LVDS

The critical factors to keep in mind are:

1. Set the V_{REF} level to maximize system margins.
2. Double-check that the selected V_{REF} is a valid common-mode level for the receiver.
3. Double-check that the maximum voltage specifications of the receiver are not violated if interfacing between I/Os with different power supply voltages.

Interfacing singled-ended drivers to differential receivers should be done with care. Differential receivers are extremely sensitive. They might take as little as ±100mV or less to distinguish between a logic high and a logic low. The singled-ended signals, ideally, should be strictly monotonic within several hundred milli-volts of the selected V_{REF}. Waveforms such as those in figure 7 would cause unreliable performance whereas they would be no problem for single-ended receivers.

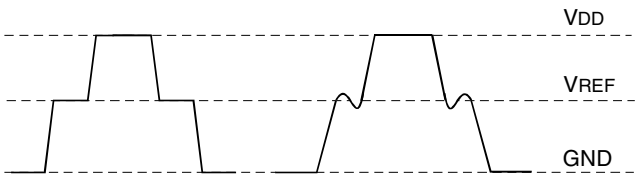

Figure 7 : Waveform Examples

The most common way to interface between the differential signaling standards is AC-coupling. The issue of common-mode voltage is eliminated, but the issue of the maximum voltage remains. The maximum voltage specification is potentially an issue when interfacing between I/Os with different power supply voltages. This is a moot issue if both I/Os use the same power supply voltage; this is also true with singled-ended signaling. AC-coupling also offers the advantage that ground drops will not cause system margins to be lost. Figure 8 shows a typical example. The common-mode voltage can be set at any arbitrary value that's appropriate for the receiver. The resistors can be chosen to correctly terminate the transmission line. If the receiver is internally biased, then it's not necessary to have the resistors R1 and R2. Correct termination is still required and can be provided by R4. In the case of PECL and LVPECL, the DC path to ground is provided by resistors R3.

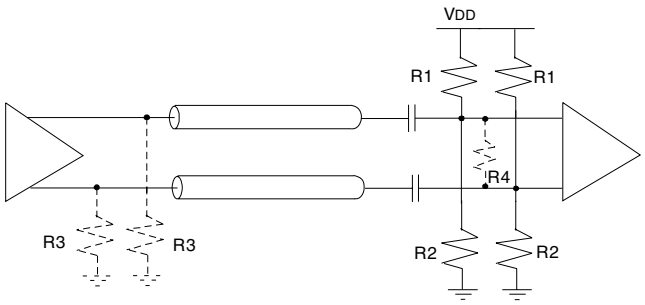

Figure 8 : Example of AC-Coupling

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Just as with single-ended signaling, DC-coupling is also possible with differential signaling. Figure 9 shows one example of connecting an LVPECL driver to an LVDS receiver. R1, R2, and R3 must be chosen to satisfy the following conditions:

1. R1 || (R2 + R3) must match the characteristic impedance of the transmission line.
2. The voltage at V_1 should be $V_{DD} - 2V$. This is generally the termination voltage for LVPECL.
3. The voltage at V_2 should be 1.2V or some other acceptable common-mode voltage for the LVDS receiver.

Incidentally, DC-coupling LVDS to LVPECL is a straight forward procedure (see figure 10). The common-mode voltage of LVDS is 1.2V. LVPECL receivers generally have a relatively wide common-mode range and can accept the 1.2V without problems; the user should nevertheless check the specifications.

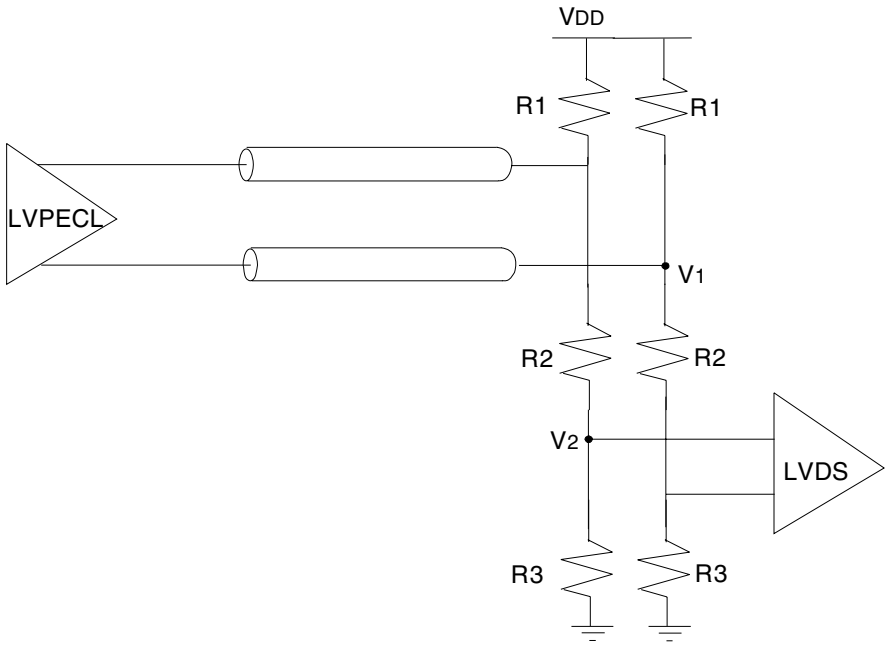

Figure 9 : LVPECL DC-Coupled to LVDS

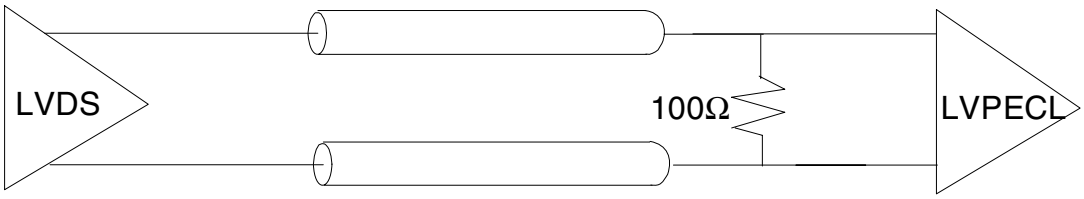

Figure 10 : LVDS DC-Coupled to LVPECL

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ADDENDUM

There are some instances where it's necessary to perform true signal translation rather than merely trying to use external passive components to perform level shifting. Examples include:

- To perform single-ended to differential conversion for better noise immunity and better performance driving long traces such as on the backplane.
- To perform differential to single-ended conversion to drive single-ended receivers.
- To increase voltage swing to drive receivers that require a larger swing. (For example, 1.8V LVTTL cannot drive 2.5V LVTTL without a conversion.)
- To interface to receivers where a solution with external passive components is not feasible or desirable.

In many cases, this signal translation can be performed at the same time as some other useful functions. IDT offers a full portfolio of devices that are capable of signal translation. The following table shows a short list of some of these parts.

Part Number	Description	Input Interface	Output Interface
5T915, 5T905, 5T907	Fanout Buffer	2.5V/1.8V LVTTL, 1.5V/1.8V HSTL, 2.5V PECL	1.8V/2.5V LVTTL, 1.8V/1.5V HSTL
5T93xx	Fanout Buffer	1.8V/1.5V HSTL, 2.5V/3.3V LVPECL, CML, LVDS	LVDS
85304	Fanout Buffer	LVPECL, LVDS, LVTTL, LVHSTL, SSTL, HCSL, CML	LVPECL
5T2110, 5T2010	Zero-Delay Buffer	Differential 1.8V/1.5V HSTL, 1.8/2.5 LVTTL, LVPECL or single-ended 1.8V/2.5V LVTTL	1.8V/1.5V HSTL, 1.8V/2.5V LVTTL
5T94x	Precision Generator	1.8V/1.5V HSTL, SSTL, LVTTL, LVPECL, LVDS	LVPEC, LVDS
5T9010	Programmable Skew	Differential 1.8V/1.5V HSTL, 1.8/2.5 LVTTL, LVPECL or single-ended 1.8V/2.5V LVTTL	1.8V/1.5V HSTL, 1.8V/2.5V LVTTL

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