

TW2984

FN8583

Rev.0.00

**4-CH WD1 (960H)/D1 Compatible Video Decoders
and Audio Codecs**

September 24, 2013

Features
Video Decoder

- WD1 (960H) and D1 compatible video decoding operation and it is programmable each channel
- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60) support with automatic format detection
- Built-in analog anti-alias filter
- Four 10-bit ADCs and analog clamping circuit for CVBS input
- Fully programmable static gain or automatic gain control for the Y channel
- Programmable white peak control for CVBS channel
- 4-H adaptive comb filter Y/C separation
- PAL delay line for color phase error correction
- Image enhancement with peaking and CTI
- Digital sub-carrier PLL for accurate color decoding
- Digital Horizontal PLL for synchronization processing and pixel sampling
- Advanced synchronization processing and sync detection for handling non-standard and weak signal
- Programmable hue, brightness, saturation, contrast, sharpness
- Automatic color control and color killer
- ITU-R 656 like YCbCr (4:2:2) output or time multiplexed output with 36/72/144MHz for WD1 or 27/54/108MHz for D1 format

Audio Codec

- Integrated five audio ADCs processing and one audio DAC
- Provides multi-channel audio mixed analog output
- Support I2S/DSP Master/Slave interface for record output and playback input
- PCM 8/16-bit and u-Law/A-Law 8-bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz

Miscellaneous

- Two-wire MPU serial bus interface
- Integrated clock PLL for 144/108MHz clock output
- Power save and Power down mode
- Low power consumption
- Single 27MHz crystal for all standards and both WD1 and D1 format
- 3.3V tolerant I/O
- 1.0V/3.3V power supply
- 8mm x 8mm 68-pin QFN package

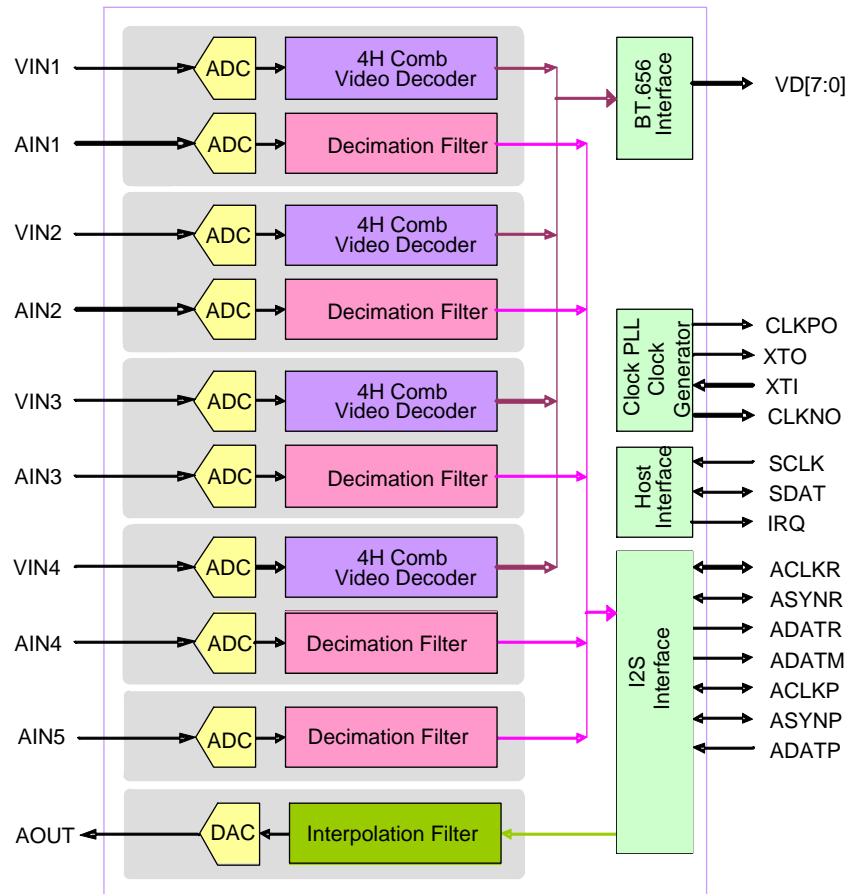


FIGURE 1. TW2984 BLOCK DIAGRAM

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW2984-NA2-CR	TW2984 NA2-CR	68 Lead QFN (8mm x 8mm)	Q68.8x8B

NOTE:

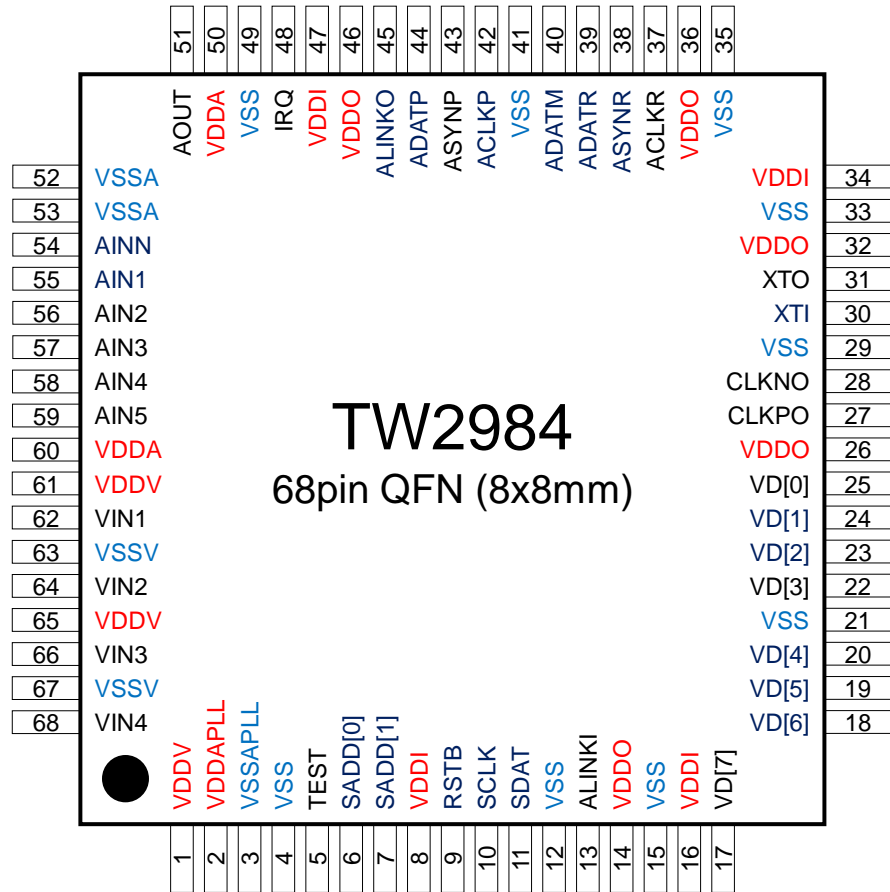
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Pin Diagrams



Pin Descriptions

Analog Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VIN1	62	A	Composite video input channel 1.
VIN2	64	A	Composite video input channel 2.
VIN3	66	A	Composite video input channel 3.
VIN4	68	A	Composite video input channel 4.
AIN1	55	A	Audio input channel 1.
AIN2	56	A	Audio input channel 2.
AIN3	57	A	Audio input channel 3.
AIN4	58	A	Audio input channel 4.
AIN5	59	A	Audio input channel 5.
AINN	54	A	Audio input negative control.
AOUT	51	A	Audio output.

Digital Video/Audio Interface Pins

NAME	NUMBER	TYPE	DESCRIPTION
VD[7:0]	17, 18, 19, 20, 22, 23, 24, 25	O	Video data output.
ACLKR	37	IO	Audio serial clock input/output of record.
ASYNR	38	IO	Audio serial sync input/output of record.
ADATR	39	O	Audio serial data output of record.
ADATM	40	O	Audio serial data output of mixing.
ACLKP	42	IO	Audio serial clock input/output of playback.
ASYNP	43	IO	Audio serial sync input/output of playback.
ADATP	44	I	Audio serial data input of playback.
ALINKI	13	I	Audio Multi-chip operation serial input.
ALINKO	45	O	Audio Multi-chip operation serial output.

System Control Pins

NAME	NUMBER	TYPE	DESCRIPTION
RSTB	9	I	System reset.
XTI	30	I	Crystal 27MHz connection or Oscillator clock input.
XTO	31	O	For crystal 27MHz connection.
CLKPO	27	O	36/72/144MHz or 27/54/108MHz clock output.
CLKNO	28	O	36/72/144MHz or 27/54/108MHz clock output.
TEST	5	I	Test pin. Connect to ground.
SCLK	10	I	Serial control clock line.
SDAT	11	IO	Serial control data line.
SADD[1:0]	7, 6	I	Serial control address.
IRQ	48	O	Interrupt request output.

Power and Ground Pins

NAME	NUMBER	TYPE	DESCRIPTION
VDDI	8, 16, 34, 47	P	1.0V Power for internal logic.
VDDO	14, 26, 32, 36, 46	P	3.3V Power for output driver.
VSS	4, 12, 15, 21, 29, 33, 35, 41, 49	G	Ground for internal logic and output driver.
VDDV	1, 61, 65	P	3.3V Power for analog video ADC.
VSSV	63, 67	G	Ground for analog video ADC.
VDDA	50, 60	P	3.3V Power for analog audio.
VSSA	52, 53	G	Ground for analog audio.
VDDAPLL	2	P	3.3V Power for clock PLL.
VSSAPLL	3	G	Ground for clock PLL.

Parametric Information

ESD Rating

ESD Rating

Human Body Model (Analog video inputs to VSSV/VDDV).....	8000V
Human Body Model (Analog audio inputs to VSSA/VDDA).....	8000V
Human Body Model (Tested per JESD22-A114E, all pins)	7000V
Machine Model (Tested per JESD22-A115-A)	300V
CDM Model (Tested per JESD22-C101)	2000V

AC/DC Electrical Parameters

TABLE 1. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDDV (Measured to VSSV)	VDDVM	-	3.3	3.96	V
VDDA (Measured to VSSA)	VDDAM	-	3.3	3.96	V
VDDAPLL (Measured to VSSAPLL)	VDDAPLLM	-	3.3	3.96	V
VDDI (Measured to VSS)	VDDIM	-	1.0	1.2	V
VDDO (Measured to VSS)	VDDOM	-	3.3	3.96	V
Voltage on any Digital Signal Pin (See the note below)	-	VSS -0.5	-	VDDO + 10%	%
Analog Video Input Voltage	-	VSSV - 0.5	-	VDDV + 10%	V
Analog Audio Input Voltage	-	VSSA - 0.5	-	VDDA + 10%	V
Storage Temperature	T _S	-65	-	+150	°C
Junction Temperature	T _J	-40	-	+125	°C
Reflow Soldering	T _{PEAK}	255 +5/-0 (10-30 seconds)			°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 1 can induce destructive latch-up.

TABLE 2. CHARACTERISTICS

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
SUPPLY					
Power Supply — IO	VDDO	3.0	3.3	3.6	V
Power Supply — Analog Video	VDDV	3.0	3.3	3.6	V
Power Supply — Analog Audio	VDDA	3.0	3.3	3.6	V
Power Supply — Clock PLL	VDDAPLL	3.0	3.3	3.6	V
Power Supply — Digital	VDDI	0.9	1.0	1.1	V

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
VIN1, VIN2, VIN3, VIN4 Input Range (AC Coupling Required)		0.5	1.0	1.4	V
AIN1, AIN2, AIN3, AIN4, AIN5 Input Range (AC Coupling Required)		0.21	1.4	2.4	V
Ambient Operating Temperature	T _A	-40		+85	°C
Analog Video Supply Current	I _{vddv}	-	80	-	mA
Analog Audio Supply Current	I _{vdda}	-	21	-	mA
Clock PLL Supply Current	I _{vddapll}	-	5	-	mA
Digital I/O Supply Current	I _{ddo}	-	28	-	mA
Digital Core Supply Current	I _{ddi}	-	54	-	mA
DIGITAL INPUTS					
Input High Voltage (TTL)	V _{IH}	2.0	-	3.6	V
Input Low Voltage (TTL)	V _{IL}	-0.3	-	0.8	V
Input High Voltage (XTI)	V _{IH}	2.0	-	V _{DDO} + 0.5	V
Input Low Voltage (XTI)	V _{IL}	-	-	0.8	V
Input High Current (V _{IN} = V _{DD})	I _{IH}	-	-	10	μA
Input Low Current (V _{IN} = V _{SS})	I _{IL}	-10	-	-	μA
Input Capacitance (f = 1 MHz, V _{IN} = 2.4V)	C _{IN}	-	5	-	pF
DIGITAL OUTPUTS					
Output High Voltage (I _{OH} = -2mA)	V _{OH}	2.4	-	V _{DDO}	V
Output Low Voltage (I _{OL} = 2mA)	V _{OL}	-	0.2	0.4	V
3-State Current	I _{oz}	-	-	10	μA
Output Capacitance	C _o	-	5	-	pF
ANALOG VIDEO INPUT					
Analog Pin Input Voltage	V _i	-	1	-	V _{pp}
Analog Pin Input Capacitance	C _A	-	7	-	pF
VIDEO ADCS					
ADC Resolution	ADCR	-	10	-	bits
ADC Integral Non-Linearity	AINL	-	±1	-	LSB
ADC Differential Non-Linearity	ADNL	-	±1	-	LSB
ADC Clock Rate	f _{ADC}	-	27	-	MHz
Video Bandwidth (-3db)	BW	-	10	-	MHz

PARAMETER	SYMBOL	MIN (NOTE 3)	TYP	MAX (NOTE 3)	UNITS
HORIZONTAL PLL					
Line Frequency (50Hz)	f _{LN}	-	15.625	-	kHz
Line Frequency (60Hz)	f _{LN}	-	15.734	-	KHz
Static Deviation	Δf _H	-	-	6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f _{sc}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGI)	f _{sc}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f _{sc}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f _{sc}	-	3582056	-	Hz
Lock In Range	Δf _H	±450	-	-	Hz
CRYSTAL SPEC					
Nominal Frequency (Fundamental)		-	27	-	MHz
Deviation (Note 2)		-	-	±50	ppm
Load Capacitance	CL	-	18	-	pF
Series Resistor (ESR)	RS	-	50	-	Ω
OSCILLATOR INPUT					
Nominal Frequency		-	27	-	MHz
Deviation		-	-	±50	ppm
Duty Cycle		-	-	55	%

NOTE:

1. Supply current measurement is based on 0x93[2:0] = 6 setting. These bits should be set to 6 after power-on and resets. Lower settings will increase power consumption.
2. Crystal deviation is based on normal operation condition.
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

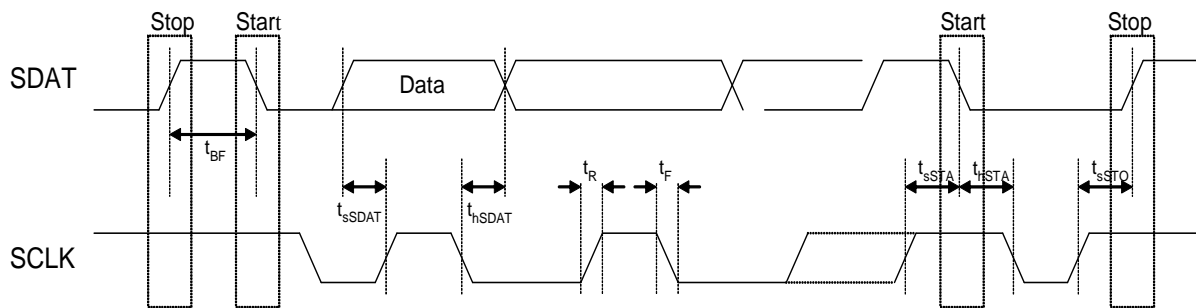
Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (NOTE 1)	TYP	MAX (NOTE 1)	UNITS
Bus Free Time between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	74			ns
SDAT Hold Time	t_{hSDAT}	50		900	ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for each Bus Line	C_{BUS}			400	pF
SCLK Clock Frequency	f_{SCLK}			400	KHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Serial Host Interface Timing Diagram

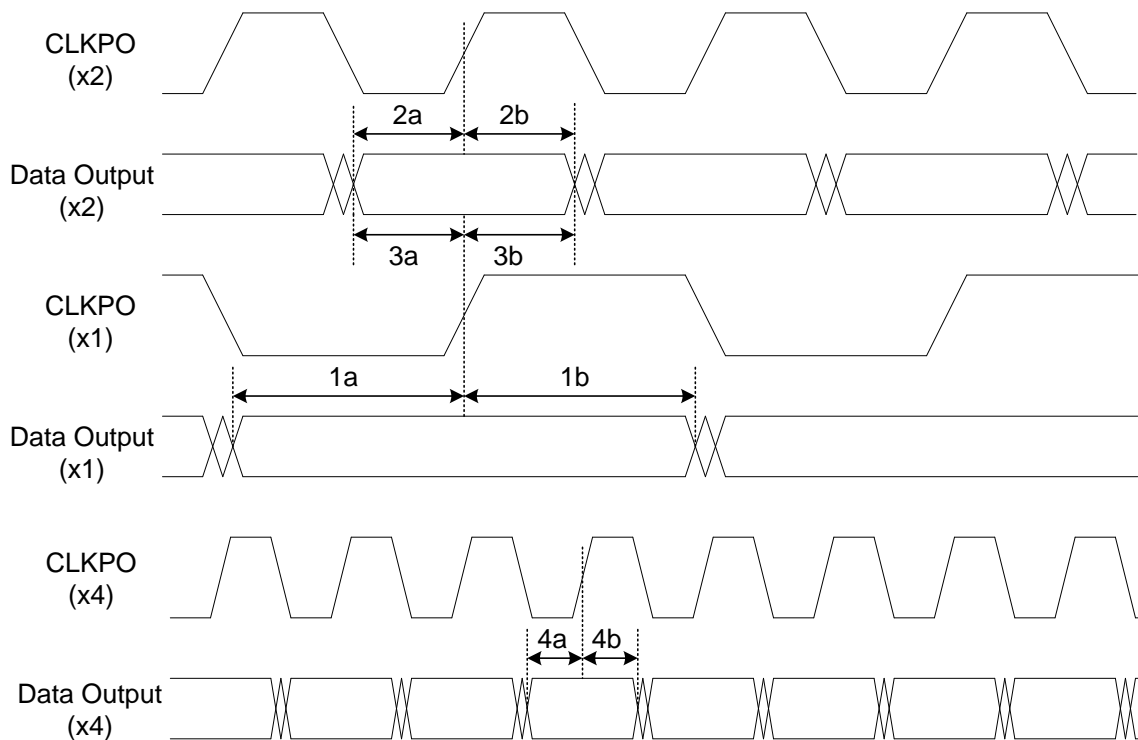


CLKPO and Video Data Timing

PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
Setup from CLKPO(x1) to Video Data(x1)	1a	8		10	ns
Hold from CLKPO(x1) to Video Data(x1)	1b	15		17	ns
Setup from CLKPO(x2) to Video Data(x2)	2a	6		8	ns
Hold from CLKPO(x2) to Video Data(x2)	2b	3		6	ns
Setup from CLKPO(x1) to Video Data(x2)	3a	8		10	ns
Hold from CLKPO(x1) to Video Data(x2)	3b	2		4	ns
Setup from CLKPO(x4) to Video Data(x4)	4a	2		3.5	ns
Hold from CLKPO(x4) to Video Data(x4)	4b	3		4	ns

NOTE:

1. CLKPO timing is related with CLKPO_DEL register value. The following timing diagram is illustrated in the case that the CLKPO_DEL is set to 0hex and CLKPO_POL is set to 0. CLKNO timing is inversed CLKPO timing as default setting. CLKPO_DEL/CLKNO_DEL can make more timings.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

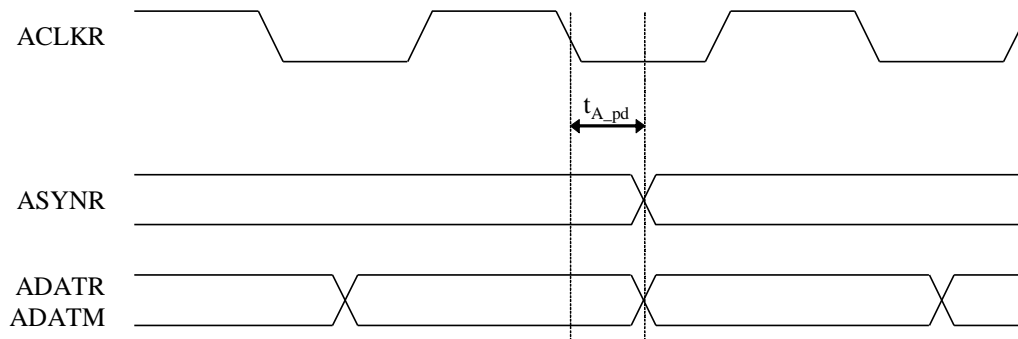


Digital Serial Audio Interface Timing

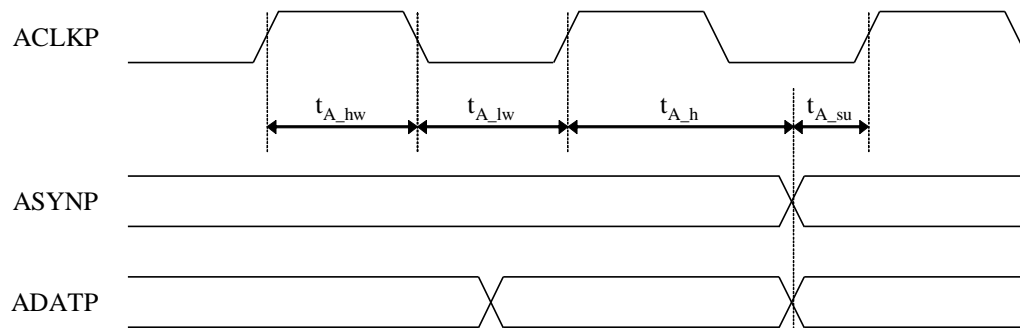
PARAMETER	SYMBOL	MIN (NOTE 2)	TYP	MAX (NOTE 2)	UNITS
ASYNR, ADATR, ADATM Propagation Delay	T_{A_pd}	1.0		4	ns
ACLKP High Pulse Duration	T_{A_hw}	27			ns
ACLKP Low Pulse Duration	T_{A_lw}	54			ns
ASYNP, ADATP Setup Time	T_{A_su}	26			ns
ASYNP, ADATP Hold Time	T_{A_h}	25			ns

NOTE:

1. T_{A_lw} Min value and T_{A_su} Min value are $F_s=48\text{KHz}$ mode only. If $F_s < 48\text{KHz}$, these Min values are more bigger. High period of ACLKR/ACLKP is 36MHz one clock period.
2. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.



(A) RECORD AND MIX AUDIO(MASTER MODE)



(B) PLAYBACK AUDIO(MASTER MODE)

Analog Audio Parameters

PARAMETER	SYMBOL	MIN (NOTE 4)	TYP	MAX (NOTE 4)	UNITS
ANALOG AUDIO INPUT CHARACTERISTICS					
AIN1-5 Input Impedance	RINX	9.5			k Ω
Interchannel gain mismatch			0.2		dB
Input voltage range		0	1.4	2.4	Vpp
Full scale input voltage (peak to peak) (Note 1)	ViFULL	0.21	1.4	2.4	Vpp
Interchannel Isolation (Note 2)			85		dB
ANALOG AUDIO OUTPUT CHARACTERISTICS					
AOUT Output Load Resistance	RLAO	300			ohm
AOUT Load Capacitance	CLAO			1	nF
AOUT Offset Voltage	VOSAO			300	mV
Full Scale Output Voltage (Note 3)	VoFULL		1.0	1.4	Vpp

NOTE:

1. Tested at input gain of 0 dB, Fin = 1kHz.
2. Tested at input gain of 0 dB, Fs=8kHz and 16kHz.
3. Tested at output gain of 0 dB, Fout = 1kHz.
4. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Video Decoder

VIDEO DECODER OVERVIEW

The TW2984 is a low power NTSC/PAL video decoder chip that is designed for video surveillance applications. It consumes very low power in a typical composite input application. The available power down mode further reduces the power consumption. It uses the 1.0V for digital supply voltage and 3.3V for I/O and analog power. A single 27MHz crystal is all that needed to decode all analog video standards.

The video decoder decodes the base-band analog CVBS into digital 8-bit 4:2:2 YCbCr for output. It consists of analog front-end with input source selection, variable gain amplifier and analog-to-digital converters, Y/C separation circuit, multi-standard color decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC 4.43) and synchronization circuitry. The Y/C separation is done with high quality adaptive 4H (5-line) comb filter for reduced cross color and cross luminance. The advanced synchronization processing circuitry can produce stable pictures for non-standard signal as well as weak signal.

Analog Front End

The analog front-end prepares and digitizes the AC coupled analog signal for further processing. Each channel has built-in anti-aliasing filter and 10-bit over-sampling ADCs. The characteristic of the filter is available in the filter curve section. The Y channel has additional 2-input multiplexer, and a variable gain amplifier for automatic gain control (AGC). It can support a maximum input voltage range of 1.4V without attenuation.

Sync Processor

The sync processor of TW2984 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward. It allows the sampling of the video signal in line-locked fashion.

Y/C Separation

For NTSC and PAL standard signals, the luma/chroma separation can be done either by adaptive comb filtering or notch/band-pass filter combination. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter are shown in the filter curve section.

TW2984 employs high quality 4-H (5-line) adaptive comb filter to reduce artifacts like hanging dots and crawling dots. Due to the line buffer used in the comb filter, there is always two lines processing delay in the output images no matter what standard or filter option is chosen.

Color Demodulation

The color demodulation of NTSC and PAL signal is done by first quadrature down mixing and then low-pass filtering. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

AUTOMATIC CHROMA GAIN CONTROL

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC control is -6db to +26db.

COLOR KILLER

For low color amplitude signals, black and white video or very noisy signals, the color will be suppressed or killed. The color killer uses the burst amplitude measurement as well as sub-carrier PLL status to switch-off the color.

AUTOMATIC STANDARD DETECTION

The TW2984 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC or PAL color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM. Each standard can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection. The SECAM standard can be recognized but not properly decoded.

TW2984 supports all common video formats as shown in Table 3. The video decoder needs to be programmed appropriately for each of the composite video input formats.

TABLE 3. VIDEO INPUT FORMATS SUPPORTED BY THE TW2984

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (Note 1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding
NTSC 50	625	50	3.579545 MHz	

NOTE:

1. NTSC-Japan has 0 IRE setup.

Component Processing

The TW2984 supports the brightness, contrast, color saturation and Hue adjustment for changing the video characteristic. The Cb and Cr gain can be adjusted independently for flexibility.

SHARPNESS

The TW2984 also provides a sharpness control function through control registers. It provides the control up to +9db. The center frequency of the enhancement curve is selectable. A coring function is provided to prevent noise enhancement.

COLOR TRANSIENT IMPROVEMENT

A programmable Color Transient Improvement circuit is provided to enhance the color bandwidth. Low level noise enhancement can be suppressed by a programmable coring logic. Overshoot and undershoot are also removed by special circuit to prevent false color generation at the color edge.

VIDEO OUTPUT FORMAT

The TW2984 supports ITU-R BT.656 like format. All video data and timing signal of four channels are synchronous with the pins CLKPO or CLKNO output. Therefore, CLKPO or CLKNO can be connected to four channel interfaces for synchronizing data.

CHANNEL ID

The channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Each ITU-R BT.656 like data stream in 4x output data, 2x output data can have this Sync Code and Blanking Code. Table 4 shows this Channel ID format. Nibble data value **m** shows Video Decoder number to be output in this video stream.

TABLE 4. THE CHANNEL ID FORMAT FOR 4X960H, 2X960H TIME-MULTIPLEXED FORMAT

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE			
Field	Vtime	Htime	F	V	H	First	Second	Third	Fourth
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xFm
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE _m
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD _m
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC _m
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB _m
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA _m
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9 _m
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x8 _m

(a) ITU-R BT.656 Sync Code with Channel ID

VIDEO	H BLANKING CODE WITH CHANNEL ID		
	Y	CB	CR
VIN _n	8'h1 _m	8'h8 _m	8'h8 _m

(b) Horizontal Blanking Code with Channel ID

As default, m = 0 Video1 656 data, m = 1 Video2 656 data, m = 2 Video3 656 data, m = 3 Video4 656 data. n = m+1.CH1NUM, CH2NUM, CH3NUM and CH4NUM registers can change this m value in each video channel output data if necessary.

VIDEO LOSS OUTPUT

When NOVID_656 register is set to 1, bit7 of Fourth byte of SAV/EAV code will be 0 when video signal is lost. This can be an optional set of 656 SAV/EAV code for no-video (video lost) specific application.

ITU-R BT.656 LIKE FORMAT

In ITU-R BT.656 like format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 2. The SAV and EAV sequences are shown in Table 5. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

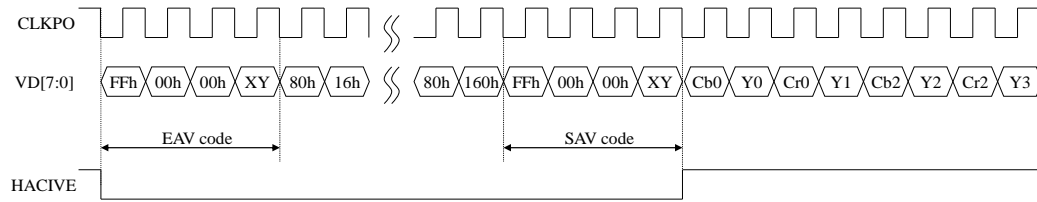


FIGURE 2. TIMING DIAGRAM OF ITU-R BT.656 LIKE FORMAT

TABLE 5. ITU-R BT.656 LIKE SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH	
									NORMAL	OPTION (NOTE NOTE:1)
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE:

- Option includes video loss information in ITU-R BT.656 like format.

TWO CHANNEL ITU-R BT.656 TIME-MULTIPLEXED FORMAT WITH 54/72MHZ

The TW2984 supports two channels ITU-R BT.656 like time-multiplexed format with x2(54MHz/72MHz) that is useful to security application requiring two channel outputs through one channel video port. The CHMD register enables the dual ITU-R BT.656 like time-multiplexed format and the MAINCH/SELCH register selects channel output to be multiplexed with its own channel on each VD pins. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Figure 3 and Figure 4 illustrate VD[7:0]/CLKPO/CLKNO pin timing with x2(54MHz/72MHz),x1(27MHz/36MHz) clock output mode.

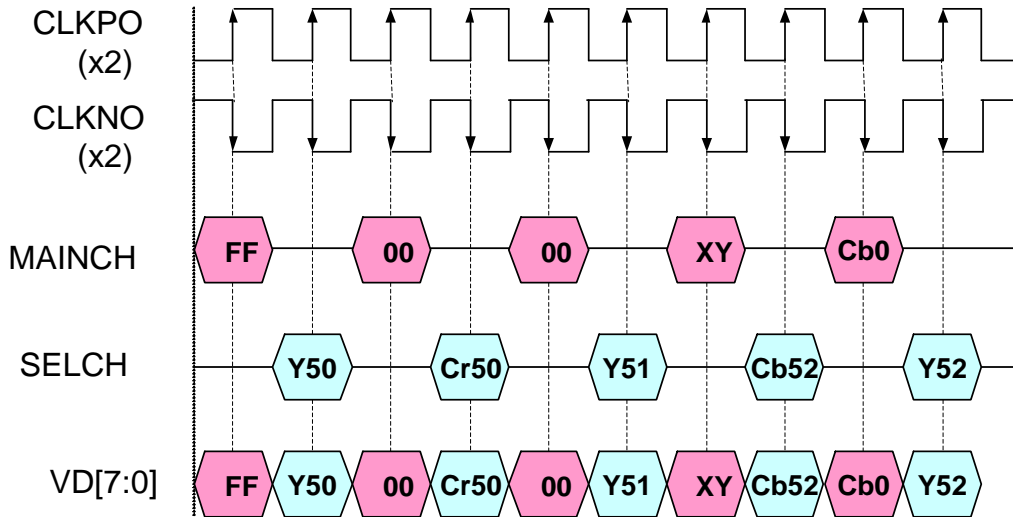


FIGURE 3. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH X2 CLOCK

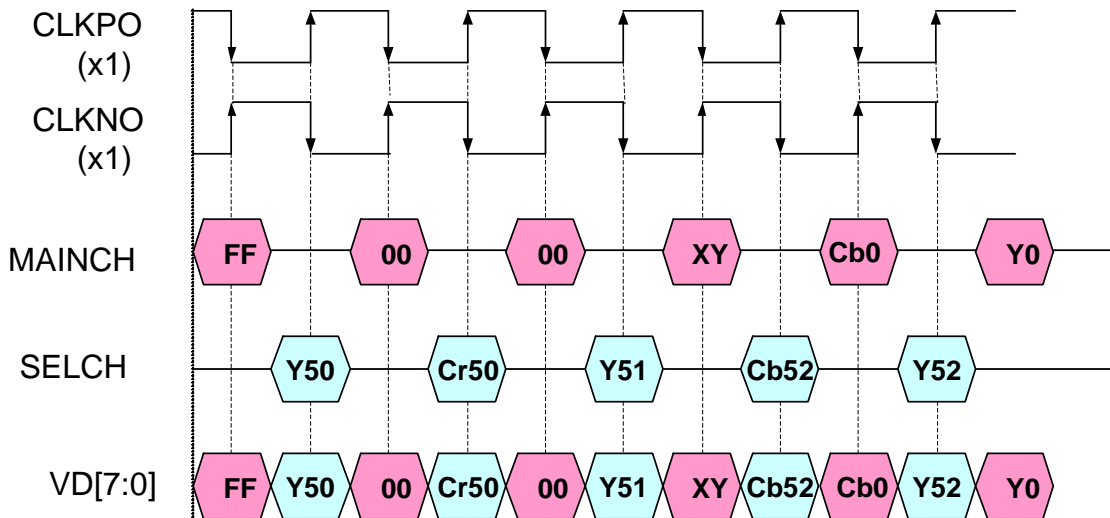


FIGURE 4. PIN OUTPUT TIMING OF TWO CHANNEL TIME-MULTIPLEXED FORMAT WITH X1 CLOCK.

FOUR CHANNEL 960H TIME-DIVISION-MULTIPLEXED FORMAT WITH 108/144MHZ

Four channel of 960H/720H at 36MHz/27MHz video stream that are time-division-multiplexed at x4(144MHz/108MHz) data rate format is implemented in TW2984 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, TW2984 implements single 8-bit bus at 4 times the base band pixel clock rate of x1(36MHz/27MHz). While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band x1(36MHz/27MHz) ITU-R BT.656 like specification. For interface that can accept the new x4(144MHz/108MHz) clock bus, only one single clock at x4(144MHz/108MHz) is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

Figure 5 depicts the temporal arrangement of the video data in x4(144MHz/108MHz) data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is x4(144MHz/108MHz) clock

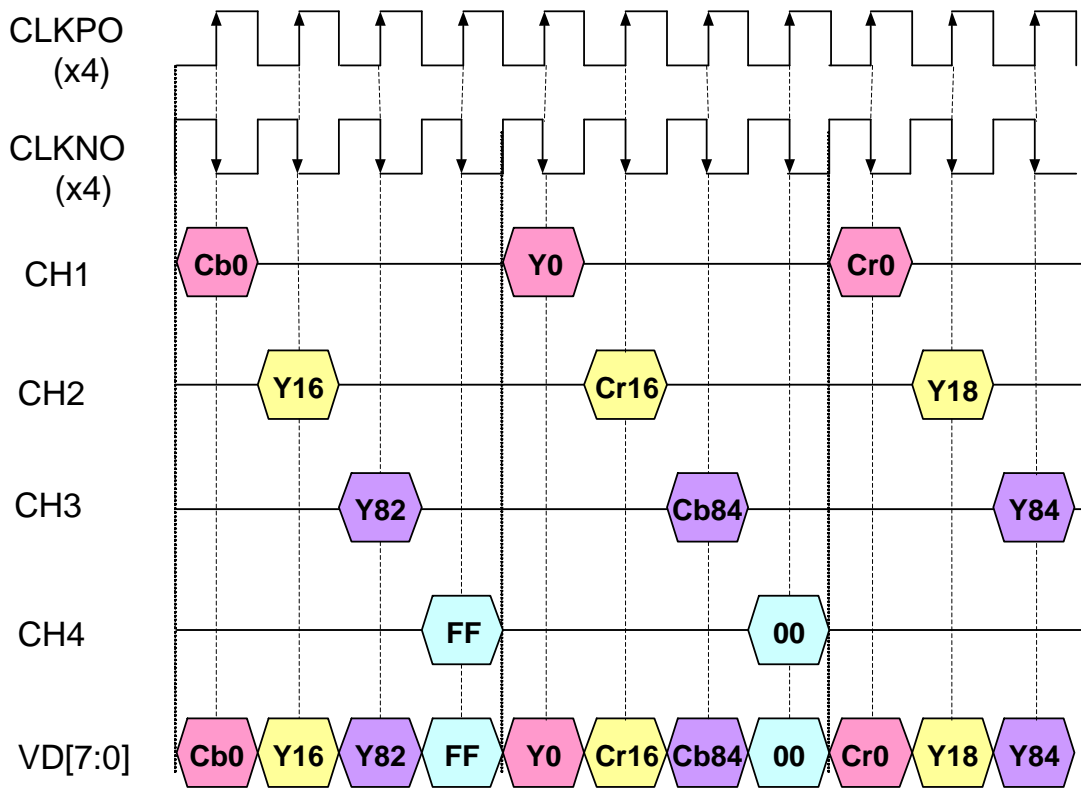


FIGURE 5. PIN OUTPUT TIMING OF 4 CH TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH X4 CLOCK

TABLE 6. SHOWS THE SPECIAL FORMAT OF ITU-R BT. 656 LIKE EMBEDDED TIMING CODE AND CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
Field	V-time	H-time	F	V	H	First	Second	Third	Fourth			
									Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

OUTPUT ENABLING ACT

After power-up, the TW2984 registers have the default values. After RSTB pin is asserted and released, all registers have the default values. After reset, the TW2984 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

VIDEO OUTPUT CHANNEL SELECTION

If CHMD[1:0] in Reg0xCA is set to 0hex, MAINCH[1:0] in Reg0xCD selects one number of Video Channels to be output on VD[7:0] pin as Single Channel ITU-R BT.656 like Format output. If CHMD[1:0] in Reg0xCA is set to 1hex, MAINCH[1:0] in Reg0xCD and SELCH[1:0] in Reg0xCC select two numbers of Video Channels to be output on VD[7:0] pin as Two Channel ITU-R BT.656 like Time-multiplexed Format output. If CHMD[1:0] in Reg0xCA is set to 2hex, Four Channel ITU-R BT.656 like x4 Time-multiplexed Format is output on VD[7:0] pin.

Audio Codec

The audio codec in the TW2984 is composed of five audio Analog-to-Digital converters processing, one Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as the Figure 6. The TW2984 can accept 5 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

The level of analog audio input signal AIN1 ~ AIN5 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1,AIGAIN2,AIGAIN3,AIGAIN4 and AIGAIN5 registers and then sampled by each Analog-to-Digital converters. The digital serial audio input data through the ACLKP, ASYNP and ADATP pins are used for playback function. To record audio data, the TW2984 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pins.

The TW2984 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO5 and MIX_RATIO6 registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the AOGAIN register. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The main purpose of AIN5 is to make the standard I2S/DSP digital audio output on ADATM pin for special application. Usually, 4 AIN1/AIN2/AIN3/AIN4 audio data are only used on ADATR pin output.

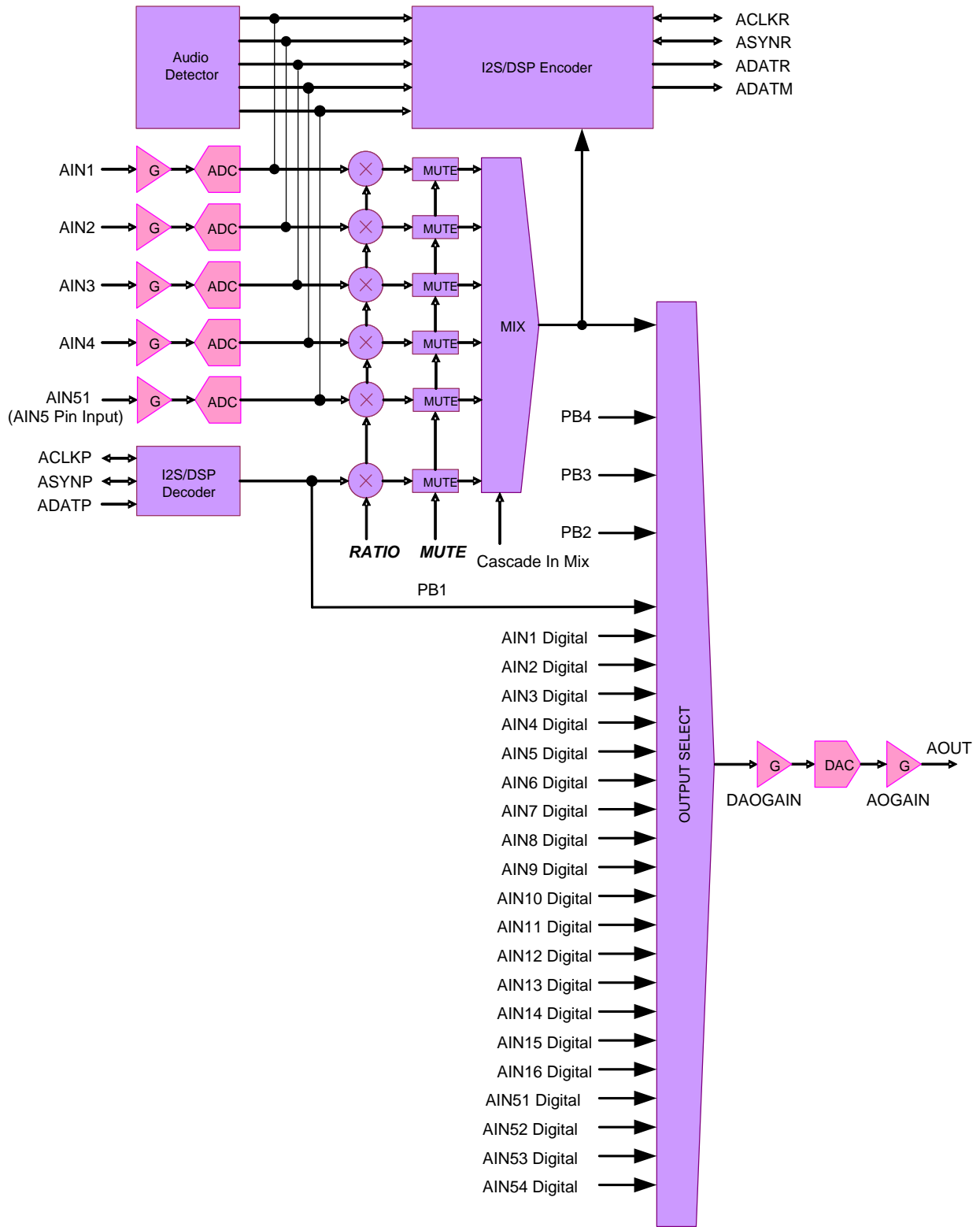


FIGURE 6. BLOCK DIAGRAM OF AUDIO CODEC

AUDIO CLOCK MASTER/SLAVE MODE

The TW2984 has two types of Audio Clock modes. If ACLKRMAS_{TER} register is set to 1, fs audio sample date is processed from audio clock internal ACKG (Audio Clock Generator) generates. In this master mode, ACLKR/ASYNR pins are output mode. ASYNROEN register for ASYNR pin should be set to 0 (output enable mode). If ACLKRMAS_{TER} register is set to 0, fs audio sample rate is processed from audio clock on ACLKR pin input. 256xfs, 320xfs or 384xfs audio clock should be connected to ACLKR pin from external master clock source in this slave mode. ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode. AIN5MD and AFS384 register set up Audio fs mode by following table.

REGISTER		FS MODE
AIN5MD	AFS384	
0	0	256xfs
1	0	320xfs
0	1	384xfs

AUDIO DETECTION

The TW2984 has an audio detector for individual 5 channels. There are 2 kinds of audio detection method defined by the ADET_TH. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1 ~ ADET_TH5 registers. The detection of differential amplitude is recommended for most use. The status for audio detection is read by the STATE_AVDET register and it also makes the interrupt request through the IRQ pin with the combination of the status for video loss detection.

MULTI-CHIP OPERATION

TW2984 can output 16 channel audio data on ACLKR/ASYNR/ADATR output simultaneously. Therefore, up to 4 chips should be connected on most Multi-Chip application cases. SMD register selects Audio cascade serial interface mode. If SMD register is set to 2, ALINKI pin is audio cascade serial input and ALINKO pin is audio cascade serial output mode.

Each stage chip can accept 5 analog audio signals so that four cascaded chips will be 16-channel audio controller as default {AFS384, AIN5MD} = 00. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW2984 can generate 16 channel data simultaneously using multi-channel method. In addition, each stage chip can support 4 channel record outputs that are corresponding with analog audio inputs. This first stage chip can also output 16 channel mixing audio data by the digital serial audio data and analog audio signal. The first stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog converter in the first stage chip.

Several Master/Slave mode configurations are available. Figure 7 is the most recommended and demanded system with Clock Master mode (ACLKRMAS_{TER} = 1). Figure 8 is the most recommended system with Clock Slave Sync Slave mode (ACLKRMAS_{TER}=0, ASYNROEN=1). Other system combinations are also available if application need different type specific system. Figure 7 and Figure 8 show the most typical system.

In the following FIGURES, Mix1-16-51-54/Pb1 means Mix output of AIN1-16, AIN51-54 and Playback1. AIN1-16-51-54/Pb1 means one selected Audio output in AIN1-16-51-54/Pb1.

If one of TW2984s uses {AFS384, AIN5MD} = 01 or {AFS384, AIN5MD} = 10, all other cascaded TW2984 chips must set up same {AFS384 AIN5MD} mode together.

In Multi-Chip Audio operation mode, one same Oscillator clock source need to be connected to all TW2984 XTI pins.

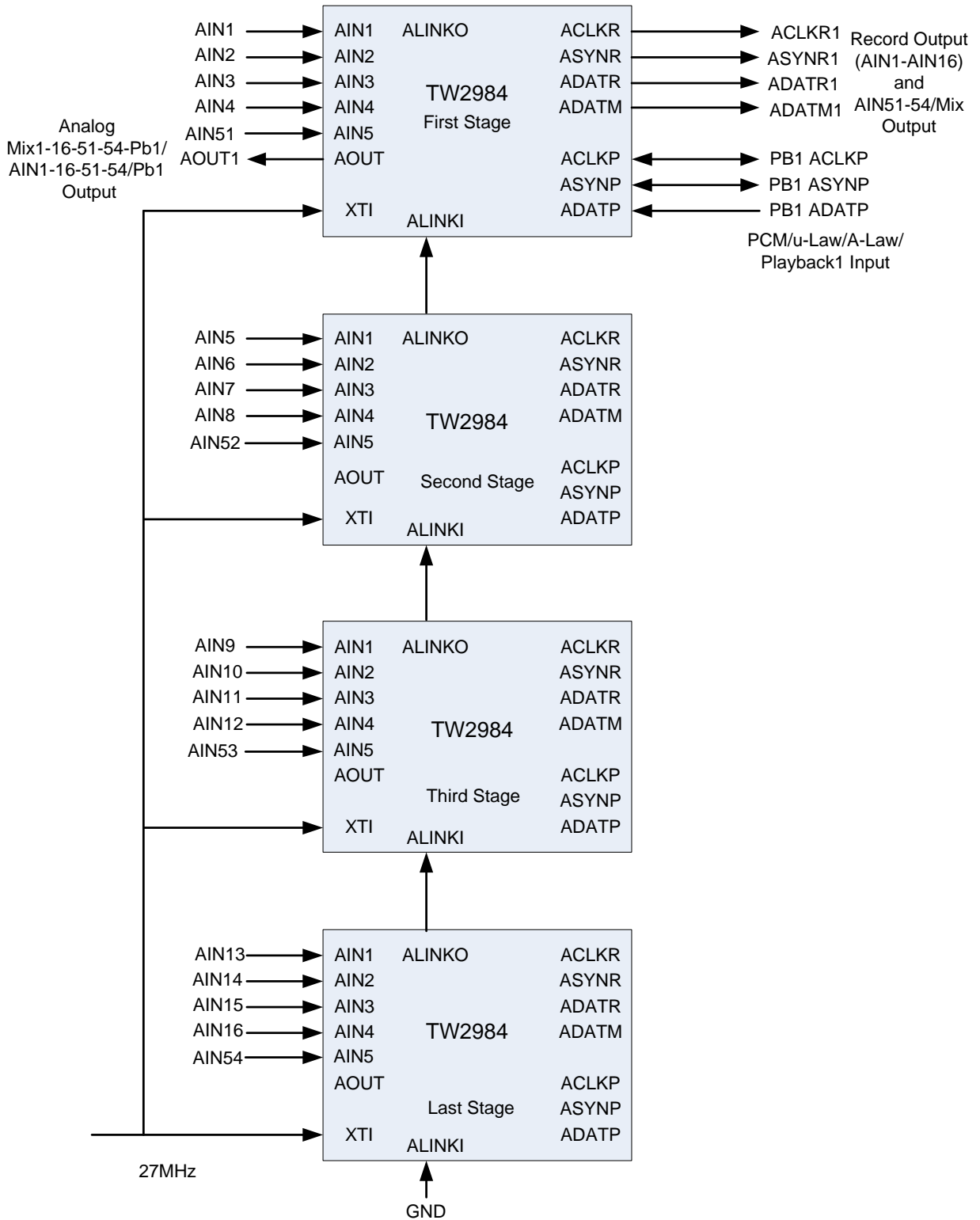


FIGURE 7. RECOMMENDED CLOCK MASTER CASCADE MODE SYSTEM

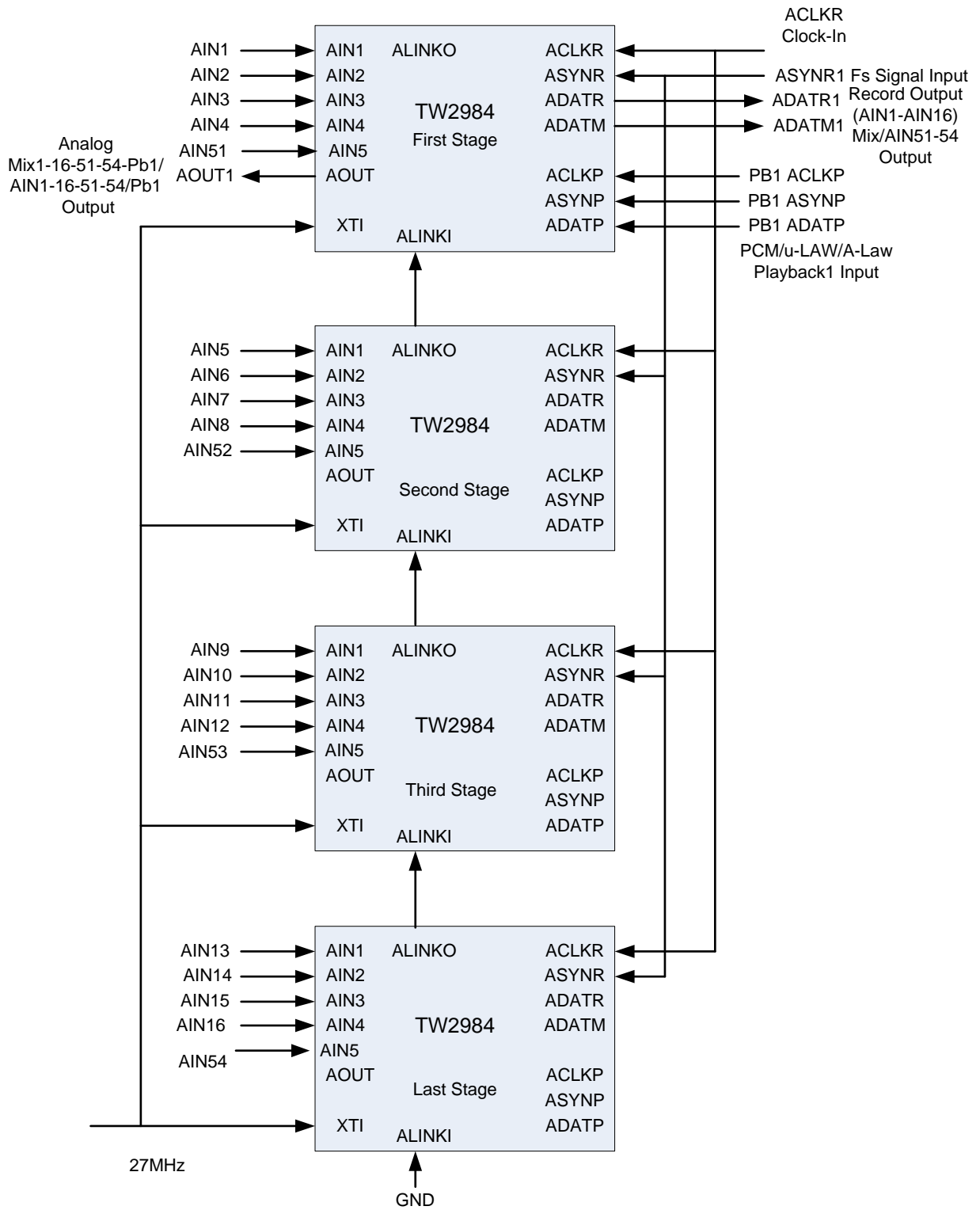


FIGURE 8. RECOMMENDED CLOCK SLAVE SYNC SLAVE CASCADE MODE SYSTEM

SERIAL AUDIO INTERFACE

There are 3 kinds of digital serial audio interfaces in the TW2984; the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in Figure 9.

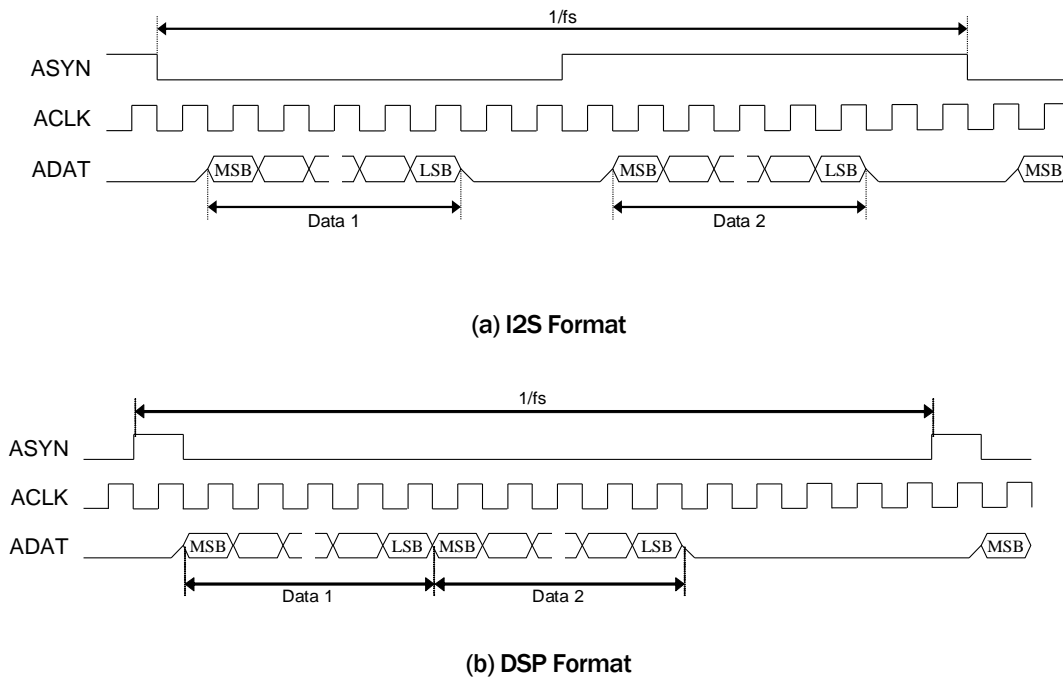


FIGURE 9. FIG13 TIMING CHART OF SERIAL AUDIO INTERFACE

Playback Input

The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW2984 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from 256xfs, 320xfs or 384xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW2984 can provide an extended I2S and DSP format which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256xACLKR clock length with AIN5MD=0. Figure 10 shows the digital serial audio data organization for multi-channel audio.

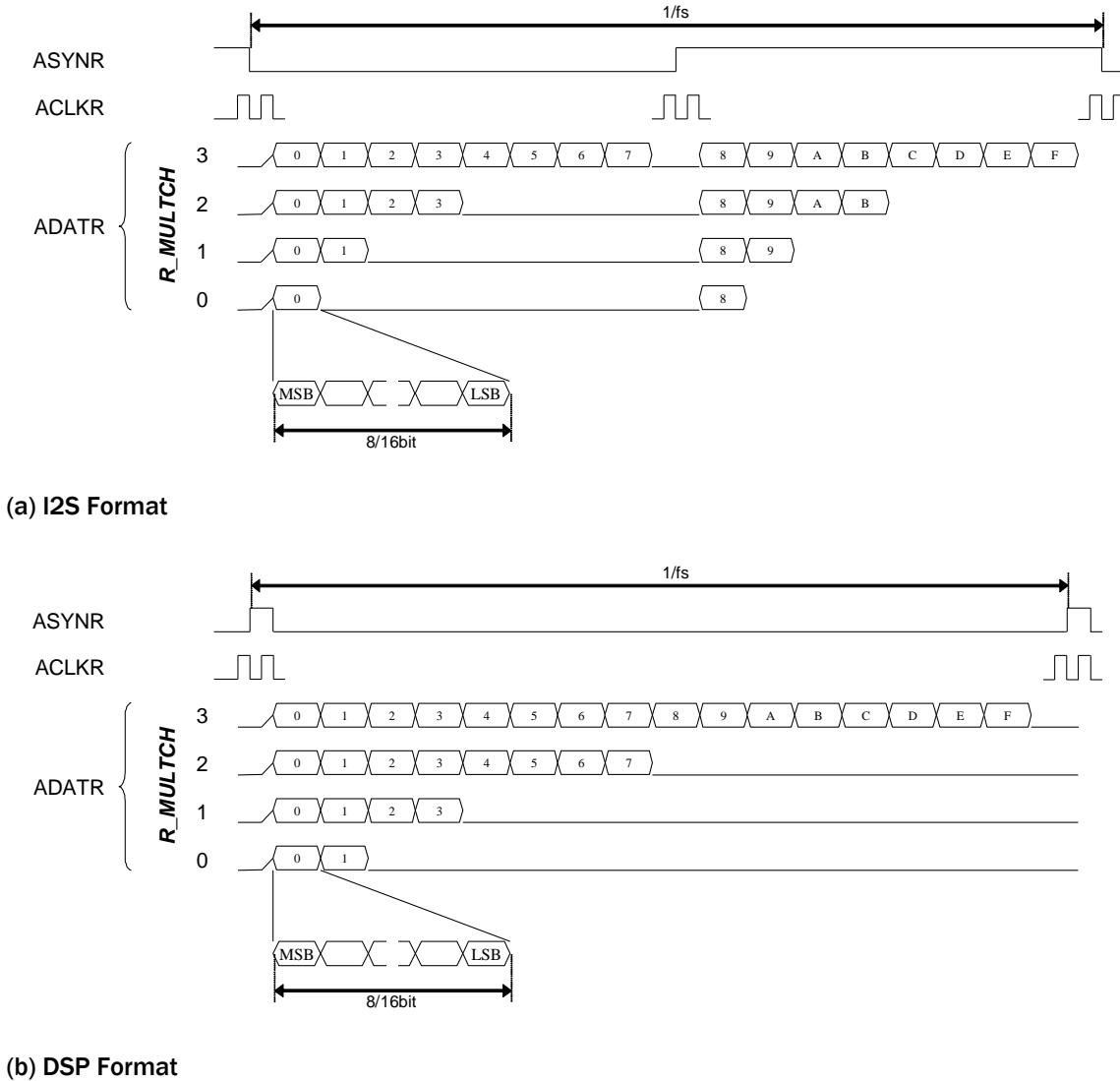


FIGURE 10. TIMING CHART OF MULTI-CHANNEL AUDIO RECORD

Table 7 shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is also shown in Table 7.

TABLE 7. SEQUENCE OF MULTI-CHANNEL AUDIO RECORD

(a) I2S Format

R_MULTCH	PIN	LEFT CHANNEL								RIGHT CHANNEL							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(b) DSP Format

R_MULTCH	PIN	LEFT/RIGHT CHANNEL															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data, which are mixing audio, and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

AUDIO CLOCK SLAVE MODE DATA OUTPUT TIMING

TW2984 always output ASYNR/ADATR/ADATM by ACLKR falling edge triggered timing. ADATR/ADATM output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR/ADATM output are always fixed to one ACLKR falling edge timing. However, if ASYNR is input, ADATR/ADATM output timing changes by ASYNR input timing.

ASYNR is ACLKR falling edge triggered input/output

If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge, or if ASYNR is output, TW2984 output ADATR/ADATM by ACLKR falling edge triggered timing as shown in the following Figures. ASYNR signal is changing during ACLKR = 0. TW2984 output ADATR/ADATM data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

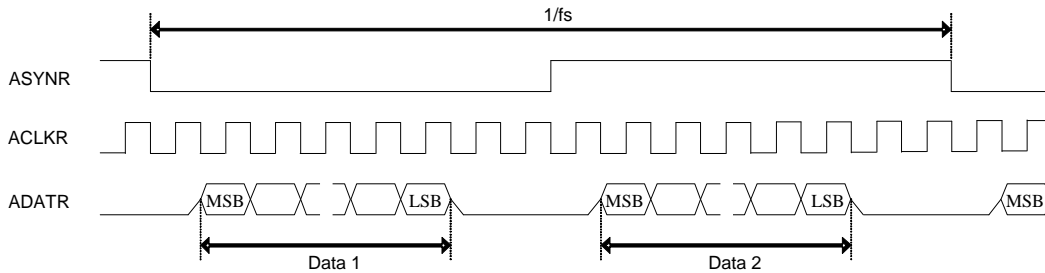


FIGURE 11. ACLKMASTER=0, RM_SYNC=0

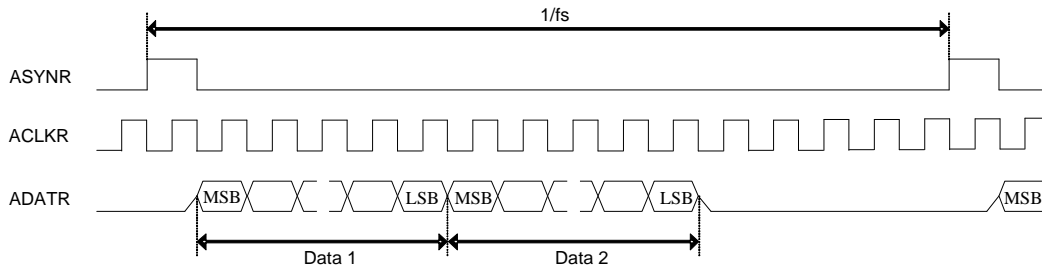


FIGURE 12. ACLKMASTER=0, RM_SYNC=1

ASYNR is ACLKR rising edge triggered input

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge, TW2984 output ADATR/ADATM by ACLKR falling edge triggered timing as shown in the following FIGURES. ASYNR signal is changing during ACLKR = 1. TW2984 output ADATR/ADATM data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

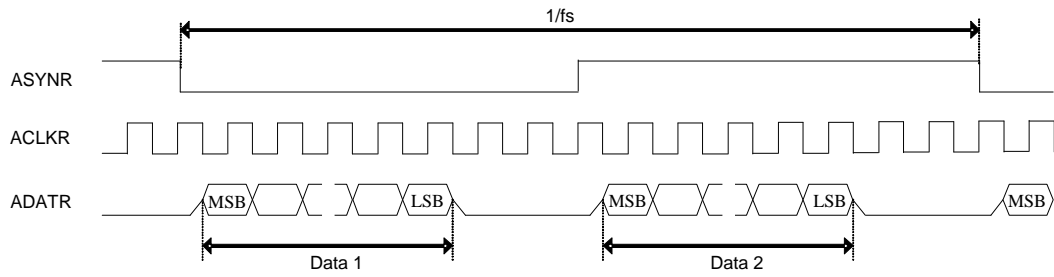


FIGURE 13. ACLKMASTER=0, RM_SYNC=0, ASYNROEN=1

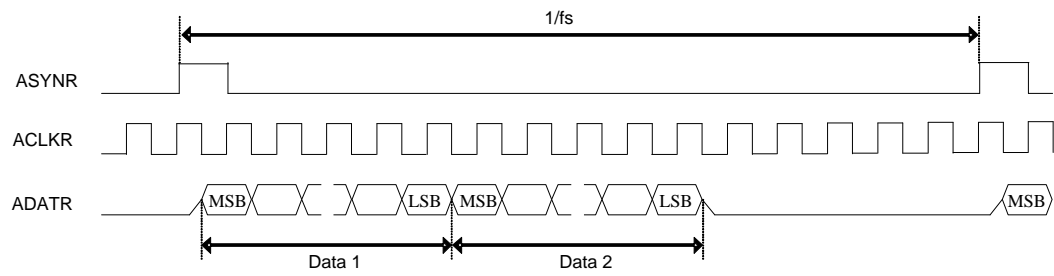


FIGURE 14. ACLKMASTER=0, RM_SYNC=1, ASYNROEN=1

ACLKP/ASYNP SLAVE MODE DATA INPUT TIMING

The following 8 data input timings are supported. ADATPDLY register needs to be set up according to the difference of ADATP data input timings. Data1 is only used as default. The MSB bit is the first input bit as default PBINSWAP = 0. If PBINSWAP = 1, LSB bit is the first input bit.

ASYNP is ACLKP falling edge triggered input.

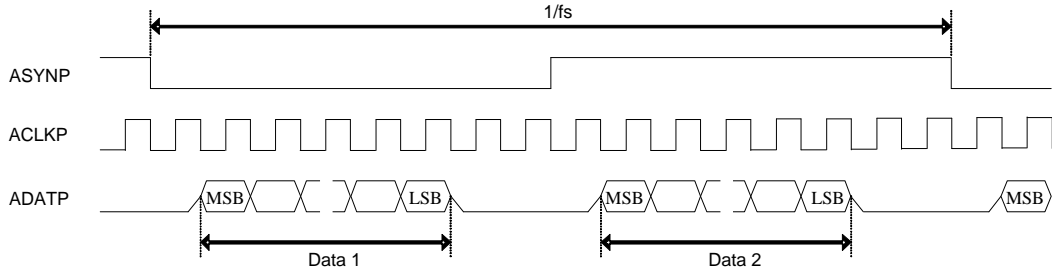


FIGURE 15. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

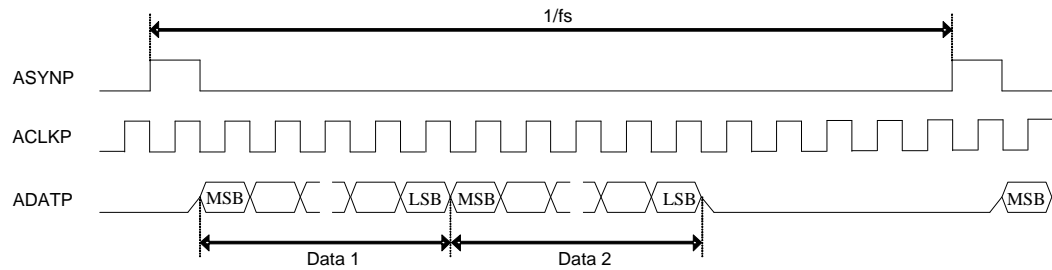


FIGURE 16. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

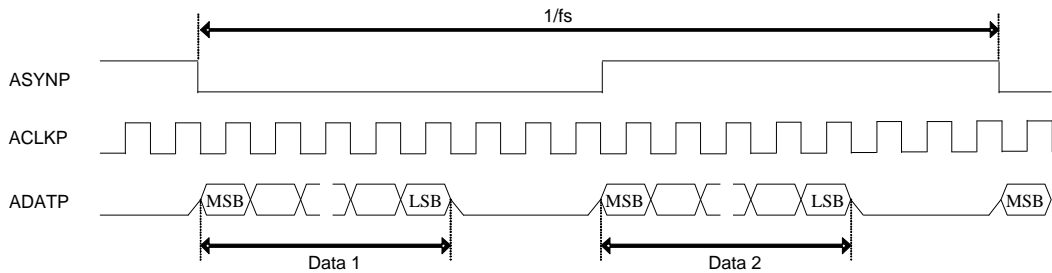


FIGURE 17. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

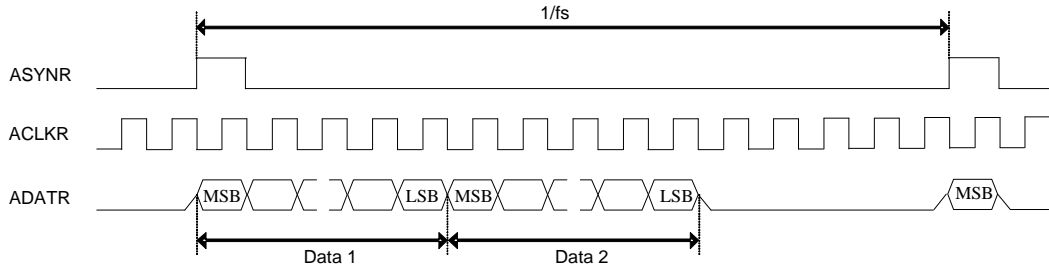


FIGURE 18. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

ASYNP is ACLKP rising edge triggered input.

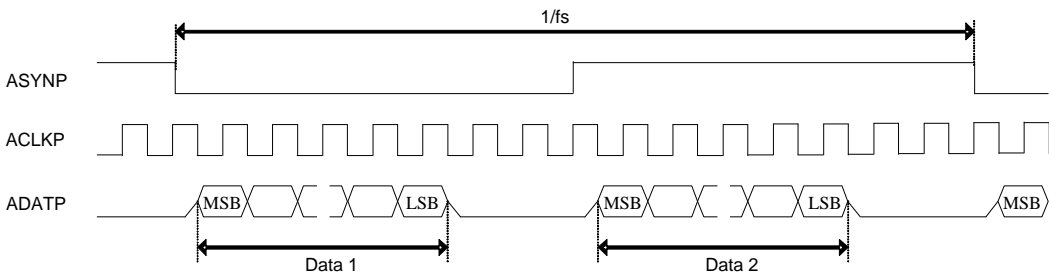


FIGURE 19. RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

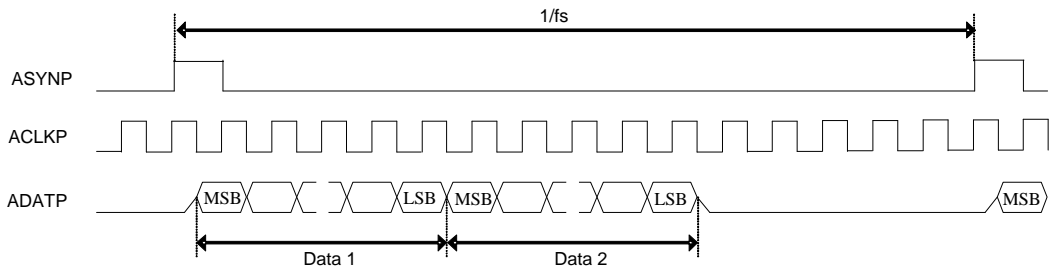


FIGURE 20. RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

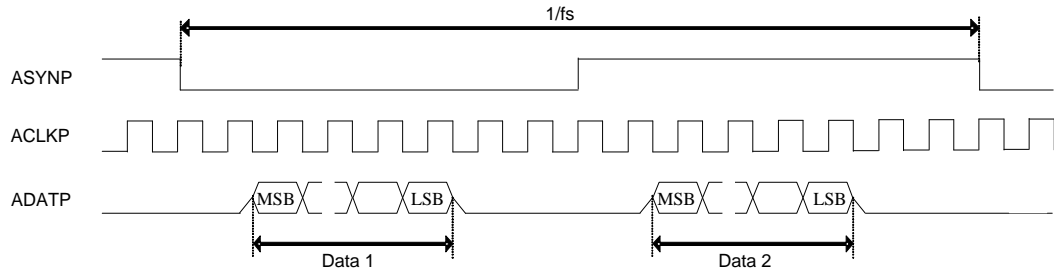


FIGURE 21. RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

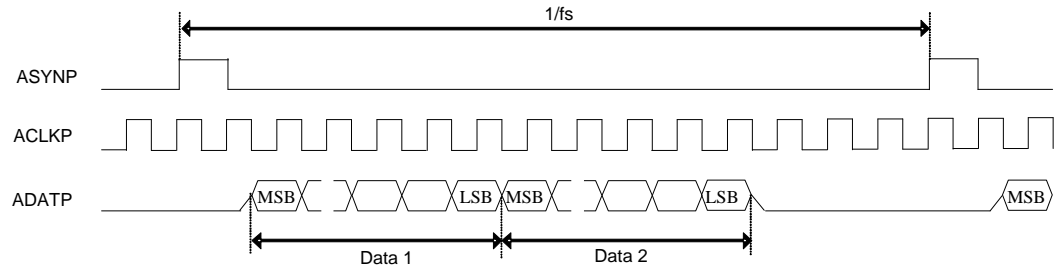


FIGURE 22. RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

AUDIO CLOCK GENERATION

TW2984 has built-in audio clock generator. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKI register based following two equations.

$ACKI = \text{round} (F_{AMCLK} / F_{27MHz} * 2^{23})$, it gives the Audio master Clock Nominal increment.

ACKI registers make audio_source_clock by 27MHz clock.

If MASCKMD=0, AMCLK=audio_source_clock.If MASCKMD=1, AMCLK=audio_source_clock/2.

AMCLK is used as audio system clock and audio ADC clock in Master clock mode.

The following table provides setting example of some common used audio frequency assuming XTI clock frequency of 27MHz.If ACLKRMASMASTER register bit is set to 1, following AMCLK is used as audio system clock with MASCKMD inside TW2984.

ACPL=1(Loop open) should be used in TW2984 system.

256xfs mode: AFS384 = 0, AIN5MD = 0,MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
256 X 16 KHZ		
4.096	2545166	26-D6-0E
256 x 8 KHz		
2.048	1272583	13-6B-07

320xfs mode: AFS384 = 0, AIN5MD = 1, MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
320 x 16 KHz		
5.12	3181457	30-8B-91
320 x 8 KHz		
2.56	1590729	18-45-C9

384xfs mode: AFS384 = 1, AIN5MD=0, MASCKMD = 1.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
384 x 16 KHz		
6.144	3817749	3A-41-15
384 x 8 KHz		
3.072	1908874	1D-20-8A

256xfs mode: AFS384=0, AIN5MD=0, MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
256 x 48 KHz		
12.288	3817749	3A-41-15
256 x 44.1KHz		
11.2896	3507556	35-85-65
256 x 32 KHz		
8.192	2545166	26-D6-0E
256 x 16 KHz		
4.096	1272583	13-6B-07
256 x 8 KHz		
2.048	636291	9-B5-83

320xfs mode: AFS384=0,AIN5MD=1,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
320 x 32 KHz		
10.24	3181457	30-8B-91
320 x 16 KHz		
5.12	1590729	18-45-C9
320 x 8 KHz		
2.56	795364	C-22-E4

384xfs mode: AFS384=1,AIN5MD=0,MASCKMD=0.

AMCLK(MHZ)	ACKI [DEC]	ACKI [HEX]
384 x 32kHz		
12.288	3817749	3A-41-15
384 x 16kHz		
6.144	1908874	1D-20-8A
384 x 8kHz		
3.072	954437	E-90-45

AUDIO CLOCK AUTO SETUP

If ACLKRMAS_{TER} = 1 audio clock master mode is selected, and AFAUTO register is set to "1", TW2984 set up ACKI register by AFMD register value automatically. ACKI control input in ACKG module block is automatically set up to the required value by the condition of AFS384 and AIN5MD register value.

AFAUTO	AFMD	ACKG MODULE ACKI CONTROL INPUT VALUE
1	0	8kHz mode value by each AFS384/AIN5MD case.
1	1	16kHz mode value by each AFS384/AIN5MD case.
1	2	32kHz mode value by each AFS384/AIN5MD case.
1	3	44.1kHz mode value by each AFS384/AIN5MD case.
1	4	48kHz mode value by each AFS384/AIN5MD case.
0	X	ACKI register set up ACKI control input value.

Two-wire Serial Bus Interface

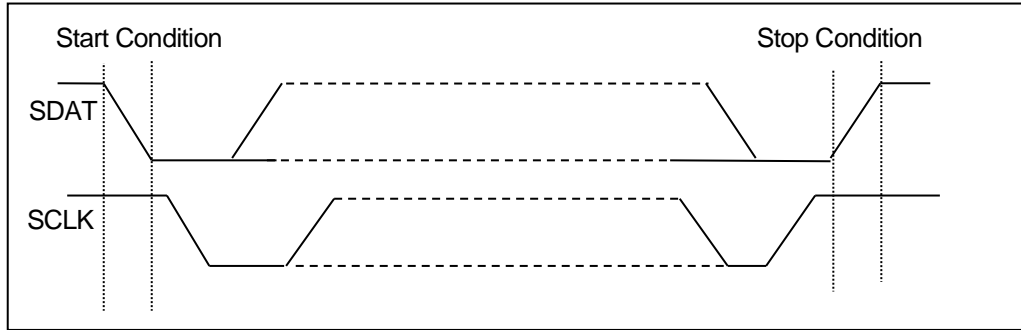


FIGURE 23. DEFINITION OF THE SERIAL BUS INTERFACE BUS START AND STOP

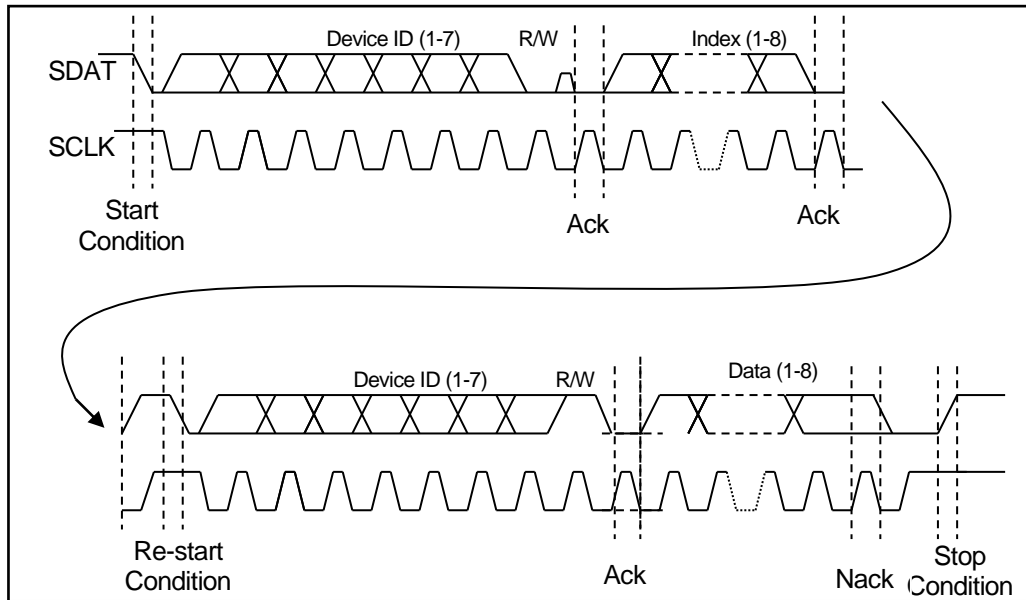


FIGURE 24. ONE COMPLETE REGISTER READ SEQUENCE VIA THE SERIAL BUS INTERFACE

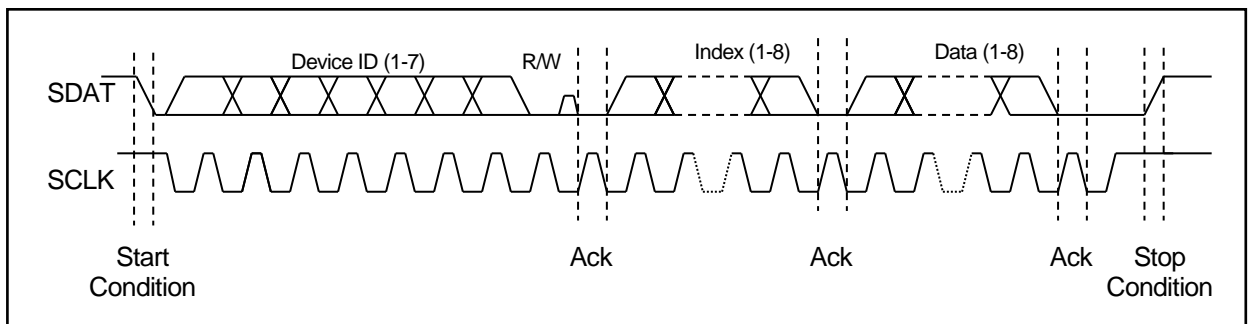


FIGURE 25. ONE COMPLETE REGISTER WRITE SEQUENCE VIA THE SERIAL BUS INTERFACE

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the TW2984 registers. SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by resistors connected to VDD0. ICs communicate on the bus by pulling SCLK and SDAT low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDAT line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCLK is high.

The TW2984 is operated as a bus slave device. It can be programmed to respond to one of two 7-bit slave device addresses by tying the SIAD[1:0] (Serial Interface Address) pins to either VDD00 or VSS (See below Table) through a pull-up or pull-down resistor. The SIAD[1:0] pins are multi-purpose pins and must not be tied to supply voltage or ground directly. If the SIAD[1:0] pins are tied to VDD00, then the least significant 2-bit of the 7-bit address is a "11". If the SIAD[1:0] pins are tied to VSS then the least significant 2-bit of the 7-bit address is a "00". The most significant 5-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high, the next byte will be read from the slave device. If it is low, the next byte will be a write to the slave. When a bus master (the host microprocessor) drives SDAT from high to low, while SCLK is high, this is defined to be a start condition (See Figure 23). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 24. (For the TW2984, the next byte is normally the index to the TW2984 registers and is a write to the TW2984 therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the SDAT line while holding SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDAT line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

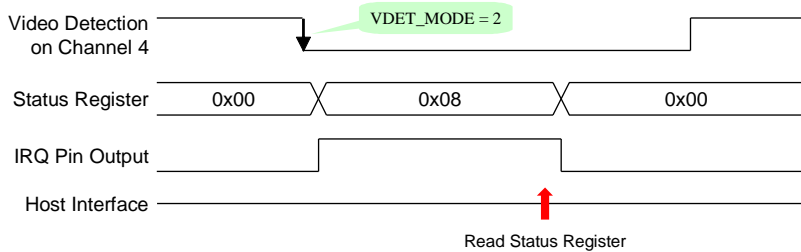
To write to the internal register of the TW2984, the master sends another 8-bits of data, the TW2984 loads this to the register pointed to by the internal index register. The TW2984 will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the TW2984 if they are in ascending sequential order. After each 8-bit transfer, the TW2984 will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the TW2984 the host will issue a stop condition.

SERIAL BUS INTERFACE 7-BIT SLAVE ADDRESS							READ/WRITE BIT
0	1	0	1	0	SIAD[1]	SIAD[0]	1=Read 0=Write

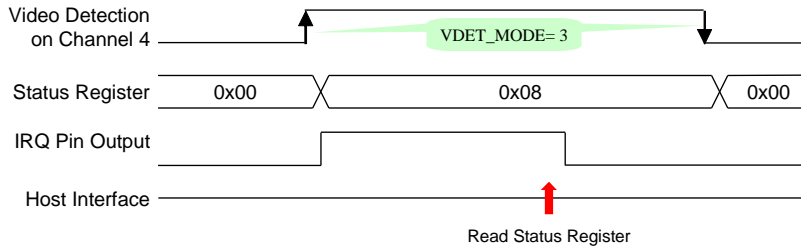
A TW2984 read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See Figure 28). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDAT line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDAT is left high during a clock pulse) and issue a stop condition.

Interrupt Interface

The TW2984 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video or audio signal from TW2984. To use interrupt request function, the interrupt request should be enabled by the IRQENA and polarity of the IRQ pin should be selected by the IRQPOL. In addition, each channel of video and audio detection should be enabled by the AVDET_ENA. Then, the interrupt mode should be defined by the VDET_MODE and ADET_MODE that control the time to request interrupt and set the status register AVDET_STATE. Figure 26 shows operation of interrupt when the VDET_MODE and/or ADET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading the AVDET_STATE. When the VDET_MODE and/or ADET_MODE are 1 or 2, the status register AVDET_STATE will also be cleared automatically by reading AVDET_STATE. However, when the VDET_MODE and/or ADET_MODE are 3, the status register AVDET_STATE will not be cleared automatically, but has the same value as actual status of video and audio detection flag.



(A) STATUS REGISTER OF AUTOMATIC CLEARED MODE



(B) STATUS REGISTER SAME AS VIDEO AND AUDIO DETECTION FLAG MODE

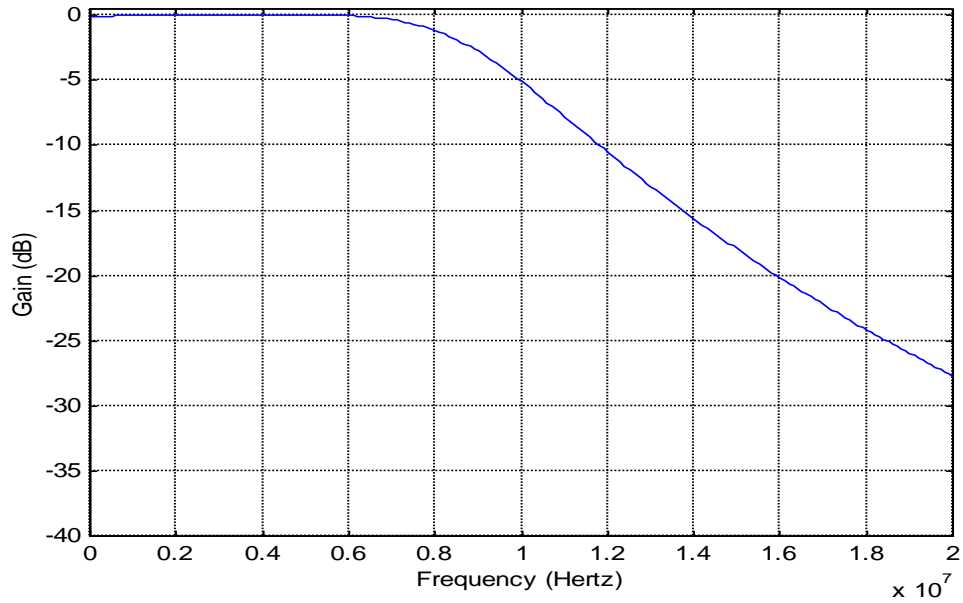
FIGURE 26. TIMING DIAGRAM OF INTERRUPT INTERFACE

Clock PLL

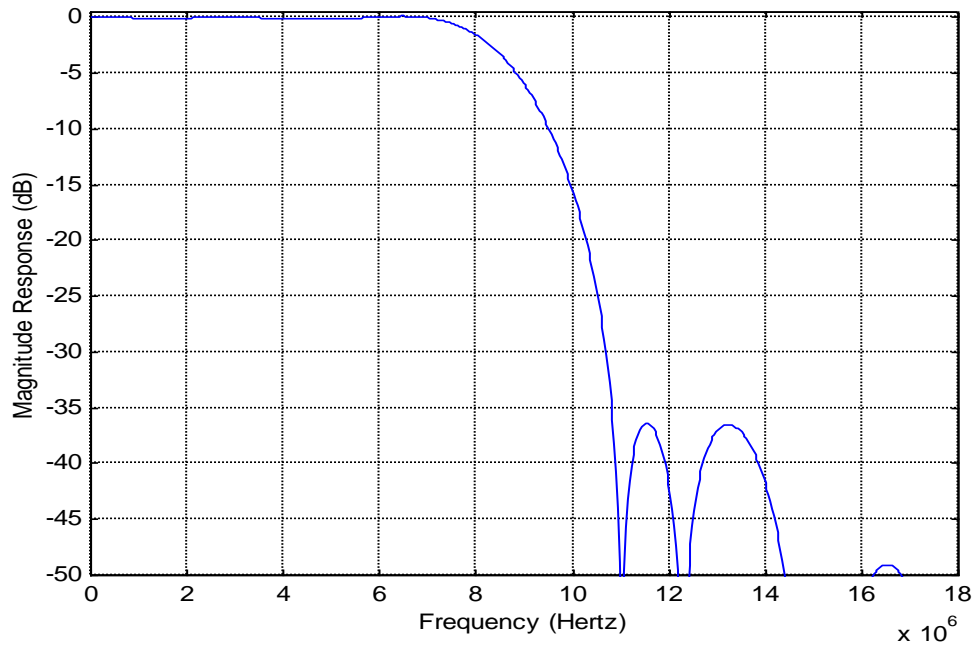
The TW2984 has built-in clock PLL. It generates 108MHz clock and 144MHz clock from 27MHz input reference clock.

Video Decoder Filter Curves

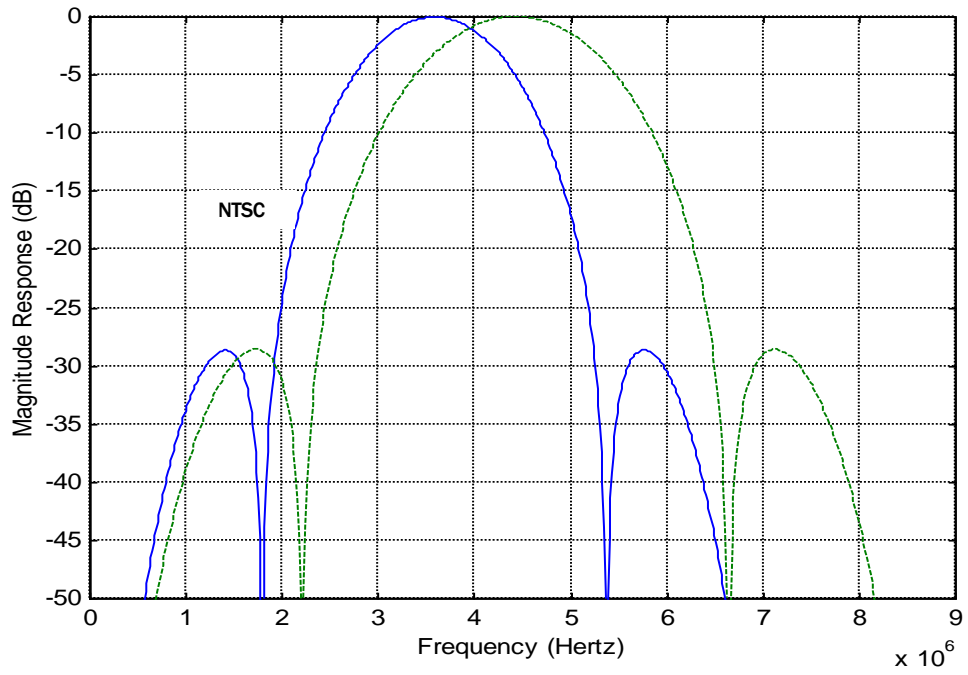
ANTI-ALIAS FILTER



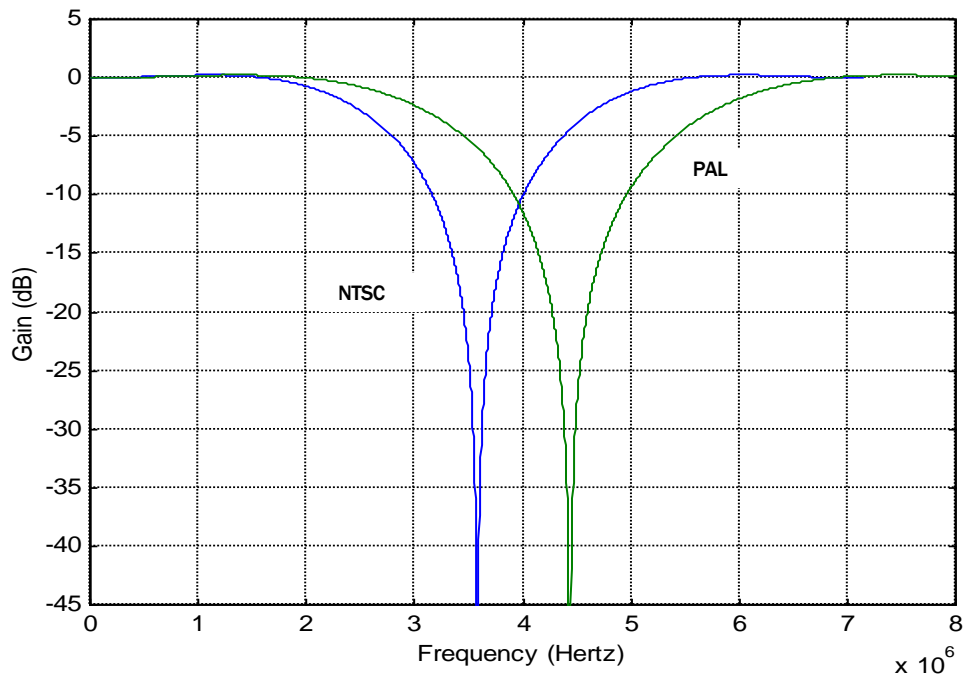
DECIMATION FILTER



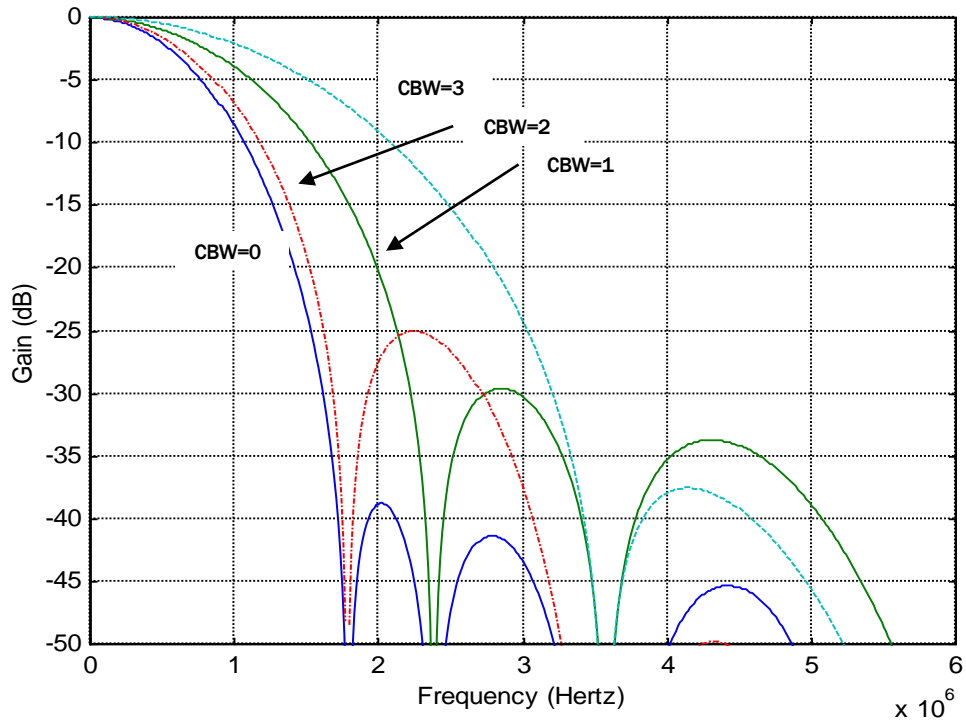
CHROMA BAND PASS FILTER CURVES



LUMA NOTCH FILTER CURVE FOR NTSC AND PAL

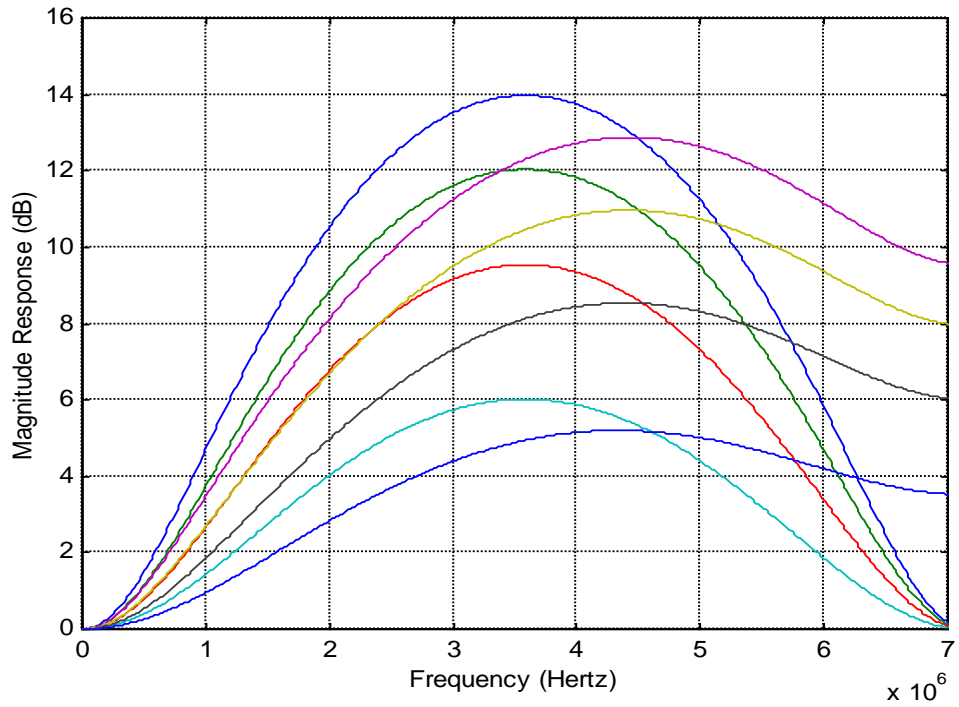


CHROMINANCE LOW-PASS FILTER CURVE

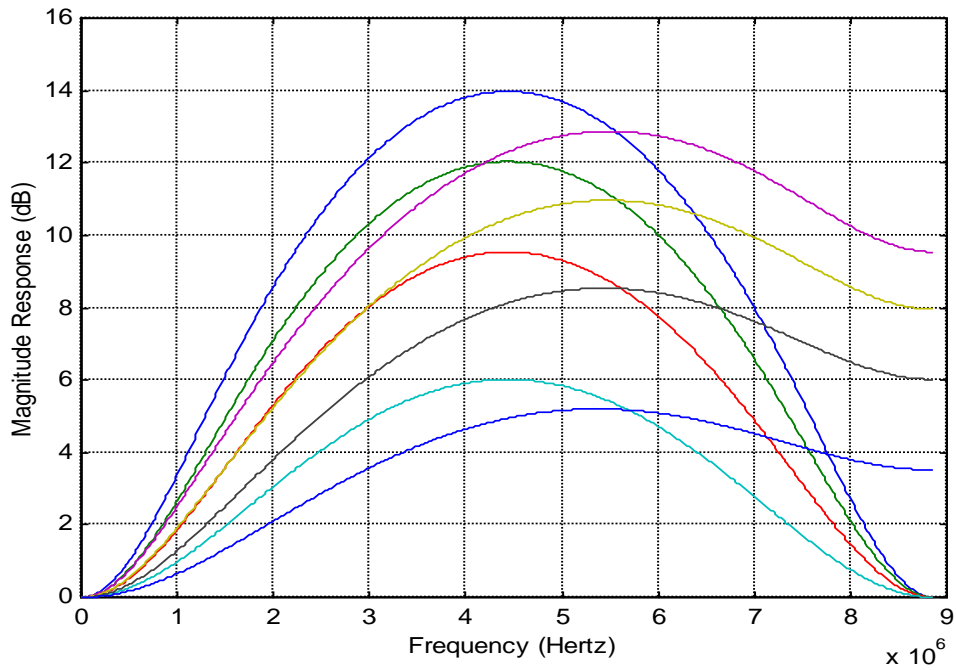


PEAKING FILTER CURVES

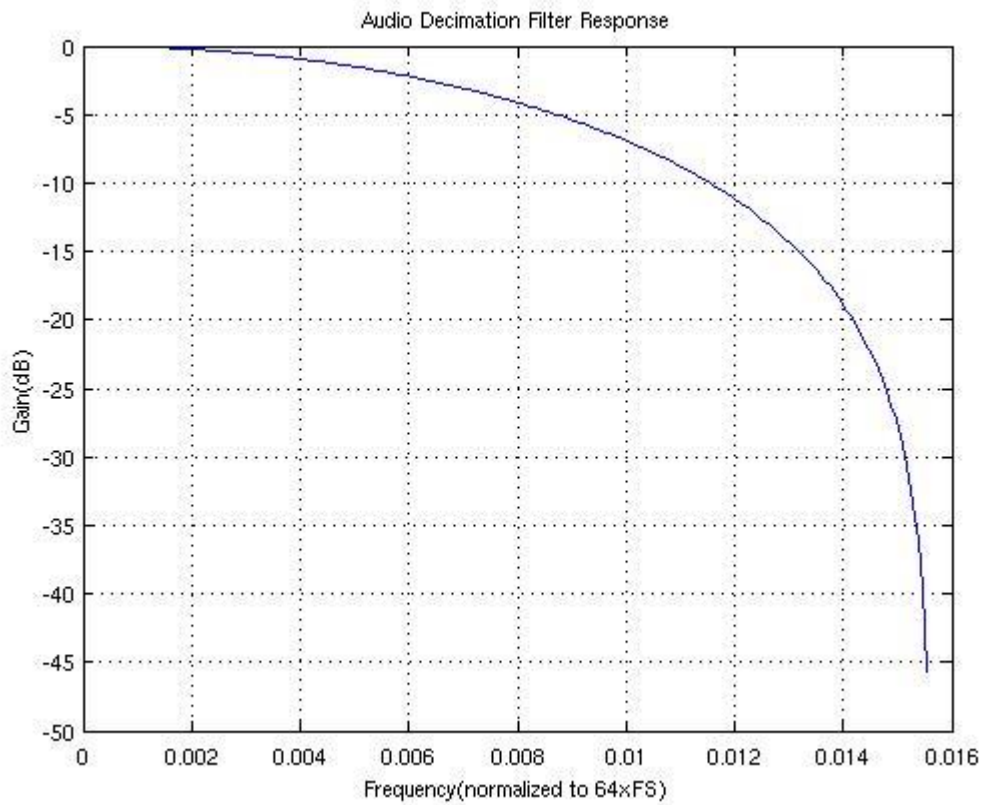
NTSC



PAL



Audio Decimation Filter Response



(*) 0.016 line = $0.016 \times 64 \times F_s$

Control Register

REGISTER MAP

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x00	0x10	0x20	0x30	VIDSTAT *	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	Reserved*	MONO*	DET50*
0x01	0x11	0x21	0x31	BRIGHT	BRIGHTNESS							
0x02	0x12	0x22	0x32	CONTRAST	CONTRAST							
0x03	0x13	0x23	0x33	SHARPNESS	SCURVE	VSF	CTI		SHARPNESS			
0x04	0x14	0x24	0x34	SAT_U	SAT_U							
0x05	0x15	0x25	0x35	SAT_V	SAT_V							
0x06	0x16	0x26	0x36	HUE	HUE							
0x07	0x17	0x27	0x37	CROP_HI	VDELAY[9:8]		VACTIVE[9:8]		HDELAY[9:8]		HACTIVE[9:8]	
0x08	0x18	0x28	0x38	VDELAY_LO	VDELAY[7:0]							
0x09	0x19	0x29	0x39	VACTIVE_LO	VACTIVE[7:0]							
0x0A	0x1A	0x2A	0x3A	HDELAY_LO	HDELAY[7:0]							
0x0B	0x1B	0x2B	0x3B	HACTIVE_LO	HACTIVE[7:0]							
0x0C	0x1C	0x2C	0x3C	MVSN*	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE*
0x0D	0x1D	0x2D	0x3D	STATUS2*	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	0	0	0
0x0E	0x1E	0x2E	0x3E	SDT	DETSTUS*	STDNOW*			ATREG	STANDARD		
0x0F	0x1F	0x2F	0x3F	SDTR	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
0xA0	0xA1	0xA2	0xA3	NT50	NT50	CVSTD*			CVFMT			
0xA4	0xA5	0xA6	0xA7	IDCNTL	IDX		NSEN/SSEN/PSEN/WKTH					
0xC4	0xC5	0xC6	0xC7	HREF*	HREF*							

Note: * Read only registers

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x50				VDFREQ	VD4FREQ	VD3FREQ	VD2FREQ	VD1FREQ	H960EN4	H960EN3	H960EN2	H960EN1
0x51				FBITINV	0	0	0	0	FBITINV4	FBITINV3	FBITINV2	FBITINV1
0x52				ANADACTEST	VCM_SEL	LPF_SEL			BIAS_SEL	AN_ADACTEST		
0x54				ASAVE	0	ADACLK_INV	DOUT_RST	DIV_RST	ACALEN	ASAVE		
0x55				AAFLPF	AAFLPF4		AAFLPF3		AAFLPF2		AAFLPF1	
0x56				HASYNC	HASYNC4	HASYNC3	HASYNC2	HASYNC1	HBLEN4[8]	HBLEM3[8]	HBLEN2[8]	HBLEN1[8]
0x57				HBLEN1	HBLEM1[7:0]							
0x58				HBLEN2	HBLEM2[7:0]							
0x59				HBLEN3	HBLEM3[7:0]							

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x5A				HLEN4	HLEN4[7:0]							
0x5B				CKDS	0	0	0	0	PLLCKOUT	XTI36	CKN_DS	CLP_DS
0x5C				BGCTL	0	0	BGCTL	VSWEN	VSWNUM			
0x5D				CH2MISC2	NKILL_2	PKILL_2	SKILL_2	CBAL_2	FCS_2	LCS_2	CCS_2	BST_2
0x5E				CH3MISC2	NKILL_3	PKILL_3	SKILL_3	CBAL_3	FCS_3	LCS_3	CCS_3	BST_3
0x5F				CH4MISC2	NKILL_4	PKILL_4	SKILL_4	CBAL_4	FCS_4	LCS_4	ICCS_4	BST_4
0x60				VCO	CLK_DIFF	CP_SEL			LP_X8		VCO	
0x61				XTIMD	PLL_RST	PLL_PD	PLL_IREF	DECOSC	SEL_144_72	SEL_108_54	XTIMD	
0x62				O36M	O36M4	O36M3	O36M2	O36M1				
0x63				CH21NUM	CH2NUM				CH1NUM			
0x64				CH43NUM	CH4NUM				CH3NUM			
0x65				VDOEB	0	0	0	VD40RD	0	VDOEB	0	0
0x67				HZST	HZST							
0x68				HZOOM_HI	HZOOM4[9:8]		HZOOM3[9:8]		HZOOM2[9:8]		HZOOM1[9:8]	
0x69				HZOOM1_LOW	HZOOM1[7:0]							
0x6A				HZOOM2_LOW	HZOOM2[7:0]							
0x6B				HZOOM3_LOW	HZOOM3[7:0]							
0x6C				HZOOM4_LOW	HZOOM4[7:0]							
0x6D				D1 NMGAIN	NMGAIN720				SHCOR720			
0x6E				PCLAMP720	PCLAMP720							
0x70				ACLKPOL	ACK36MD	S2I_8BIT	ACLKRPOL	ACLKPPOL	AFAUTO	AFMD		
0x71				AINCTL	I2S8MODE	MASCKMD	PBINSWAP	ASYNDRDLY	ASYNPDLY	ADATPDLY	INLAWMD	
0x72				MRATIOMD	MRATIOMD	ADACTEST	AOFFCORE	DAORATIO	DAOGAIN			
0x73				A5NUM	Reserved				AIN51FORM	AINTPOFF	A51DET_ENA	
0x74				A5DETST	0	0	0	0	0	0	0	A5DET_STATE*
0x75				AADC50FS_H	0	0	0	0	0	0	AADC50FS[9:8]	
0x76				AADC50FS_L	AADC50FS[7:0]							
0x77				AUD5ADC_H	0	0	0	0	0	0	AUD5ADC[9:8]	
0x78				AUD5ADC_L	AUD5ADC[7:0]							
0x79				ADJAADC5_H	0	0	0	0	0	0	ADJAADC5[9:8]	
0x7A				ADJAADC5_L	ADJAADC5[7:0]							
0x7B				I2S0_RSEL	0	0	0	I2S0_RSEL				
0x7C				I2S0_LSEL	0	0	0	I2S0_LSEL				
0x7D				RECSEL5	I2SRECSEL54		I2SRECSEL53		I2SRECSEL52		I2SRECSEL51	
0x7E				ADATMI2S	A5OUTOFF	ADATM_I2SOEN	MIX_MUTE_A5	ADET_TH5[4:0]				
0x7F				AIGAIN5	AIGAIN5				MIX_RATIO5			
0x80				SRST	0	0	AUDIORST	VOUSTRST	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST
0x81				ACNTL	0	0	0	0	CLKPDN	0	YFLEN	0

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
CH1	CH2	CH3	CH4										
	0x82			ACNTL2	CTEST	YCLEN	CKIPOL	0	GTEST	VLPF	CKLY	CKLC	
	0x83			CNTRL1	PBW	DEM	IDSNS	SET7	COMB	HCOMP	YCOMB	PDLY	
	0x84			CKHY	GMEN	CKHY		HSDLY					
	0x85			SHCOR960	SHCOR960			VIN4	VIN3	VIN2	VIN1		
	0x86			CORING	CTCOR		CCOR	VCOR		CIF			
	0x87			CLMPG	CLPEND			CLPST					
	0x88			IAGC	NMGAIN960			WPGAIN				0	
	0x89			AIN5MD	ATHROUGH	ASYN SERIAL	ACLKR128	ACLKR64	AFS384	AIN5MD	0	0	
	0x8A			PEAKWT	PEAKWT								
	0x8B			CLMPL	CLMPLD	CLMPL							
	0x8C			SYNCT	SYNCTD	SYNCT							
	0x8D			MISSCNT	MISSCNT			HSWIN					
	0x8E			PCLAMP960	PCLAMP960								
	0x8F			VCNTL1	VLCKI		VLCKO	VMODE	DETV	AFLD	VINT		
	0x90			VCNTL2	BSHT			VSHT					
	0x91			CKILL	CKILMAX			CKILMIN					
	0x92			VTL	HTL			VTL					
	0x93			LDLY	CKLM	YDLY		PD_BIAS	VSAVE				
	0x94			MISC1	HPLC	EVCNT	PALC	SDET	0	BYPASS	0		
	0x95			CBW	HPM		ACCT		SPM		CBW		
	0x96			MISC2	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST	
	0x97			CLMD	FRM		YNR		CLMD		PSP		

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x9C				OVSEND	0		OFDLY		0	0	0	0
0x9E				NOVID	VDELAYMD	FC27	CHID_MD		NOVID_656	EAVSWAP	VIPCFG	NTSC656
0x9F				CLKODEL	CLKNO_DEL				CLKPO_DEL			
0xAA				AGCEN	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0xAB				AGCGAIN1	AGCGAIN1[7:0]							
0xAC				AGCGAIN2	AGCGAIN2[7:0]							
0xAD				AGCGAIN3	AGCGAIN3[7:0]							
0xAE				AGCGAIN4	AGCGAIN4[7:0]							
0xAF				VSH2P1	0	VSH2P2			0	VSH2P1		
0xB0				VSH2P4	0	VSH2P4			0	VSH2P3		
0xB1				CH8IDEN	CH8IDEN	0	0	0	CLPOE	TESTVNUM		
0xB2				VADC_CKPOL	VADC_CKPOL4	VADC_CKPOL3	VADC_CKPOL2	VADC_CKPOL1				
0xB3				AADC0FS_H	AADC40FS[9:8]		AADC30FS[9:8]		AADC20FS[9:8]		AADC10FS[9:8]	
0xB4				AADC10FS_L	AADC10FS[7:0]							
0xB5				AADC20FS_L	AADC20FS[7:0]							
0xB6				AADC30FS_L	AADC30FS[7:0]							
0xB7				AADC40FS_L	AADC40FS[7:0]							
0xB8				AUDADC_H*	AUD4ADC[9:8]		AUD3ADC[9:8]		AUD2ADC[9:8]		AUD1ADC[9:8]	
0xB9				AUD1ADC_L*	AUD1ADC[7:0]							
0xBA				AUD2ADC_L*	AUD2ADC[7:0]							
0xBB				AUD3ADC_L*	AUD3ADC[7:0]							
0xBC				AUD4ADC_L*	AUD4ADC[7:0]							
0xBD				ADJAADC_H*	ADJAADC4[9:8]		ADJAADC3[9:8]		ADJAADC2[9:8]		ADJAADC1[9:8]	
0xBE				ADJAADC1_L*	ADJAADC1[7:0]							
0xBF				ADJAADC2_L*	ADJAADC2[7:0]							
0xC0				ADJAADC3_L*	ADJAADC3[7:0]							
0xC1				ADJAADC4_L*	ADJAADC4[7:0]							

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
CH1	CH2	CH3	CH4										
0xCA				CHMD	CHMD								
0xCC				SELCH	SELCH								
0xCD				MAINCH	MAINCH								
0xCE				ANAPWDN	AAUTOMUTE	Reserved	A_DAC_PWDN	A_ADC_PWDN	VADC_PWDN				
0xCF				SMD	SMD		0	0	0	0	0	0	0
0xD0				AIGAIN21	AIGAIN2				AIGAIN1				
0xD1				AIGAIN43	AIGAIN4				AIGAIN3				
0xD2				R_MULTCH	M_RLSWAP	RM_SYNC	RM_PBSEL		R_ADATM		R_MULTCH		
0xD3				R_SEQ10	R_SEQ_1				R_SEQ_0				
0xD4				R_SEQ32	R_SEQ_3				R_SEQ_2				
0xD5				R_SEQ54	R_SEQ_5				R_SEQ_4				
0xD6				R_SEQ76	R_SEQ_7				R_SEQ_6				
0xD7				R_SEQ98	R_SEQ_9				R_SEQ_8				
0xD8				R_SEQBA	R_SEQ_B				R_SEQ_A				
0xD9				R_SEQDC	R_SEQ_D				R_SEQ_C				
0xDA				R_SEQFE	R_SEQ_F				R_SEQ_E				

Address				Mnemonic	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
CH1	CH2	CH3	CH4										
0xDB				AMASTER	ADACEN	AADCEN	PB_MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMMASTER	
0xDC				MIX_MUTE	LAWMD		MIX_DERATIO	MIX_MUTE					
0xDD				MIX_RATIO21	MIX_RATIO2			MIX_RATIO1					
0xDE				MIX_RATIO43	MIX_RATIO4			MIX_RATIO3					
0xDF				MIX_RATIOP	AOGAIN			MIX_RATIOP					
0xE0				MIX_OUTSEL	0	AADCCKPOL	ADACCKPOL	MIX_OUTSEL					
0xE1				ADET	AAMPMD	ADET_FILTER		ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]		
0xE2				ADET_TH21	ADET_TH2[3:0]			ADET_TH1[3:0]					
0xE3				ADET_TH43	ADET_TH4[3:0]			ADET_TH3[3:0]					
0xF0				ACKI_L	ACKI[7:0]								
0xF1				ACKI_M	ACKI[15:8]								
0xF2				ACKI_H	0	0	ACKI[21:16]						
0xF3				ACKN_L	ACKN[7:0]								
0xF4				ACKN_M	ACKN[15:8]								
0xF5				ACKN_H	0	0	0	0	0	0	ACKN[17:16]		
0xF6				SDIV	0	0	SDIV						
0xF7				LRDIV	0	0	LRDIV						
0xF8				ACCNTL	APZ	APG		Reserved	ACPL	SRPH	LRPH		
0xF9				VMISC	LIM16	PBREFEN	YCBCR422	Reserved	VBI_FRAM	CNTL656	CLKNF	CLKPF	
0xFA				CLKOCTL	0	OE	CLKNO_OEB	CLKPO_OEB	CLKNO_MD		CLKPO_MD		
0xFB				AVDET_MODE	CLKNO_POL	CLKPO_POL	IRQENA	IRQPOL	ADET_MODE		VDET_MODE		
0xFC				AVDET_ENA	AVDET_ENA								
0xFD				AVDET_STATE*	AVDET_STATE								
0xFE				TEST	DEV_ID[6:5]*		0	0	0	TEST			
0xFF				DEV_ID*	DEV_ID[4:0]*					REV_ID			

Note: * Read only registers

Register Descriptions

0X00(CH1)/0X10(CH2)/0X20(CH3)/0X30(CH4) – VIDEO STATUS REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDLOSS	R	1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected.	0
6	HLOCK	R	1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked.	0
5	SLOCK	R	1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked.	0
4	FIELD	R	0 = Odd field is being decoded. 1 = Even field is being decoded.	0
3	VLOCK	R	1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked.	0
2	Reserved	R	Reserved	0
1	MONO	R	1 = No color burst signal detected. 0 = Color burst signal detected.	0
0	DET50	R	0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked.	0

0X01(CH1)/0X11(CH2)/0X21(CH3)/0X31(CH4) – BRIGHTNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	BRIGHT	R/W	These bits control the brightness. They have value of -128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data.	00

0X02(CH1)/0X12(CH2)/0X22(CH3)/0X32(CH4) – CONTRAST CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	CNTRST	R/W	These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step.	64h

0X03(CH1)/0X13(CH2)/0X23(CH3)/0X33(CH4) – SHARPNESS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SCURVE	R/W	This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center	0
6	VSF	R/W	This bit is for internal used.	0
5-4	CTI	R/W	CTI level selection. 0 = None. 3 = highest.	1
3-0	SHARP	R/W	These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest.	1

0X04(CH1)/0X14(CH2)/0X24(CH3)/0X34(CH4) – CHROMA (U) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_U	R/W	These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%.	80

0X05(CH1)/0X15(CH2)/0X25(CH3)/0X35(CH4) – CHROMA (V) GAIN REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	SAT_V	R/W	These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%.	80

0X06(CH1)/0X16(CH2)/0X26(CH3)/0X36(CH4) – HUE CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HUE	R/W	These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system.	00

0X07(CH1)/0X17(CH2)/0X27(CH3)/0X37(CH4) – CROPPING REGISTER, HIGH

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Vertical Delay register.	0
5-4	VACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register.	1
3-2	HDELAY_HI	R/W	These bits are bit 9 to 8 of the 10-bit Horizontal Delay register.	0
1-0	HACTIVE_HI	R/W	These bits are bit 9 to 8 of the 10-bit HACTIVE register.	2

0X08(CH1)/0X18(CH2)/0X28(CH3)/0X38(CH4) – VERTICAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VDELAY_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video.	12

0X09(CH1)/0X19(CH2)/0X29(CH3)/0X39(CH4) – VERTICAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	VACTIVE_LO	R/W	These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output. The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.	20

0X0A(CH1)/0X1A(CH2)/0X2A(CH3)/0X3A(CH4) – HORIZONTAL DELAY REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HDELAY_LO	R/W	<p>These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video.</p> <p>The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.</p>	0A

0X0B(CH1)/0X1B(CH2)/0X2B(CH3)/0X3B(CH4) – HORIZONTAL ACTIVE REGISTER, LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HACTIVE_LO	R/W	<p>These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.</p>	D0

0X0C(CH1)/0X1C(CH2)/0X2C(CH3)/0X3C(CH4) – MACROVISION DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SF	R	This bit is for internal use.	0
6	PF	R	This bit is for internal use.	0
5	FF	R	This bit is for internal use.	0
4	KF	R	This bit is for internal use.	0
3	CSBAD	R	1 = Macrovision color stripe detection may be un-reliable	0
2	MVCSN	R	1 = Macrovision AGC pulse detected. 0 = Not detected.	0
1	CSTRIPE	R	1 = Macrovision color stripe protection burst detected. 0 = Not detected.	0
0	CTYPE	R	This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection	0

0X0D(CH1)/0X1D(CH2)/0X2D(CH3)/0X3D(CH4) – CHIP STATUS II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCR	R	VCR signal indicator.	0
6	WKAIR	R	Weak signal indicator 2.	0
5	WKAIR1	R	Weak signal indicator controlled by WKTH.	0
4	VSTD	R	1 = Standard signal 0 = Non-standard signal	0
3	NINTL	R	1 = Non-interlaced signal 0 = interlaced signal	0
2-0	Reserved	R	Reserved	0h

0X0E(CH1)/0X1E(CH2)/0X2E(CH3)/0X3E(CH4) – STANDARD SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	DETSTUS	R	0 = Idle 1 = detection in progress	0
6-4	STDNOW	R	Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid	0
3	ATREG	R/W	1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard	0
2-0	STD	R/W	Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM(not supported) 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection	7

0X0F(CH1)/0X1F(CH2)/0X2F(CH3)/0X3F(CH4) – STANDARD RECOGNITION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATSTART	R/W	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit.	0
6	PAL6_EN	R/W	1 = enable recognition of PAL60. 0 = disable recognition.	1
5	PALN_EN	R/W	1 = enable recognition of PAL (CN). 0 = disable recognition.	1
4	PALM_EN	R/W	1 = enable recognition of PAL (M). 0 = disable recognition.	1
3	NT44_EN	R/W	1 = enable recognition of NTSC 4.43. 0 = disable recognition.	1
2	SEC_EN	R/W	1 = enable recognition of SECAM. 0 = disable recognition.	1
1	PALB_EN	R/W	1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition.	1
0	NTSC_EN	R/W	1 = enable recognition of NTSC (M). 0 = disable recognition.	1

0X56(CH1/CH2/CH3/CH4) – HASYNC

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HASYNC4	R/W	1: the length of EAV to SAV is set up and fixed by CH4 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by CH4 HACTIVE registers.	0
6	HASYNC3	R/W	1: the length of EAV to SAV is set up and fixed by CH3 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by CH3 HACTIVE registers.	0
5	HASYNC2	R/W	1: the length of EAV to SAV is set up and fixed by CH2 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by CH2 HACTIVE registers.	0
4	HASYNC1	R/W	1: the length of EAV to SAV is set up and fixed by CH1 HBLEN registers. 0: the length of SAV to EAV is set up and fixed by CH1 HACTIVE registers.	0
3	HBLEN4[8]	R/W	Bit8 of CH4 HBLEN[8:0].Please see HBLEN description.	0
2	HBLEN3[8]	R/W	Bit8 of CH3 HBLEN[8:0]. Please see HBLEN description.	0
1	HBLEN2[8]	R/W	Bit8 of CH2 HBLEN[8:0]. Please see HBLEN description.	0
0	HBLEN1[8]	R/W	Bit8 of CH1 HBLEN[8:0]. Please see HBLEN description.	0

0X57(CH1)/0X58(CH2)/0X59(CH3)/0X5A(CH4) – HBLEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HBLENn[7:0] n=1,2,3,4	R/W	These bits are effective when HASYNC bit is set to 1. These bits set up the length of EAV to SAV code when HASYNC bit is 1. Normal value is (Total pixel per line – HACTIVE) value. HBLENn[8] is 0 normally. HBLENn[8] is optional purpose only. 36MHz WD1 Vdeo Decoder mode. NTSC/PAL-M(60Hz): B8h(184dec)=1144-960 PAL/SECAM(50Hz): C0h(192dec)=1152-960 27MHz D1 Vdeo Decoder mode. NTSC/PAL-M(60Hz): 8Ah(138dec)=858-720 PAL/SECAM(50Hz): 90h(144dec)=864-720	90h

0X68(CH1/CH2/CH3/CH4) – HZOOM_HI

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HZOOM4 [9:8]	R/W	Bit9-8 of CH4 HZOOM registers.	0
5-4	HZOOM3 [9:8]	R/W	Bit9-8 of CH3 HZOOM registers.	0
3-2	HZOOM2 [9:8]	R.W	Bit9-8 of CH2 HZOOM registers.	0
1-0	HZOOM1 [9:8]	R/W	Bit9-8 of CH1 HZOOM registers.	0

0X69(CH1)/0X6A(CH2)/0X6B(CH3)/0X6C(CH4) – HZOOM_LOW

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HZOOM [7:0]	R/W	Bit7-0 of Horizontal Zoom Up register. This register has Horizontal Zoom Up function together HZOOMn[9:8] by following equation. $HZOOM[9:0] = 1024 \times \text{source H pixel number} / \text{output H pixel number}$. For example, source H pixel number = 948 Output H pixel number = 960 $HZOOM[9:0] = 1024 \times 948 / 960 = 1011.2 = 3F3h$. If HZOOM=000h is set up, No HZOOM(path through) output.	00h

0XA0(CH1)/0XA1(CH2)/0XA2(CH3)/0XA3(CH4) – NT50

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NT50	R/W	1 = Force decoding format to 50Hz NTSC. 0 = decoding format is set by register Standard Selection.	0
6-4	VSTD	R/W	Reserved	0h
3-0	CVFMT	R/W	Reserved	8h

0XA4(CH1)/0XA5(CH2)/0XA6(CH3)/0XA7(CH4) – ID DETECTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	IDX	R/W	These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register.	0
5-0	NSEN / SSEN / PSEN / WKTH	R/W	IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH).	1A / 20 / 1C / 11

0XAA(CH1/CH2/CH3/CH4) – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AGCEN4	R/W	Select Video AGC loop function on VIN4 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN4	0
6	AGCEN3	R/W	Select Video AGC loop function on VIN3 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN3	0
5	AGCEN2	R/W	Select Video AGC loop function on VIN2 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN2	0
4	AGCEN1	R/W	Select Video AGC loop function on VIN1 0: AGC loop function enabled (recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN1	0
3	AGCGAIN4[8]	R/W	AGCGAIN4 MSB bit	0
2	AGCGAIN3[8]	R/W	AGCGAIN3 MSB bit	0
1	AGCGAIN2[8]	R/W	AGCGAIN2 MSB bit	0
0	AGCGAIN1[8]	R/W	AGCGAIN1 MSB bit	0

0XAB(CH1)/0XAC(CH2)/0XAD(CH3)/0XAE(CH4) – VIDEO AGC CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AGCGAIN[7:0]	R/W	To control the AGC Gain when AGC loop is disabled. AGCGAIN bit7-0.	F0h

0XC4(CH1)/0XC5(CH2)/0XC6(CH3)/0XC7(CH4) – H MONITOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HFREF	R	Horizontal line frequency indicator (Test purpose only)	X

0X50 – VDFREQ/H960EN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6	VDFREQ	R/W	1 : VD[7:0] pin output 36MHz video data. 0 : VD[7:0] pin output 27MHz video data.	0
5-4	Reserved	R/W		0h
3	H960EN4	R/W	1 : Ch4 video decoder is in 36MHz WD1 mode. 0 : Ch4 video decoder is in 27MHz D1 mode.	0
2	H960EN3	R/W	1 : Ch3 video decoder is in 36MHz WD1 mode. 0 : Ch3 video decoder is in 27MHz D1 mode.	0
1	H960EN2	R/W	1 : Ch2 video decoder is in 36MHz WD1 mode. 0 : Ch2 video decoder is in 27MHz D1 mode.	0
0	H960EN1	R/W	1 : Ch1 video decoder is in 36MHz WD1 mode. 0 : Ch1 video decoder is in 27MHz D1 mode.	0

0X51 – FBITINV

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0h
3	FBITINV4	R/W	1 : F-bit in 4th byte of 656 EAV/SAV code is inverted. 0 : normal mode.F-bit is not inverted.	0
2	FBITINV3	R/W	1 : F-bit in 4th byte of 656 EAV/SAV code is inverted. 0 : normal mode.F-bit is not inverted.	0
1	FBITINV2	R/W	1 : F-bit in 4th byte of 656 EAV/SAV code is inverted. 0 : normal mode.F-bit is not inverted.	0
0	FBITINV1	R/W	1 : F-bit in 4th byte of 656 EAV/SAV code is inverted. 0 : normal mode.F-bit is not inverted.	0

0X52 – AUDIO DAC CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VCM_SEL	R/W	Reserved.	0
5-4	LPF_SEL	R/W	Audio DAC LPF corner frequency selection. 0h : 15.6kHz 1h : 7.8kHz 2h : Don't use 3h : 3.9kHz 4h,5h,6h : Don't use 7h : 2.6kHz	0
3	BIAS_SEL	R/W	Bias selection. 0 : AVDD33 as the reference voltage. 1 : select bandgap voltage as the reference.	0
2-0	ADACTEST	R/W	Audio DAC Test control. 0h : normal operation 1h : ibias places to the dac_out(Don't use) 2h : din_0 is placed to the dac_out(Don't use) 3h : both ibias and din_0 are placed at the dac_out(Don't use) 4h : disable output driver.Dac_out floating 5h : disable output driver,ibias places to dac_out 6h : disable output driver,din_0 places to dac_out 7h : don't use	0

0X54 – AUDIO ADC CONTROL 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6	ADACLK_INV	R/W	Audio DAC clock inversion. 0 : not inversed inside audio DAC. 1 : Clock is inversed inside audio DAC.	0
5	DOUT_RST	R/W	Audio ADC digital output reset for all channel. Test purpose only. This bit must be set up to 0 again after 1 value is set up.	0
4	DIV_RST	R/W	Audio ADC divider reset.Test purpose Only. This bit must be set up to 0 again after 1 value is set up.	0
3	ACALEN	RW	Audio ADC Calibration control.Test purpose only. This bit must be set up to 0 again after 1 value is set up.	0
2-0	ASAVE	R/W	7h : normal mode. Others : test purpose only.	7

0X55 – VIDEO INPUT ANTI-ALIASING FILTER SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AAFLPF4	R/W	Ch4 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
5-4	AAFLPF3	R/W	Ch3 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
3-2	AAFLPF2	R/W	Ch2 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0
1-0	AAFLPF1	R/W	Ch1 Video input Anti-aliasing filter selection. 0h : 9MHz,0dB gain. 1h : 10MHz,-3.4dB gain. 2h : 7MHz,0db gain. 3h : 8MHz,-3.4dB gain.	0

0X5B – CLOCK OUTPUT PIN DRIVE SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R		0
3	PLLCKOUT	R/W	1 : IRQ pin output PLL 36MHz clock. CLKPO pin output PLL 144MHz clock. CLKNO pin output PLL 108MHz clock. Test purpose only. 0 : normal mode.	0
2	XTI36	R/W	0 : XTI pin is normal 27MHz input. 1 : Special WD1 mode.XTI pin is one of 36MHz/72MHz/144MHz input. 27MHz/54MHz/108MHz D1 mode is not supported in this special mode.	0
1	CKN_DS	R/W	0 : CLKNO pin output is 12mA current drive mode. 1 : CLKNO pin output is 16mA current drive mode.	0
0	CKP_DS	R/W	0 : CLKPO pin output is 12mA current drive mode. 1 : CLKPO pin output is 16mA current drive mode.	0

0X5C- BGCTL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5	BGCTL	R/W	0: Reg96[7:0] control all CH1/CH2/CH3/CH4 video. 1: Reg96[7:0] control only CH1 video. Reg5D[7:0] control only CH2 video. Reg5E[7:0] control only CH3 video. Reg5F[7:0] control only CH4 video.	0
4-0	Reserved	R/W		0h

0X5D – CH2 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_2	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_2	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_2	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_2	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_2	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_2	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_2	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_2	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5E – CH3 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_3	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_3	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_3	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_3	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_3	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_3	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_3	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_3	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X5F – CH4 MISCELLANEOUS CONTROL II ON BGCTL=1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL_4	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL_4	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL_4	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL_4	R/W	0 = Normal output 1 = special output mode.	0
3	FCS_4	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS_4	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS_4	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST_4	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X60 – CLOK PLL CONTROL 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLK_DIFF	R/W	1 : XTI pin to PLL REF clock input is differential input. 0 : XTI pin to PLL REF clock input is non-differential input.	0
6-4	CP_SEL	R/W	Charge-pump current for PLL 0h : 1uA, 1h : 5uA, 2h : 10uA, 3h : 20uA, 4h : 40uA, 5h : 60UA, 6h : 80uA, 7h : 100uA.	2
3-2	LP_X8	R/W	Loop resistor for PLL 0h : 55.7K, 1h : 17.6K, 2h ; 8.81K, 3h : 6.23K	1
1-0	VCO	R/W	Select VCO gain for PLL 0h : 416MHz/V, 1h : 517MHz/V, 2h : 615MHz/V, 3h : 755MHz/V	2

0X61 – VIDEO CLOCK SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PLL_RST	R/W	PLL module Reset#.Test purpose only. 1 : PLL module Reset#, 0 : PLL module is in normal mode.	0
6	PLL_PD	R/W	1 : PLL module is in power down mode. 0 : PLL module is in normal mode.	0
5	PLL_IREF	R/W	PLL Current bias reference	0
4	DECOSC	R/W	Video Decoder system clock select. 0: (PLL output clock)/4 is selected for video decoder process. 1: Video decoder system clock is generated by XTI input crystal clock.	1
3	SEL_144_72	R/W	1 : PLL module output 144MHz clock for D1 video decoder. 0 : PLL module output 72MHz clock.Test purpose only.	1
2	SEL_108_54	R/W	1 : PLL module output 108MHz clock for D1 video decoder. 0 : PLL module output 54MHz clock.Test purpose only.	1
1-0	XTIMD	R/W	XTI pin input clock process control. If XTIMD=0/1/2, Clock PLL Output clock is not used for internal logic process. 0: XTI clock is directly used for all video decoder clock source. 1: XTI/2 clock is used for all video decoder clock source. 2: XTI/4 clock is used for all video decoder clock source. 3: PLL output clock is used for all video decoder clock source when DECOSC=0.	3h

0X62 – 036M

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	036M4	R/W	0 : CH4 video decoder output 27MHz video data. 1 : CH4 video decoder output 36MHz video data.	0
6	036M3	R/W	0 : CH3 video decoder output 27MHz video data. 1 : CH3 video decoder output 36MHz video data.	0
5	036M2	R/W	0 : CH2 video decoder output 27MHz video data. 1 : CH2 video decoder output 36MHz video data.	0
4	036M1	R/W	0 : CH1 video decoder output 27MHz video data. 1 : CH1 video decoder output 36MHz video data.	0
3-0	Reserved	R/W		0h

0X63 – CHANNEL ID 12

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CH2NUM	R/W	Set up Channel ID number in VIN2 video decoder data output.	1h
3-0	CH1NUM	R/W	Set up Channel ID number in VIN2 video decoder data output.	0h

0X64 – CHANNEL ID 34

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CH4NUM	R/W	Set up Channel ID number in VIN4 video decoder data output.	3h
3-0	CH3NUM	R/W	Set up Channel ID number in VIN3 video decoder data output.	2h

0X65 – VIDEO BUS TRI-STATE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4	VD4ORD	R/W	Select the video channel output order on 4xD1 output mode. 0:Ch1->Ch2->Ch3->Ch4->Ch1->Ch2->Ch3->....(increase). 1:Ch4->Ch3->Ch2->Ch1->Ch4->Ch3->Ch2->....(decrease)	0
3	Reserved	R/W		0
2	VDOEB	R/W	VD[7:0] output tri-state control. 1: tri-state output VD[7:0]. 0: normal output VD[7:0].	0
1-0	Reserved	R/W		0

0X67 – HZST

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	HZST	R/W	HZOOM UP process start control.After this number's pixels passed out data process from internal hsync(pksync),Hzoom Up module starts it's zooming up process.	80h

0X6D – D1 NMGAIN/SHCOR

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	NMGAIN 720	R/W	These bits control the normal AGC loop maximum correction value in 720H D1 video decoder.	2h
3-0	SHCOR 720	R/W	These bits provide coring function for the sharpness control in 720H WD1 video decoder.	8h

0X6E – D1 CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP 720	R/W	These bits set the clamping position from the PLL sync edge in 720H D1 video decoder.	38h

0X70 – AUDIO CLOCK CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ACK36MD	R/W	1 : 36MHz clock source is used for audio system clock. Special Test purpose only. 0 : 27MHz clock source is used for audio system clock.	0
6	S2I_8BIT	R/W	0 : ACLKP/ASYNP/ADATP pin input is 16-bit control. 1 : ACLKP/ASYNP/ADATP pin input is 8-bit control.	0
5	ACLKRPOL	R/W	ACLKR input signal polarity inverse. 0 : not inverted. 1 : inverts.	0
4	ACLKPPOL	R/W	ACLKP input signal polarity inverse. 0 : not inverted. 1 : inverted.	0
3	AFAUTO	R/W	ACKI[21:0] control automatic set up with AFMD registers. This mode is only effective when ACLKRMAS _{TER} =1. 0 : ACKI[21:0] registers set up ACKI control. 1 : ACKI control is automatically set up by AFMD register values.	1
2-0	AFMD	R/W	AFAUTO control mode. 0 : 8kHz setting (default). 1 : 16kHz setting. 2 : 32kHz setting. 3 : 44.1kHz setting. 4 : 48kHz setting.	0h

0X71 – DIGITAL AUDIO INPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	I2S8MODE	R/W	8-bit I2S Record output mode. 0 : L/R half length separated output. 1 : One continuous packed output equal to DSP output format.	0
6	MASCKMD	R/W	Audio Clock Master ACLKR output wave format. 0 : High period is one 27MHz clock period.This bit must be 0 when audio cascade is used with more than 32kHz Fs mode. 1 : Almost duty 50-50% clock output on ACLKR pin. If this mode is selected, two times bigger number value need to be set up ACKI registers. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1. SDIV=00h is used with this function normally.	1
5	PBINSWAP	R/W	Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping. 0 : Not swapping. 1 : Swapping.	0
4	ASYNRDLY	R/W	ASYNR input signal delay. 0 : No delay. 1 : Add one 27MHz period delay in ASYNR signal input.	0
3	ASYNPDLY	R/W	ASYNP input signal delay. 0 : No delay. 1 : Add one 36MHz period delay in ASYNP signal input.	0
2	ADATPDLY	R/W	ADATP input data delay by one ACLKP clock. 0 : No delay. This is for I2S type 1T delay input interface. 1 : Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.	0
1-0	INLAWMD	R/W	Select u-Law/A-Law/PCM/SB data input format on ADATP pin. 0 : PCM input 1 : SB(Signed MSB bit in PCM data is inverted) input 2 : u-Law input 3 : A-Law input	0h

0X72 – MIX RATIO VALUE 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	MRATIOMD	R/W	Audio Mixing ratio value divider control 0 : MIX_RATIO 0 0.25 (default) 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1 : MIX_RATIO / 64	0
6	ADACTEST	R/W	0 : must be set up 0 in normal mode. 1 : test purpose only	0
5	AOFFCORE	R/W	0: Audio No-input Noise reduction on(Test purpose only) 1: Audio No-input Noise reduction off	1

0X72 – MIX RATIO VALUE 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4	DAORATIO	R/W	Digital Audio Output Gain is controlled by following. 0: DAOGAIN 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00(default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 1: DAOGAIN / 64	0
3-0	DAOGAIN	R/W	Digital Audio Output Gain. Gain is controlled with DAORATIO mode.	8h

0X73 – A51DET_ENA

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	Reserved	R	Reserved	00h
2	AIN51FORM	R/W	<p>AIN51/52/53/54 record output format selection. This bit is only effective when A51OUTOFF register is set to 0. When AIN1/2/3/4/51 and AIN6/7/8/9/52 are required to be continuous order in record output, 1 is necessary.</p> <p>0: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat4><dat5> <dat6><dat7><dat51>< dat52> R dat : <dat8><dat9><datA><datB><datC><datD> <datE><datF><dat53><dat54></p> <p>If DSP mode(RM_SYNC=1) all data are continuous. <dat0><dat1><dat2><dat3><dat4><dat5><dat6> <dat7><dat8><dat9><datA><datB><datC><datD> <datE><datF><dat51><dat52><dat53><dat54></p> <p>1: If I2S mode(RM_SYNC=0) L dat : <dat0><dat1><dat2><dat3><dat51><dat4> <dat5><dat6><dat7><dat52> R dat : <dat8><dat9><datA><datB><dat53><datC> <datD>< datE>< datF><dat54></p> <p>If DSP mode(RM_SYNC=1) all data continuous. <dat0><dat1><dat2><dat3>< dat51><dat4><dat5> <dat6><dat7><dat52><dat8><dat9><datA><datB> <dat53><datC><datD><datE><datF><dat54></p>	0
1	AINTPOFF	R/W	0 : must be set up 1 : test purpose only	0
0	A51DET_ENA	R/W	<p>Enable state register updating and interrupt request of audio AIN51 (AIN5 input in this chip) detection for each input.</p> <p>0 : Disable state register updating and interrupt request 1 : Enable state register updating and interrupt request</p>	0

0X74 – STATUS OF AUDIO 5 DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-1	Reserved	R		00h
0	A5DET_STATE	R	<p>State of Audio AIN51(AIN5 input in this chip) detection. This bit is activated according ADET_MODE.</p> <p>0 : Inactivated 1 : Activated</p>	0

0X7B – ADATM I2S OUTPUT SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4-0	I2SO_RSEL	R/W	Select R-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h

***Note :**

Both I2SO_RSEL and I2SO_LSEL select output data by following order.

0	Select record audio of channel 1(AIN1)
1	Select record audio of channel 2(AIN2)
2	Select record audio of channel 3(AIN3)
3	Select record audio of channel 4(AIN4)
4	Select record audio of channel 5(AIN5)
5	Select record audio of channel 6(AIN6)
6	Select record audio of channel 7(AIN7)
7	Select record audio of channel 8(AIN8)
8	Select record audio of channel 9(AIN9)
9	Select record audio of channel 10(AIN10)
10(Ah)	Select record audio of channel 11(AIN11)
11(Bh)	Select record audio of channel 12(AIN12)
12(Ch)	Select record audio of channel 13(AIN13)
13(Dh)	Select record audio of channel 14(AIN14)
14(Eh)	Select record audio of channel 15(AIN15)
15(Fh)	Select record audio of channel 16(AIN16)
16(10h)	Select playback audio of the first stage chip(PB1)
17(11h)	Select playback audio of the second stage chip(PB2)
18(12h)	Select playback audio of the third stage chip(PB3)
19(13h)	Select playback audio of the last stage chip(PB4)
20(14h)	Select mixed audio.
21(15h)	Select record audio of channel 51(AIN51)(default)
22(16h)	Select record audio of channel 52(AIN52)
23(17h)	Select record audio of channel 53(AIN53)
24(18h)	Select record audio of channel 54(AIN54)
Others	no audio output.

0X7C – ADATM I2S OUTPUT SELECT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	Reserved	R		0h
4-0	I2SO_LSEL	R/W	Select L-channel output data on ADATM pin when ADATM_I2SOEN=1. *	15h

* Note : Please read 0x7B Note for detail description.

0X7D – AIN51/52/53/54 RECORD OUTPUT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	I2SRECSEL54	R/W	Select output data in bellow dat54 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	3h
5-4	I2SRECSEL53	R/W	Select output data in bellow dat53 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	2h
3-2	I2SRECSEL52	R/W	Select output data in bellow dat52 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	1h
1-0	I2SRECSEL51	R/W	Select output data in bellow dat51 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54.	0

These registers are only effective when A51OUTOFF=0. These registers function change under AIN51FORM control at that time as follows.

When AIN51FORM=0:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat51><dat52>

R data : <dat8><dat9><datA><datB><datC><datD><datE><datF><dat53><dat54>

If DSP mode(RM_SYNC=1), all data are continuous.

<dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat8><dat9><datA><datB><datC>

<datD><datE><datF><dat51><dat52><dat53><dat54>

When AIN51FORM=1:

If I2S mode(RM_SYNC=0),

L data : <dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52>

R data : <dat8><dat9><datA><datB><dat53><datC><datD><datE><datF><dat54>

If DSP mode(RM_SYNC=1), all data are continuous.

<dat0><dat1><dat2><dat3><dat51><dat4><dat5><dat6><dat7><dat52><dat8><dat9>

<datA><datB><dat53><datC><datD><datE><datF><dat54>

All other datN(N=0,1,2,,,,F) are selected by R_SEQ_N registers

0X7E – A5OUTOFF

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	A5OUTOFF	R/W	AIN5 data output control on ADATR record signal. 0: output AIN51/AIN52/AIN53/AIN54 record data on ADATR. 1: not output AIN51/AIN52/AIN53/AIN54 record data on ADATR.	1
6	ADATM_I2SOEN	R/W	Define ADATM pin output 2 word data to make standard I2S output. 0:Mixing Data or Playback Input data are only output on ADATM pin by M_RLSWAP register.(default) 1:L/R data on ADATM pin is selected by I2SO_RSEL / I2SO_LSEL registers.	0
5	MIX_MUTE_A5	R/W	MIX_MUTE_A5: Audio input AIN5 mute function control. 0:Normal 1:Muted	1
4-0	ADET_TH5[4:0]	R/W	AIN5 threshold value for audio detection	03h

0X80 – SOFTWARE RESET CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R	Reserved	00b
5	AUDIORST	W	A 1 written to this bit resets the Audio portion to its default state but all register content remains unchanged. This bit is self-resetting.	0
4	VOUTrST	W	A 1 written to this bit resets Video data mux output logic to its default state but all register content remain unchanged. This bit is self-resetting.	0
3	VDEC4RST	W	A 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
2	VDEC3RST	W	A 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
1	VDEC2RST	W	A 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0
0	VDEC1RST	W	A 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting.	0

0X81 – ANALOG CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	Reserved	R/W		0h
3	CLKPDN	R/W	0 = Normal clock operation. 1 = All 4Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active.	0
2	Reserved	R/W		0
1	YFLEN	R/W	Analog Video CH1/CH2/CH3/CH4 anti-alias filter control 1 = enable 0 = disable	1
0	Reserved	R/W		0

0X82 – ANALOG CONTROL REGISTER2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CTEST	R/W	Clamping control for debugging use.(Test purpose only)	0
6	YCLEN	R/W	1 = Y channel clamp disabled (Test purpose only) 0 = Enabled.	0
5	CKIPOL	R/W	1/4(27MHz or 36MHz) clock output signal rise/fall timing. 0 : change by 1/2(54MHz or 72MHz) clock output falling edge. 1 : change by 1/2(54MHz or 72MHz) clock output rising edge.	0
4	Reserved	R		0
3	GTEST	R/W	1 = Test.(Test purpose only) 0 = Normal operation.	0
2	VLPF	R/W	Clamping filter control.	0
1	CKLY	R/W	Clamping current control 1.	0
0	CKLC	R/W	Clamping current control 2.	0

0X83 – CONTROL REGISTER I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	PBW	R/W	1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW	1
6	DEM	R/W	Reserved	1
5	IDSNS	R/W	Reserved.	0
4	SET7	R/W	1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level.	0
3	COMB	R/W	1 = Adaptive comb filter for NTSC 0 = Notch filter	1
2	HCOMP	R/W	1 = operation mode 1. (recommended) 0 = mode 0.	1
1	YCOMB	R/W	1 = Bypass Comb filter when no burst presence 0 = No bypass	0
0	PDLY	R/W	PAL delay line. 0 = enabled. 1 = disabled.	0

0X84 – COLOR KILLER HYSTERESIS CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	GMEN	R/W	Reserved.	0
6-5	CKHY	R/W	Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow	00b
4-0	HSDLY	RW	Reserved for test.	00h

0X85 – VERTICAL SHARPNESS

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	SHCOR960	R/W	These bits provide coring function for the sharpness control in 960H WD1 video decoder.	3
3-0	Reserved	R/W		0h

0X86 – CORING CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CTCOR	R/W	These bits control the coring for CTI.	1
5-4	CCOR	R/W	These bits control the low level coring function for the Cb/Cr output.	0
3-2	VCOR	R/W	These bits control the coring function of vertical peaking.	1
1-0	CIF	R/W	These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB	0

0X87 – CLAMPING GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLPEND	R/W	These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST.	5
3-0	CLPST	R/W	These 4 bits set the start time of the clamping. It is referenced to PCLAMP position.	0

0X88 – INDIVIDUAL AGC GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	NMGAIN 960	R/W	These bits control the normal AGC loop maximum correction value for 960H WD1 video deocder.	4
3-1	WPGAIN	R/W	Peak AGC loop gain control.	1
0	Reserved	R	Reserved	0

0X89 – AUDIO FS MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ATHROUGH	R/W	0: must be set up in normal mode. 1: test purpose only.	0
6	ASYN SERIAL	R/W	ALINKO/ALINKI bit rate. 0: 27MHz.Effective for all Fs clock mode.This bit muse be 0 when audio cascade is used with more than 32kHz Fs mode. 1: 13.5MHz.Effective for Fs 8kHz/16kHz mode.	0
5	ACLKR128	R/W	ACLKR clock output mode for special 16x8bit(total 128bit) data interface. 0: ACLKR output is normal. 1: the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8-bit mode (special purpose).	0
4	ACLKR64	R/W	ACLKR clock output mode for special 4 word output interface.ACLKRMAS TER=1 mode only. 0: ACLKR output is normal 1: the number of ACLKR clock per fs is 64.	0
3	AFS384	R/W	Special Audio fs Sampling mode. 0: Audio fs Sampling mode is normal 256xfs if AIN5=0. 1: Audio fs Sampling mode is 384xfs mode.	0
2	AIN5MD	R/W	Audio Input process mode. 0: AIN1/AIN2/AIN3/AIN4 4 Audio input only process. This mode is 256xfs if AFS384=0.In this mode, AIN5 input is not processed. 1: AIN1/AIN2/AIN3/AIN4/AIN5 5 Audio input process. This mode is 320xfs Mode if AFS384=0.	0
1-0	Reserved	R		0h

0X8A – WHITE PEAK THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PEAKWT	R/W	These bits control the white peak detection threshold. Setting 'FF' can disable this function.	D8

0X8B– CLAMP LEVEL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLMPLD	R/W	0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d.	1
6-0	CLMPL	R/W	These bits determine the clamping level of the Y channel.	3C

0X8C– SYNC AMPLITUDE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	SYNCTD	R/W	0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h.	1
6-0	SYNCT	R/W	These bits determine the standard sync pulse amplitude for AGC reference.	38

0X8D – SYNC MISS COUNT REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MISSCNT	R/W	These bits set the threshold for horizontal sync miss count threshold.	4
3-0	HSWIN	R/W	These bits determine the VCR mode detection threshold.	4

0X8E – WD1 CLAMP POSITION REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	PCLAMP 960	R/W	These bits set the clamping position from the PLL sync edge in 960H WD1 video decoder.	36h

0X8F – VERTICAL CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	VLCKI	R/W	Vertical lock in time. 0 = fastest 3 = slowest.	0
5-4	VLCKO	R/W	Vertical lock out time. 0 = fastest 3 = slowest.	0
3	VMODE	R/W	This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode.	0
2	DETV	R/W	1 = recommended for special application only. 0 = Normal Vsync logic	0
1	AFLD	R/W	Auto field generation control 0 = Off 1 = On	0
0	VINT	R/W	Vertical integration time control. 1 = short 0 = normal	0

0X90 – VERTICAL CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-5	BSHT	R/W	Burst PLL center frequency control.	0
4-0	VSHT	R/W	Vsync output delay control in the increment of half line length.	00

0X91 – COLOR KILLER LEVEL CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	CKILMAX	R/W	These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value.	1
5-0	CKILMIN	R/W	These bits control the color killer threshold. Larger value gives lower killer level.	38

0X92 – COMB FILTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HTL	R/W	0 = adaptive mode 1 = fixed comb	0
6-4	HTL	R/W	Adaptive Comb filter threshold control 1.	4
3-0	VTL	R/W	Adaptive Comb filter threshold control 2.	4

0X93 – LUMA DELAY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CKLM	R/W	Color Killer mode. 0 = normal 1 = fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides -4 to +3 unit delay control.	3
3	PD_BIAS	R/W	Video ADC PD_BIAS.	0
2-0	VSAVE	R/W	Video ADC power save. 0: Highest power 7: Lowest power 6 is normal value.	0

0X94 – MISCELLANEOUS CONTROL I

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	HPLC	R/W	Reserved for internal use.	0
6	EVCNT	R/W	1 = Even field counter in special mode. 0 = Normal operation	0
5	PALC	R/W	Reserved for future use.	0
4	SDET	R/W	ID detection sensitivity. A '1' is recommended.	1
3	Reserved	R/W		0
2	BYPASS	R/W	It controls the standard detection and should be set to '1' in normal use.	1
1-0	Reserved	R/W		0

0X95 – LOOP CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	HPM	R/W	Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal	2
5-4	ACCT	R/W	ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast	2
3-2	SPM	R/W	Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest	1
1-0	CBW	R/W	Chroma low pass filter bandwidth control. Refer to filter curves.	1

0X96 – MISCELLANEOUS CONTROL II

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	NKILL	R/W	1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled.	1
6	PKILL	R/W	1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled.	1
5	SKILL	R/W	1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled.	1
4	CBAL	R/W	0 = Normal output 1 = special output mode.	0
3	FCS	R/W	1 = Force decoder output value determined by CCS. 0 = Disabled.	0
2	LCS	R/W	1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled.	0
1	CCS	R/W	When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black.	0
0	BST	R/W	1 = Enable blue stretch. 0 = Disabled.	0

0X97 – CLAMP MODE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	FRM	R/W	Free run mode control 0 = Auto, 2 = default to 60Hz, 3 = default to 50Hz	0
5-4	YNR	R/W	Y HF noise reduction 0 = None, 1 = smallest, 2 = small, 3 = medium	0
3-2	CLMD	R/W	Clamping mode control. 0 = Sync top, 1 = Auto, 2 = Pedestal, 3 = N/A	1
1-0	PSP	R/W	Slice level control 0 = low 1 = medium 2 = high	1

0X9C – OVSEND

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	OFDLY	R/W	FIELD output delay. 0h : 0H line delay FIELD output. Internal fld direct output mode. 1h-7h : 1H-7H line delay FIELD output.	2
3-0	Reserved	R/W		0h

0X9E – NOVID

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VDELAYMD	R/W	0 : normal VDELAY mode. 1 : Optional VDELAY mode.	0
6	FC27	R/W	1 : normal ITU-R656 operation 0 : Reserved	1
5-4	CHID_MD	R/W	Select the Channel ID format for time-multiplexed output 0h : No channel ID (default) 1h : CHID with the specific ITU-R BT.656 sync Code 2h : CHID with the specific horizontal blanking code 3h : CHID with the specific ITU-R BT.656 sync & horizontal blanking code	0
3	NOVID_656	R/W	0 : Normal ITU-R BT.656 SA/EAV(default) 1 : AN optional set of ITU-R BT.656 SAV/EAV code for No-video status	0
2	EAVSWAP	R/W	1 : EAV-SAV code is swapped.(special purpose only) 0 : EAV-SAV code is not swapped(standard 656 output mode)	0
1	VIPCFG	R/W	Set up Bit7 in 4th byte of EAV/SAV code. 1 : Standard ITU-R656 code format.(It's also VIP task-A code format.) 0 : Old VIP task-B code format.	1
0	NTSC656	R/W	1 : Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0 : Number of Even Field Video output line is same as the number of Odd field Video output line.	0

0X9F – CLOCK OUTPUT DELAY CONTROL REGISTER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	CLKNO_DEL	R/W	Control the clock delay of CLKNO pin. 0h/1h/3h/7h/Fh values are effective. 0h : no delay. 1h : about 0.26ns more delay, 3h : about 0.52ns more delay, 7h : about 0.77ns more delay, Fh : about 0.96ns more delay	0h
3-0	CLKPO_DEL	R/W	Control the clock delay of CLKPO pin. 0h/1h/3h/7h/Fh values are effective. 0h : no delay. 1h : about 0.26ns more delay, 3h : about 0.52ns more delay, 7h : about 0.77ns more delay, Fh : about 0.96ns more delay	0h

0XAF – VERTICAL PEAKING LEVEL CONTROL 1/2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP2	R/W	Select CH2 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP1	R/W	Select CH1 Video Vertical peaking level. (*) 0 : none. 7 : highest	0

*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.

0XB0 – VERTICAL PEAKING LEVEL CONTROL 3/4

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6-4	VSHP4	R/W	Select CH4 Video Vertical peaking level. (*) 0 : none. 7 : highest	0
3	Reserved	R		0
2-0	VSHP3	R/W	Select CH3 Video Vertical peaking level. (*) 0 : none. 7 : highest	0

*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.

0XB1 – CH8IDEN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CH8IDEN	R/W	<p>Video Channel ID number has following value in Sync Code and Horizontal Blanking Code with CH1NUM, CH2NUM, CH3NUM and CH4NUM.</p> <p>0 : 4 channel ID Only output VIN1 : CH1NUM[3:0] VIN2 : CH2NUM[3:0] VIN3 : CH3NUM[3:0] VIN4 : CH4NUM[3:0]</p> <p>1 : 8 channel ID output VIN1 : {1'b0,CH1NUM[2:0]} VIN2 : {1'b0,CH2NUM[2:0]} VIN3 : {1'b0,CH3NUM[2:0]} VIN4 : {1'b0,CH4NUM[2:0]}</p>	0
6-4	Reserved	R/W		0
3	CLPOE	R/W	0 : normal mode.	0
2-0	TESTVNUM	R/W	Test purpose only.	0

0XB2 – VIDEO ADC CLOCK POLARITY

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	VADC_CKPOL4	R/W	1 : CH4 video ADC clock polarity is inversed. 0 : not inversed.	0
6	VADC_CKPOL3	R/W	1 : CH3 video ADC clock polarity is inversed. 0 : not inversed.	0
5	VADC_CKPOL2	R/W	1 : CH2 video ADC clock polarity is inversed. 0 : not inversed.	0
4	VADC_CKPOL1	R/W	1 : CH1 video ADC clock polarity is inversed. 0 : not inversed.	0
3-0	Reserved	R/W		0h

0XB3 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AADC4OFS[9:8]	R/W	Ch4 Digital ADC input data offset control bit9-8.	0h
5-4	AADC3OFS[9:8]	R/W	Ch3 Digital ADC input data offset control bit9-8.	0h
3-2	AADC2OFS[9:8]	R/W	Ch2 Digital ADC input data offset control bit9-8.	0h
1-0	AADC1OFS[9:8]	R/W	Ch1 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by $ADJAADCn = AUDnADC + AADCnOFS$.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0XB4 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC1OFS[7:0]	R/W	Ch1 Digital ADC input data offset control bit7-0.	00h

0XB5 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC2OFS[7:0]	R/W	Ch2 Digital ADC input data offset control bit7-0.	00h

0XB6 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC3OFS[7:0]	R/W	Ch3 Digital ADC input data offset control bit7-0.	00h

0XB7 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC4OFS[7:0]	R/W	Ch4 Digital ADC input data offset control bit7-0.	00h

0X75 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		0h
1-0	AADC5OFS[9:8]	R/W	Ch5 Digital ADC input data offset control bit9-8.	0h

Digital ADC input data offset control. Digital ADC input data is adjusted by $ADJAADCn = AUDnADC + AADCnOFS$.

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0X76 – AUDIO ADC DIGITAL INPUT OFFSET CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AADC5OFS[7:0]	R/W	Ch5 Digital ADC input data offset control bit7-0.	00h

0XB8 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	AUD4ADC[9:8]	R	Bit9-8 of Ch4 Analog Audio ADC Digital Output Value by 2's format.	X
5-4	AUD3ADC[9:8]	R	Bit9-8 of Ch3 Analog Audio ADC Digital Output Value by 2's format.	X
3-2	AUD2ADC[9:8]	R	Bit9-8 of Ch2 Analog Audio ADC Digital Output Value by 2's format.	X
1-0	AUD1ADC[9:8]	R	Bit9-8 of Ch1 Analog Audio ADC Digital Output Value by 2's format.	X

0XB9 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD1ADC[7:0]	R	Bit7-0 of Ch1 Analog Audio ADC Digital Output Value by 2's format.	X

0XBA – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD2ADC[7:0]	R	Bit7-0 of Ch2 Analog Audio ADC Digital Output Value by 2's format.	X

0XBB – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD3ADC[7:0]	R	Bit7-0 of Ch3 Analog Audio ADC Digital Output Value by 2's format..	X

0XBC – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD4ADC[7:0]	R	Bit7-0 of Ch4 Analog Audio ADC Digital Output Value by 2's format.	X

0X77 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	AUD5ADC[9:8]	R	Bit9-8 of Ch5 Analog Audio ADC Digital Output Value by 2's format.	X

0X78 – ANALOG AUDIO ADC DIGITAL OUTPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AUD5ADC[7:0]	R	Bit7-0 of Ch5 Analog Audio ADC Digital Output Value by 2's format.	X

0XBDB – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	ADJAADC4[9:8]	R	Bit9-8 of Ch4 adjusted Audio ADC Digital Input Data Value by 2's format.	X
5-4	ADJAADC3[9:8]	R	Bit9-8 of Ch3 adjusted Audio ADC Digital Input Data Value by 2's format.	X
3-2	ADJAADC2[9:8]	R	Bit9-8 of Ch2 adjusted Audio ADC Digital Input Data Value by 2's format.	X
1-0	ADJAADC1[9:8]	R	Bit9-8 of Ch1 adjusted Audio ADC Digital Input Data Value by 2's format.	X

The value shows the first input data in front of Digital Audio Decimation Filtering process.

0XBEB – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC1[7:0]	R	Bit7-0 of Ch1 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XBFB – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC2[7:0]	R	Bit7-0 of Ch2 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC0 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC3[7:0]	R	Bit7-0 of Ch3 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0XC1 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC4[7:0]	R	Bit7-0 of Ch4 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X79 – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ADJAADC5[9:8]	R	Bit9-8 of Ch5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

0X7A – ADJUSTED ANALOG AUDIO ADC DIGITAL INPUT VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ADJAADC5[7:0]	R	Bit7-0 of Ch5 adjusted Audio ADC Digital Input Data Value by 2's format.	X

OXCA – VIDEO CHANNEL OUTPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R/W		0h
5-4	CHMD	R/W	Select video bus output mode on 8bit VD[7:0] pin. 0 : Single Channel ITU-R BT.656 format output. 1 : Two Channel ITU-R BT.656 Time-multiplexed format output. 2 : Four Channel ITU-R BT.656 Time-multiplexed format output.	0h
3-0	Reserved	R/W		0h

OXCC – 2ND CHANNEL SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R/W		0h
5-4	SELCH	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD pin 0 : CH1 video output 1 : CH2 video output 2 : CH3 video output 3 : CH4 video output	3h
3-0	Reserved	R/W		5h

OXCD – 1ST CHANNEL SELECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R/W		3h
5-4	MAINCH	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD pin 0 : CH1 video output 1 : CH2 video output 2 : CH3 video output 3 : CH4 video output	2h
3-0	Reserved	R/W		4h

0XCE – ANALOG POWER DOWN CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AAUTOMUTE	R/W	1 : When input Analog data is less than ADET_TH level, output PCM data will be 0x0000(0x00).Audio DAC data input is 0x200. 0 : No effect	0
6	Reserved	R/W		0
5	A_DAC_PWDN	R/W	Power down the audio DAC. 0 : Normal operation 1 : Power down	0
4	A_ADC_PWDN	R/W	Power down the audio ADC. 0 : Normal operation 1 : Power down	0
3-0	VADC_PWDN	R/W	Power down the video ADC. V_ADC_PWDN[3:0] stands for CH4 to CH1. 0 : Normal operation 1 : Power down	0h

0XCF – SERIAL MODE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	SMD	R/W	Set up cascade Audio Serial mode. When SMD=2hex or 3hex, ALINKO pin output cascaded audio serial data. When SMD=0hex, ALINKO pin output is tri-state. 00 : No Serial mode. ALINKO pin is tri-state output. 10 : ALINKO pin is Serial out pin. ALINKI pin is Serial input pin.	0h
5-0	Reserved	R/W		0h

0XD0, 0XD1, 0X7F - ANALOG AUDIO INPUT GAIN

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD0	7-4	AIGAIN2	R/W	Select the amplifier's gain for each analog audio input AIN1/2/3/4/5. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	6h
0xD1		AIGAIN4	R/W		
0x7F		AIGAIN5	R/W		
0xD0	3-0	AIGAIN1	R/W		6h
0xD1		AIGAIN3	R/W		
0x7F		MIXRATIO5	R/W	Audio input AIN5 ratio value for audio mixing	0h

OXD2 – NUMBER OF AUDIO TO BE RECORDED

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	M_RLSWAP	R/W	<p>Define the sequence of mixing and playback audio data on the ADATM pin.</p> <p>If RM_SYNC=0 : I2S format,</p> <p>0 : Mixing audio on position 0 and playback audio on position 8 1 : Playback audio on position 0 and mixing audio on position 8</p> <p>If RM_SYNC=1 : DSP format,</p> <p>0 : Mixing audio on position 0 and playback audio on position 1 1 : Playback audio on position 0 and mixing audio on position 1</p>	0
6	RM_SYNC	R/W	<p>Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin.</p> <p>0 : I2S format 1 : DSP format</p>	0
5-4	RM_PBSEL	R/W	<p>Select the output PlayBackIn data for the ADATM pin.</p> <p>0 First Stage PalyBackIn audio 1 Second Stage PalyBackIn audio 2 Third Stage PalyBackIn audio 3 Last Stage PalyBackIn audio</p>	0h
3-2	R_ADATM	R/W	<p>Select the output mode for the ADATM pin.</p> <p>0 : Digital serial data of mixing audio 1 : Digital serial data of ADATR format record audio 2 : Digital serial data of ADATM format record audio</p>	0h
1-0	R_MULTCH	R/W	<p>Define the number of audio for record on the ADATR pin.</p> <p>0 2 audios 1 4 audios 2 8 audios 3 16 audios</p> <p>Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. In addition, each output position data are selected by R_SEQ_0/R_SEQ_1/.../R_SEQ_F registers.</p>	0h

0XD3, 0XD4, 0XD5, 0XD6, 0XD7, 0XD8, 0XD9, 0XDA – SEQUENCE OF AUDIO TO BE RECORDED

INDEX	BIT	FUNCTION	R/W	DESCRIPTION	RESET
0xD3	7-4	R_SEQ1	R/W	Define the sequence of record audio on the ADATR pin. Refer to Figure 10 and Table 7 for the detail of the R_SEQ_0 ~ R_SEQ_F. The default value of R_SEQ_0 is "0", R_SEQ_1 is "1", and R_SEQ_F is "F". 0 AIN1 1 AIN2 2 AIN3 : : : : 14 AIN15 15 AIN16	1h
	3-0	R_SEQ0	R/W		0h
0xD4	7-4	R_SEQ3	R/W		3h
	3-0	R_SEQ2	R/W		2h
0xD5	7-4	R_SEQ5	R/W		5h
	3-0	R_SEQ4	R/W		4h
0xD6	7-4	R_SEQ7	R/W		7h
	3-0	R_SEQ6	R/W		6h
0xD7	7-4	R_SEQ9	R/W		9h
	3-0	R_SEQ8	R/W		8h
0xD8	7-4	R_SEQB	R/W		Bh
	3-0	R_SEQA	R/W		Ah
0xD9	7-4	R_SEQD	R/W		Dh
	3-0	R_SEQC	R/W		Ch
0xDA	7-4	R_SEQF	R/W		Fh
	3-0	R_SEQE	R/W		Eh

0XDB –MASTER CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	ADACEN	R/W	Audio DAC Function mode 0 : Audio DAC function disable(test purpose only) 1 : Audio DAC function enable	1
6	AADCEN	R/W	Audio ADC Function mode 0 : Audio ADC function disable(test purpose only) 1 : Audio ADC function enable	1
5	PB_MASTER	R/W	Define the operation mode of the ACLKP and ASYNP pin for playback. 0 : All type I2S/DSP Slave mode(ACLKP and ASYNP is input) 1 : TW2984 type I2S/DSP Master mode (ACLKP and ASYNP is output)	0
4	PB_LRSEL	R/W	Select audio data to be used for playback input. If PB_SYNC=0 I2S format, 0 : 1st Left channel audio data(default), 1 : 1st Right channel audio data. If PB_SYNC=1 DSP format, 0 : 1st input audio data. 1 : 2nd input audio data	0
3	PB_SYNC	R/W	Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin. 0 : I2S format 1 : DSP format	0
2	RM_8BIT	R/W	Define output data format per one word unit on ADATR pin. 0 : 16bit one word unit output 1 : 8bit one word unit packed output	0
1	ASYNROEN	R/W	Define input/output mode on the ASYNR pin. 1 : ASYNR pin is input 0 : ASYNR pin is output	1
0	ACLKRMASER	R/W	Define input/output mode on the ACLKR pin and set up audio system processing. 0 : ACLKR pin is input. External 256xfs or 320fs or 384xfs clock should be connected to ACLKR pin by AIN5MD/AFS384 setting. 1 : ACLKR pin is output. Internal ACKG generates audio system clock.	0

0XDC – U-LAW/A-LAW OUTPUT AND MIX MUTE CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	LAWMD	R/W	Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin. 0 : PCM output 1 : SB(Signed MSB bit in PCM data is inverted) output 2 : u-Law output 3 : A-Law output	0
5	MIX_DERATIO	R/W	Disable the mixing ratio value for all audio. 0 : Apply individual mixing ratio value for each audio 1 : Apply nominal value for all audio commonly	0
4-0	MIX_MUTE	R/W	Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0] : Audio input AIN1. MIX_MUTE[1] : Audio input AIN2. MIX_MUTE[2] : Audio input AIN3. MIX_MUTE[3] : Audio input AIN4. MIX_MUTE[4] : Playback audio input. 0 : Normal 1 : Muted.	10h

0XDD – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO2	R/W	Audio input AIN2 ratio value for audio mixing	0
3-0	MIX_RATIO1	R/W	Audio input AIN1 ratio value for audio mixing	0

0XDE – MIX RATIO VALUE

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	MIX_RATIO4	R/W	Audio input AIN4 ratio value for audio mixing	0
3-0	MIX_RATIO3	R/W	Audio input AIN3 ratio value for audio mixing	0

0XDF – ANALOG AUDIO OUTPUT GAIN

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	AOGAIN	R/W	Define the amplifier gain for analog audio output. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75	8h
3-0	MIX_RATIOP	R/W	Playback audio input ratio value for audio mixing.	0h

0XE0 – MIX OUTPUT SELECTION 1

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R		0
6	AADCCKPOL	R/W	1 : Analog Audio ADC input clock polarity inverse 0 : not inverse.	0
5	ADACCKPOL	R/W	1 : Analog Audio DAC input clock polarity inverse at digital portion. 0 : not inverse.	0

OXE0 – MIX OUTPUT SELECTION 2

BIT	FUNCTION	R/W	DESCRIPTION	RESET
4-0	MIX_OUTSEL	R/W	Define the final audio output for analog and digital mixing out. 0 Select record audio of channel 1 1 Select record audio of channel 2 2 Select record audio of channel 3 3 Select record audio of channel 4 4 Select record audio of channel 5 5 Select record audio of channel 6 6 Select record audio of channel 7 7 Select record audio of channel 8 8 Select record audio of channel 9 9 Select record audio of channel 10 10(Ah) Select record audio of channel 11 11(Bh) Select record audio of channel 12 12(Ch) Select record audio of channel 13 13(Dh) Select record audio of channel 14 14(Eh) Select record audio of channel 15 15(Fh) Select record audio of channel 16 16(10h) Select playback audio of the first stage chip PB1 17(11h) Select playback audio of the first stage chip PB2 18(12h) Select playback audio of the last stage chip PB3 19(13h) Select playback audio of the first stage chip PB4 20(14h) Select mixed audio 21(15h) Select record audio of channel AIN51 22(16h) Select record audio of channel AIN52 23(17h) Select record audio of channel AIN53 24(18h) Select record audio of channel AIN54 Others no sound. Default 1Fh.	1Fh

OXE1 – AUDIO DETECTION PERIOD AND AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	AAMPMD	R/W	Define the audio detection method. 0 : Detect audio if absolute amplitude is greater than threshold(Test purpose only) 1 : Detect audio if differential amplitude is greater than threshold(recommended)	1
6-4	ADET_FILT	R/W	Select the filter for audio detection 0 : Wide LPF. 7 : Narrow LPF	7
3	ADET_TH4[4]*	R/W	MSB bit of AIN4 threshold value for audio detection.	0
2	ADET_TH3[4]*	R/W	MSB bit of AIN3 threshold value for audio detection.	0
1	ADET_TH2[4]*	R/W	MSB bit of AIN2 threshold value for audio detection.	0
0	ADET_TH1[4]*	R/W	MSB bit of AIN1 threshold value for audio detection.	0

* Note:

ADET_TH :Define the threshold value for audio detection.

ADET_TH1: Audio input AIN1.

ADET_TH2: Audio input AIN2.

ADET_TH3: Audio input AIN3.

ADET_TH4: Audio input AIN4.

ADET_TH5: Audio input AIN5.

0:Low value (default)

. .

31:High value

0XE2 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH2[3:0]	R/W	Bit3-0 of AIN2 threshold value for audio detection.	3h
3-0	ADET_TH1[3:0]	R/W	Bit3-0 of AIN1 threshold value for audio detection.	3h

0XE3 – AUDIO DETECTION THRESHOLD

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-4	ADET_TH4[3:0]	R/W	Bit3-0 of AIN4 threshold value for audio detection.	3h
3-0	ADET_TH3[3:0]	R/W	Bit3-0 of AIN3 threshold value for audio detection.	3h

AUDIO CLOCK INCREMENT**0XF0 – AUDIO CLOCK INCREMENT**

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKI[7:0]	R/W	ACKI[7:0], these bits control ACKI Clock Increment in ACKG block.	23h

0XF1 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKI[15:8]	R/W	ACKI[15:8], these bits control ACKI Clock Increment in ACKG block.	48h

0XF2 – AUDIO CLOCK INCREMENT

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0h
5-0	ACKI[21:16]	R/W	ACKI[21:16], these bits control ACKI Clock Increment in ACKG block.	07h

0XF3 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKN[7:0]	R/W	Reserved.	00h

0XF4 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	ACKN[15:8]	R/W	Reserved.	01h

0XF5 – AUDIO CLOCK NUMBER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-2	Reserved	R		00h
1-0	ACKN[17:16]	R/W	Reserved.	0h

0XF6 – SERIAL CLOCK DIVIDER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5-0	SDIV	R/W	These bits control SDIV Serial Clock Divider in ACKG block.	00h

0XF7 – LEFT/RIGHT CLOCK DIVIDER

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	Reserved	R		0
5-0	LRDIV	R/W	Reserved.	20h

0XF8 – AUDIO CLOCK CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	APZ	R/W	These bits control Loop in ACKG block.	1
6-4	APG	R/W	These bits control Loop in ACKG block.	4h
3	Reserved	R/W		0
2	ACPL	R/W	These bits control Loop closed/open in ACKG block. 0: Loop closed(special purpose only) 1 :Loop open(normal function mode)	1
1	SRPH	R/W	Reserved.	0
0	LRPH	R/W	Reserved.	0

0XF9 – VIDEO MISCELLANEOUS FUNCTION CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	LIM16	R/W	0 : Output ranges are limited to 2~254 1 : Output ranges are limited to 16~235 for Y and 16~239 for CbCr	0
6	PBREFEN	R/W	Audio ACKG Reference (refin) input select for test purpose. When ACPL=1, this function is no effect. 0 : ACKG has video VRST refin input selected by VRSTSEL register 1 : ACKG has audio ASYNP refin input	1
5	YBCR422	R/W	Control YCbCr 4:2:2 output mode 0 : Normal 4:2:2 output mode 1 : Averaging 4:2:2 output mode	0
4	Reserved	R/W		0
3	VBI_FRAM	R/W	Test purpose only.	0
2	CNTL656	R/W	Select invalid data value. 0 : 0x80 and 0x10 code will be output as invalid data during active video line. 1 : 0x00 code will be output as invalid data during active video line.	0
1	CLKNF	R/W	CLKNO pin output mode. 0 : output one of 27MHz/54MHz/108MHz. 1 : output one of 36MHz/72MHz/144MHz.	0
0	CLKPF	R/W	CLKPO pin output mode. 0 : output one of 27MHz/54MHz/108MHz. 1 : output one of 36MHz/72MHz/144MHz.	0

OXFA – OUTPUT ENABLE CONTROL AND CLOCK OUTPUT CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	Reserved	R/W		0
6	OE	R/W	Control the tri-state of output pin 0 : Outputs are Tri-state except clock output (CLKPO, CLKNO) pin 1 : Outputs are enabled	0
5	CLKNO_OEB	R/W	Control the tri-state of CLKNO pin 0 : Output is enabled (default) 1 : Output is Tri-state	0
4	CLKPO_OEB	R/W	Control the tri-state of CLKPO pin 0 : Output is enabled 1 : Output is Tri-state	0
3-2	CLKNO_MD	R/W	Control the clock frequency of CLKNO pin 0 : 27MHz or 36MHz clock output 1 : 54MHz or 72MHz clock output 2 : 108MHz or 144MHz clock output 3 : always 0 value	0h
1-0	CLKPO_MD	R/W	Control the clock frequency of CLKPO pin 0 : 27MHz or 36MHz clock output 1 : 54MHz or 72MHz clock output 2 : 108MHz or 144MHz clock output 3 : always 0 value	0h

0XFB – CLOCK POLARITY CONTROL

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7	CLKNO_POL	R/W	Polarity inverse control on output CLKNO signal just before CLKNO pin. 0 : Not inverted. 1 : Polarity inverse.	0
6	CLKPO_POL	R/W	Polarity inverse control on output CLKPO signal just before CLKPO pin. 0 : Not inverted. 1 : Polarity inverse.	0
5	IRQENA	R/W	Enable/Disable the interrupt request through the IRQ pin. 0 : Disable 1 : Enable	0
4	IRQPOL	R/W	Select the polarity of interrupt request through the IRQ pin. 0 : Falling edge requests the interrupt and keeps its state until cleared 1 : Rising edge requests the interrupt and keeps its state until cleared	0
3-2	ADET_MODE	R/W	Define the polarity of state register and interrupt request for audio detection. 0 : No interrupt request by the audio detection 1 : Make the interrupt request rising only when the audio signal comes in 2 : Make the interrupt request falling only when the audio signal goes out 3 : Make the interrupt request rising and falling when the audio comes in and goes out	3
1-0	VDET_MODE	R/W	Define the polarity of state register and interrupt request for video detection. 0 : No interrupt request by the video detection 1 : Make the interrupt request rising only when the video signal comes in 2 : Make the interrupt request falling only when the video signal goes out 3 : Make the interrupt request rising and falling when the video comes in and goes out	3

0XFC – ENABLE VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET_ENA	R/W	<p>Enable state register updating and interrupt request of video and audio detection for each input.</p> <p>[0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4.</p> <p>0 : Disable state register updating and interrupt request 1 : Enable state register updating and interrupt request</p>	FFh

0XFD – STATUS OF VIDEO AND AUDIO DETECTION

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-0	AVDET_STATE	R/W	<p>State of Video and Audio detection.</p> <p>These bits are activated according VDET_MODE and ADET_MODE.</p> <p>[0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4.</p> <p>0 Inactivated 1 Activated</p>	00h

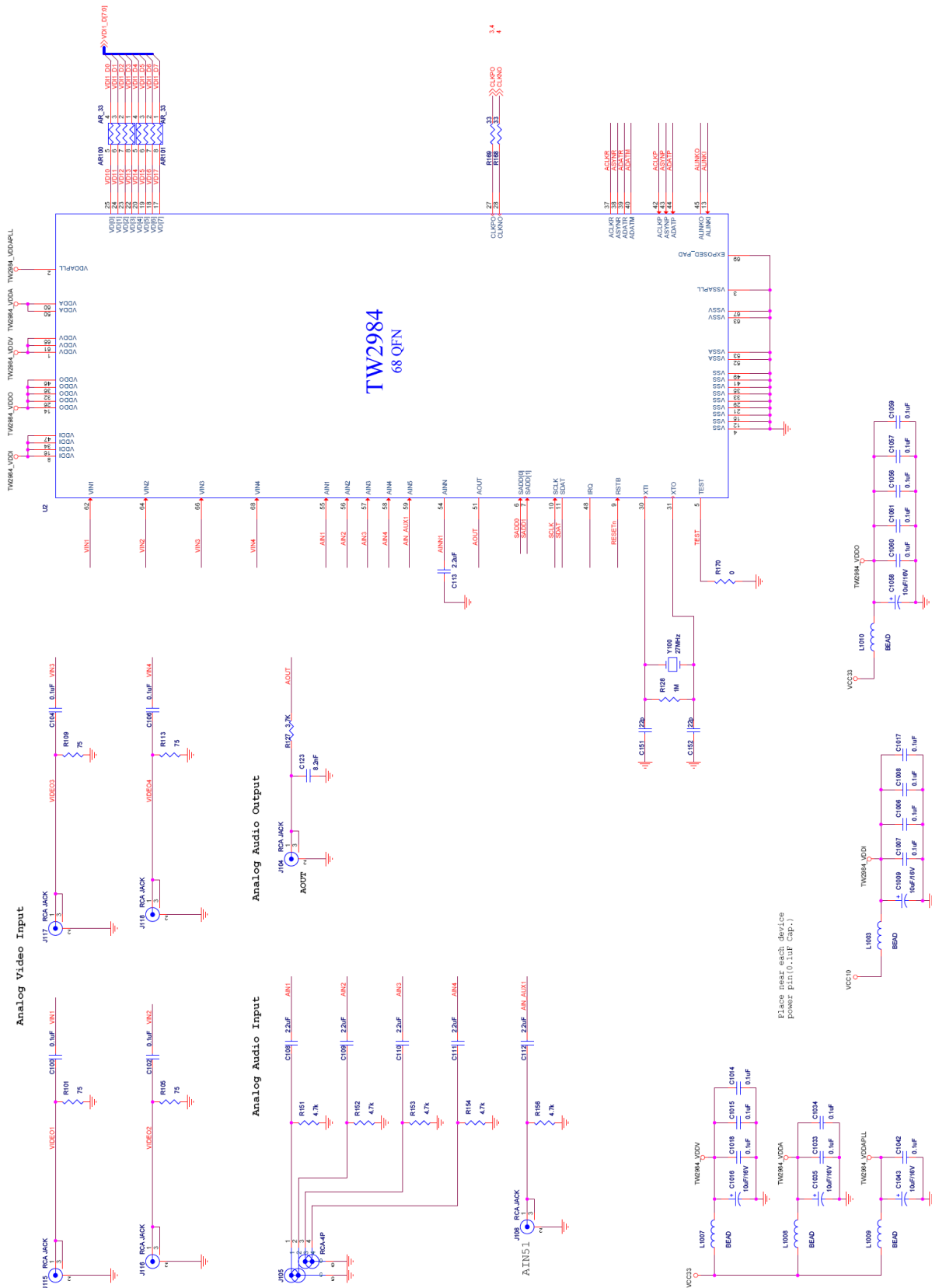
0XFE – DEVICE ID AND REVISION ID FLAG

BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-6	DEV_ID[6:5]	R	Bit6-5 of Device ID. Together with 0xFF[7:3] indicate TW2984 product ID code. DEV_ID=7'h1D	0
5-3	Reserved	R		0
2-0	TEST	R/W	Test purpose only. This must be 0 in normal mode.	0

0XFF – DEVICE ID AND REVISION ID FLAG

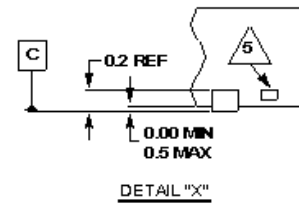
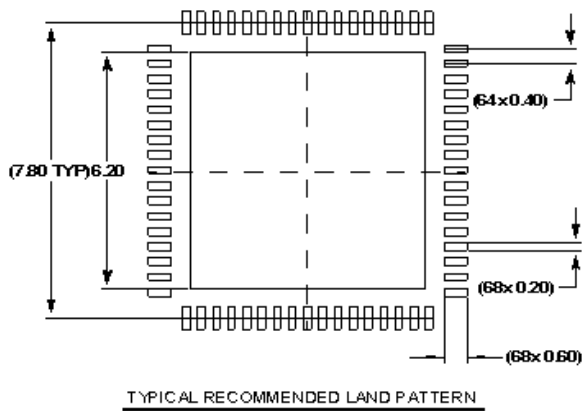
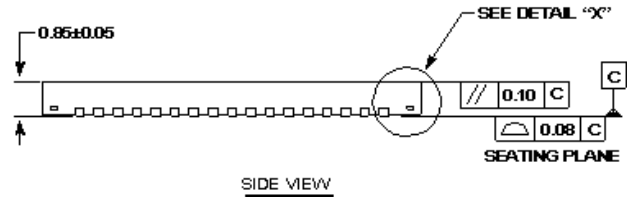
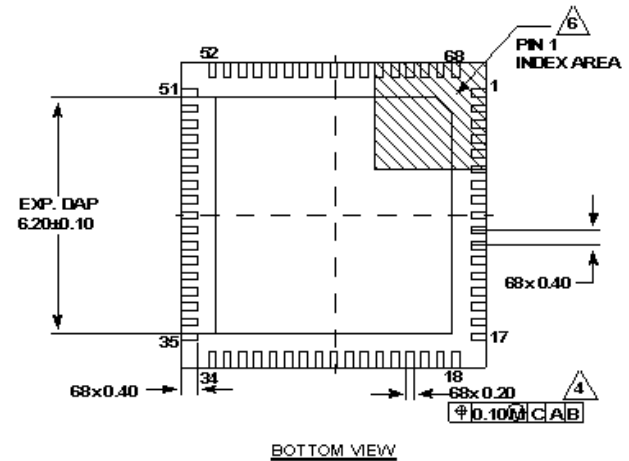
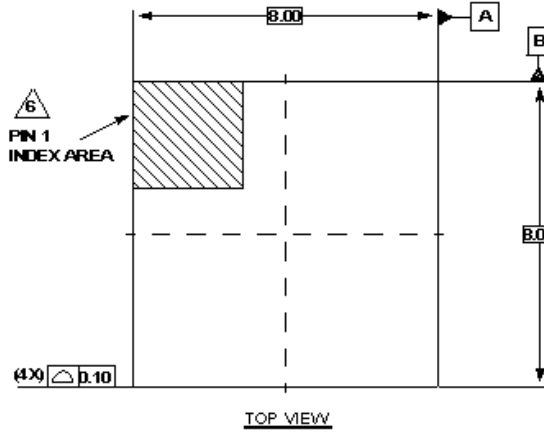
BIT	FUNCTION	R/W	DESCRIPTION	RESET
7-3	DEV_ID[4:0]	R	Bit4-0 of Device ID.	1Dh
0	REV_ID	R	The revision number.	0h

Application Schematic



Package Outline Drawing

L68.8x8B
68 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
 Rev 0, 05/13



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

Revision History

DATE	REVISION	CHANGE
September 24, 2013	FN8583.0	Initial release.

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