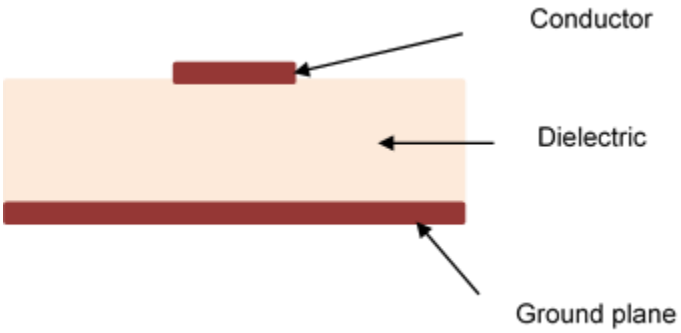
Introduction

This application note discusses the effects of using different transmission line structures to minimize crosstalk. As higher data rate and lower phase noise are required, electromagnetic interference (EMI) on PCBs becomes more significant.

On PCBs that use IDT Timing Devices, there can be multiple adjacent clock traces that have different frequencies. Without proper layout guidelines, current flowing down one trace (aggressor), can induce current on the other (victim), to cause unwanted coupling (crosstalk).

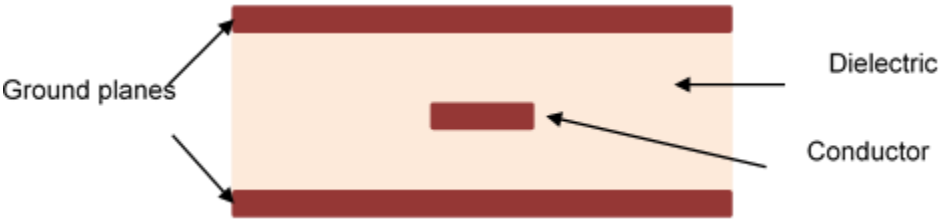
Microstrip and Stripline

Figure 1. Microstrip



Microstrip is a planar transmission line, consisting of a conducting layer and a ground plane separated by dielectric. As there is no dielectric above the conducting layer, this structure is usually used at the top or bottom of the PCB.

Figure 2. Stripline



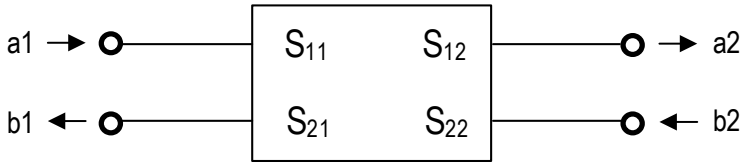
Stripline is another planar transmission line, consisting of a conducting layer and a pair of ground planes separated by dielectric.

Comparison

Due to its structure, microstrip is usually easier and less expensive to manufacture than stripline. On the other hand, compared to microstrip, stripline is better isolated due to shielding ground planes on both sides. Of the same characteristic impedance, stripline has a shorter trace width than microstrip, allowing for more densely packed traces.

S-Parameters

Figure 3. S-Parameters: Two-Port Network



S_{11} and S_{22} are the reflection coefficient, meaning the response at port 1 due to a signal at port 1 and the response at port 2 due to a signal at port 2. S_{12} and S_{21} are the transmission coefficient, meaning the response at port 1 due to a signal at port 2 and vice versa.

Experiment Methodology

The experiment consists of two evaluation boards that share the same design except for signal trace routing. Board 1 uses striplines for signal traces while Board 2 uses microstrips. Two traces with the “worst-case” crosstalk are assessed on both boards. The traces are disconnected from the clock generator IC and terminated with a 50Ω SMD resistor. After termination, s-parameters of the traces are recorded using a network analyzer for analysis.

Theoretical Approximation

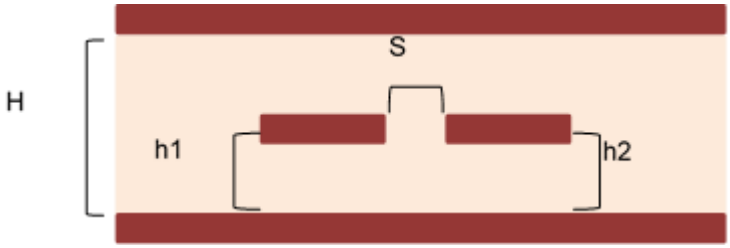
Given the board layouts, expected crosstalk for each board is evaluated.

Table 1. Transmission Line Characteristics

	Microstrip	Stripline
H: Substrate Thickness[mil]	6	12
h1: Stripline Trace 1 Height[mil]	-	6
h2: Stripline Trace 2 Height[mil]	-	6
S: Trace-Trace Separation[mil]	308	
L: Length of Trace[mil]	150	
Copper Thickness[mil]	1.4	
ε_r: Substrate Dielectric Constant	3.7	
T_R: Rise Time[s]	7E-9	

[a] Length of Trace is the distance along trace where Trace-Trace Separation is the shortest.

Figure 4. Trace Height and Spacing Separation



H: Substrate Thickness [mil]

h1: Stripline Trace 1 Height [mil]

h1: Stripline Trace 1 Height [mil]

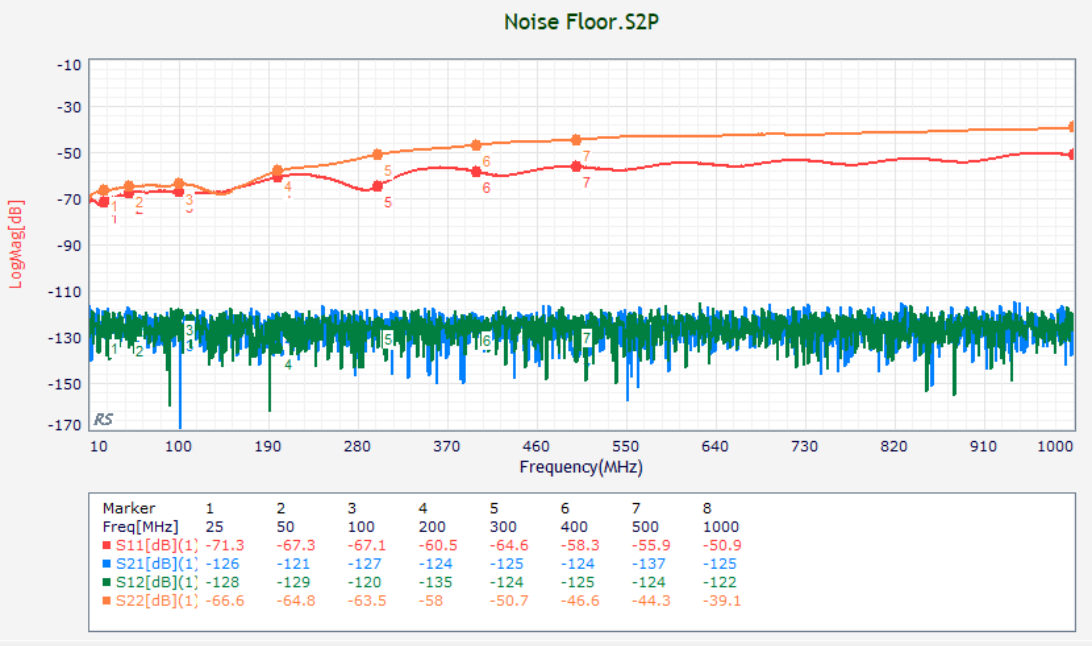
S: Trace-Trace Separation [mil]

Table 2. Transmission Line Characteristics

	Microstrip	Stripline
C_{RT}: Propagation Delay - Rise Time Ratio	$C_{RT} = \frac{2 \cdot 1.017\sqrt{\varepsilon_r \cdot 0.475 + 0.67} \cdot L \cdot 10^{-12}}{T_R}$	
XT: Crosstalk in dB	If $C_{RT} \leq 1$ $XT = 20\log\left(\frac{1}{1+\left(\frac{S}{H}\right)^2} \cdot C_{RT}\right)$ else $XT = 20\log\left(\frac{1}{1+\left(\frac{S}{H}\right)^2}\right)$	$S_{eff} = \sqrt{S^2+(h_2-h_1)^2}$ $h1_{eff} = \frac{h1*(H-h1)}{h1+(H-h1)}$ $h2_{eff} = \frac{h2*(H-h2)}{h2+(H-h2)}$ If $C_{RT} \leq 1$ $XT = 20\log\left(\frac{1}{1+\left(\frac{S_{eff}^2}{h1_{eff} \cdot h2_{eff}}\right)} \cdot C_{RT}\right)$ else $XT = 20\log\left(\frac{1}{1+\left(\frac{S_{eff}^2}{h1_{eff} \cdot h2_{eff}}\right)}\right)$
Result (Substitute values from table)	XT = -91.8dB RMS Phase Jitter = 115.7fs	XT = -103.8dB RMS Phase Jitter = 29.1fs

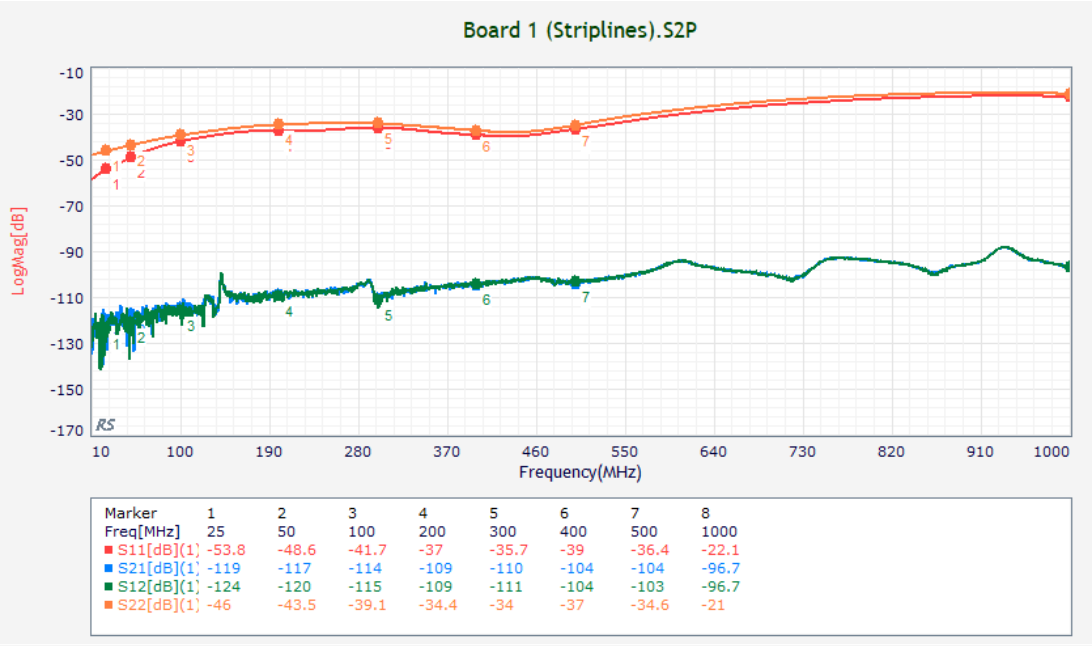
Measurements

Figure 5. Noise Floor of the Measurement System (No Boards Connected)



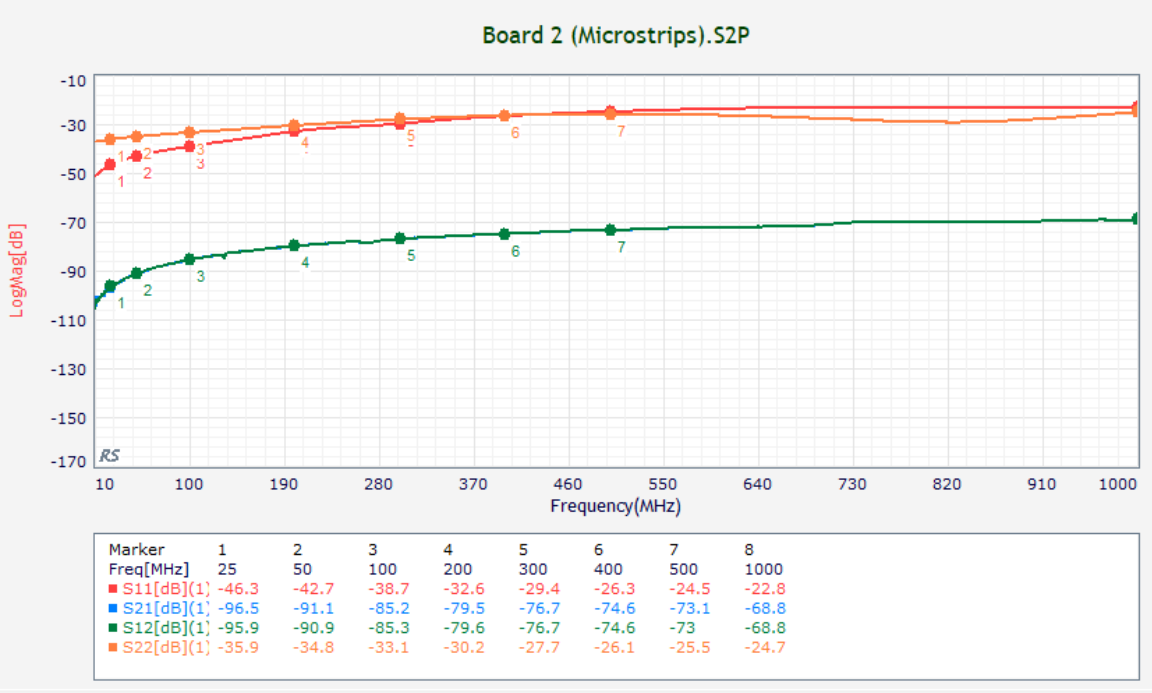
Marker	1	2	3	4	5	6	7	8
Freq[MHz]	25	50	100	200	300	400	500	1000
S11[dB](1)	-71.3	-67.3	-67.1	-60.5	-64.6	-58.3	-55.9	-50.9
S21[dB](1)	-126	-121	-127	-124	-125	-124	-137	-125
S12[dB](1)	-128	-129	-120	-135	-124	-125	-124	-122
S22[dB](1)	-66.6	-64.8	-63.5	-58	-50.7	-46.6	-44.3	-39.1

Figure 6. Board 1 (Striplines)



Marker	1	2	3	4	5	6	7	8
Freq[MHz]	25	50	100	200	300	400	500	1000
S11[dB](1)	-53.8	-48.6	-41.7	-37	-35.7	-39	-36.4	-22.1
S21[dB](1)	-119	-117	-114	-109	-110	-104	-104	-96.7
S12[dB](1)	-124	-120	-115	-109	-111	-104	-103	-96.7
S22[dB](1)	-46	-43.5	-39.1	-34.4	-34	-37	-34.6	-21

Figure 7. Board 2 (Microstrips)



While there are some variations in the reflection coefficients when comparing Board 1 and Board 2, these variations are not significant enough to have a notable effect on the transmission coefficients.

Table 3. Comparison of Board 1 and Board 2

	25M	50M	100M	200M	300M	400M	500M	1000M
Stripline S_{12}[dB],S_{21}[dB]	-124,-119	-120,-117	-115,-114	-109,-109	-111,-110	-104,-104	-103,-104	-97,-97
Microstrip S_{12}[dB],S_{21}[dB]	-96,-97	-91,-91	-85,-85	-80,-80	-77,-77	-75,-75	-73,-73	-69,-69
Difference[dB]	-28,-22	-29,-26	-30,-29	-29,-29	-34,-33	-29,-29	-39,-31	-28,-28
RMS Phase Jitter Improvement[fs]	**143, 127**	**127, 127**	**127, 126**	**112, 112**	**106, 106**	**100, 100**	**101, 101**	**80, 80**

[a] RMS phase jitter improvement when using striplines over microstrips

Rise time of 7ns can be approximated to 50MHz in frequency domain1. The theoretical crosstalk values are comparable to the measurement crosstalk values at 50MHz.

S12 and S21 of Board 1 are lower than those of Board 2 by anywhere from ~20dB all the way to ~40dB. The spurs at these particular frequency points can be interpreted in RMS Jitter2. It is clear that Board 1, with stripline signal routing, produces less crosstalk than Board 2, with microstrip signal routing, resulting in improvement of RMS jitter. For example, with two clocks close to 100MHz in adjacent microstrip traces, one clock can cause a -85dBc spur at the other clock, equivalent to 127fs jitter contribution. Changing to stripline, lowers the spur to -115dBc and the RMS jitter contribution to only 4fs.

Conclusion

Both the theory and measurements convey that crosstalk can be reduced using striplines over microstrips. For applications that use IDT Timing Devices with below 1ps RMS phase jitter requirement, it is recommended to use striplines for any signal traces. For applications with above 1ps RMS phase jitter requirement, use of striplines for signal traces should be considered but not necessarily prioritized.

Appendix

Rise Time to Bandwidth Conversion

$$BW = \frac{.35}{T_R}$$

TR: 10-90% rise time of a square wave in s

BW: bandwidth of the signal in Hz

Spur to Jitter Conversion2

$$J = \frac{10^{\frac{P}{20}}}{\pi \cdot \sqrt{2} \cdot f_c}$$

J: RMS phase jitter in s

fc: carrier frequency in Hz

P: spur amplitude in dBc

RMS Jitter Improvement

$$J_{improv} = \sqrt{J_{micro}^{2} - J_{strip}^{2}}$$

J_{improv}: RMS phase jitter improvement in s

J_{micro}: RMS phase jitter of microstrip in s

J_{strip}: RMS phase jitter of stripline in s

Theoretical Approximation Calculation

	Microstrip	Stripline
Bandwidth	$BW = \frac{.35}{7 \cdot 10^{-9}} = 50MHz$	
C_{RT}	$C_{RT} = \frac{2.1.017\sqrt{3.7 \cdot 0.475 + 0.67} \cdot 150 \cdot 10^{-12}}{7 \cdot 10^{-9}} = 0.0679$	
Crosstalk RMS Phase Jitter	$XT = 20\log(\frac{1}{1+(\frac{308}{6})^2} \cdot 0.0679) = -91.8dB$ $J[fs] = \frac{10^{\frac{-91.8}{20}}}{\pi \cdot \sqrt{2} \cdot 50 \cdot 10^6]} = 115.7fs$	$S_{eff} = \sqrt{308^2 + (6-6)^2} = 308mil$ $h1_{eff} = \frac{6*(12-6)}{6+(12-6)} = 3mil$ $h2_{eff} = \frac{6*(12-6)}{6+(12-6)} = 3mil$ $XT = 20\log(\frac{1}{1+(\frac{308^2}{6 \cdot 6})} \cdot 0.0679) = -103.8dB$ $J[fs] = \frac{10^9 \cdot 10^{\frac{-103.8}{20}}}{\pi \cdot \sqrt{2} \cdot 50]} = -29.1dB$
Result	XT = -91.8dB RMS Phase Jitter = 115.7fs	XT = -103.8dB RMS Phase Jitter = 29.1fs

Revision History

Revision Date	Description of Change
November 1, 2018	Updated to latest IDT style guidelines. Completed minor changes throughout.
September 5, 2018	Initial release.

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