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Introduction

Slave SPI can provide data conversion, and transfer data from one device to others. Also, when parallel ports are just not feasible, a single serial port gets used. This serial signal can be converted to parallel information by the SLG46620 IC. Please note that the maximum number of bits which can be converted is 8 at a time.

SPI converter circuit design

As shown in Figure 1, using two main blocks (SPI block and SPI Parallel Output block), it is possible to perform this conversion.

In this example, SPI serial data is input at Pin 10. nCSB is input at Pin 5, and SCLK is input at Pin 7. The converted SPI Parallel Out signals can then go directly to output pins, or sent to other on-chip blocks (SPI parallel output option should be enabled). In this example they are connected to PINs 13 to 20.

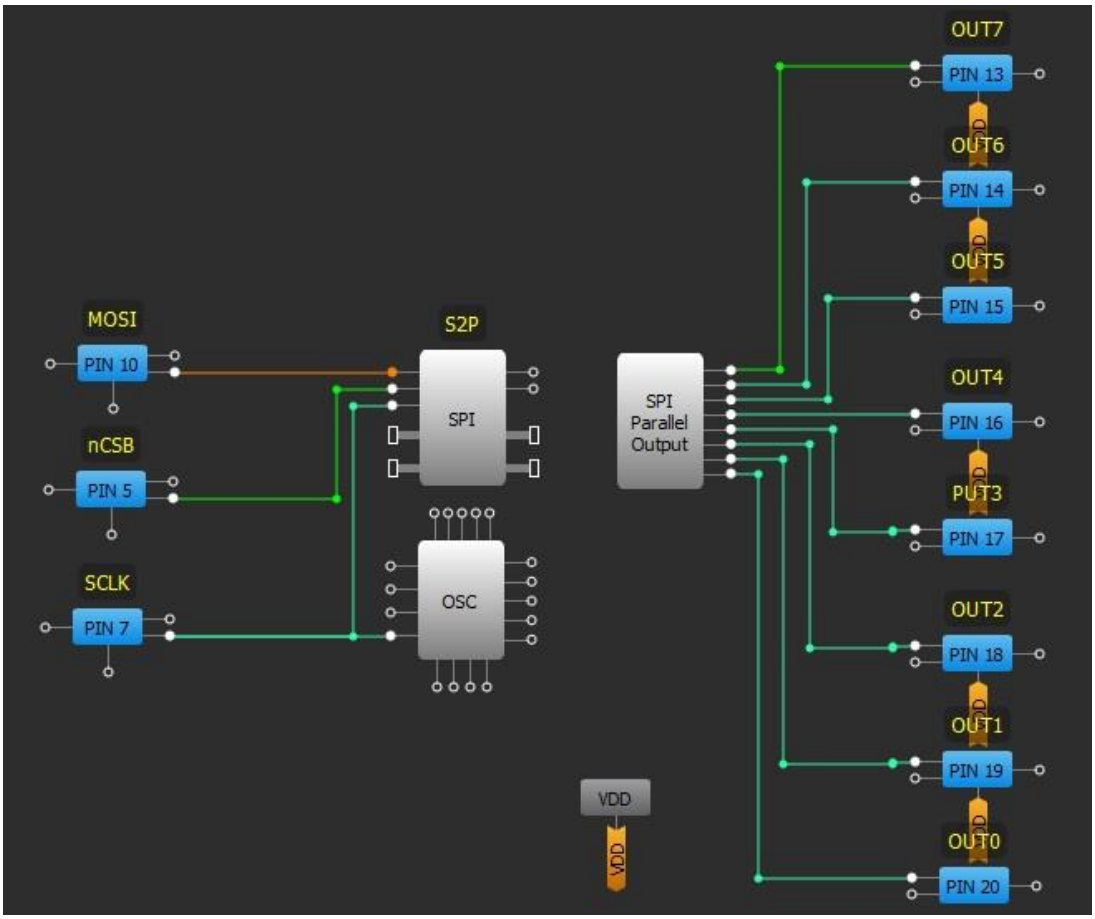


Figure 1. SPI converter circuit

SPI converter circuit analysis

Only after the nCSB signal goes from HIGH to LOW can valid serial data input be started. Depending on SPI 1-bit CPOL and CPHA register settings, information input may happen on rising or falling SCLK signal edges, and SCLK signal may be inverted or not. See clock phase and polarity description with respect to the data in the SLG46620 datasheet file.

First case (CPHA = 0; CPOL = 0)

In this case SCLK signal is not inverted and MOSI input is written on the rising edge of the SCLK signal. See block configuration in Figure 2.

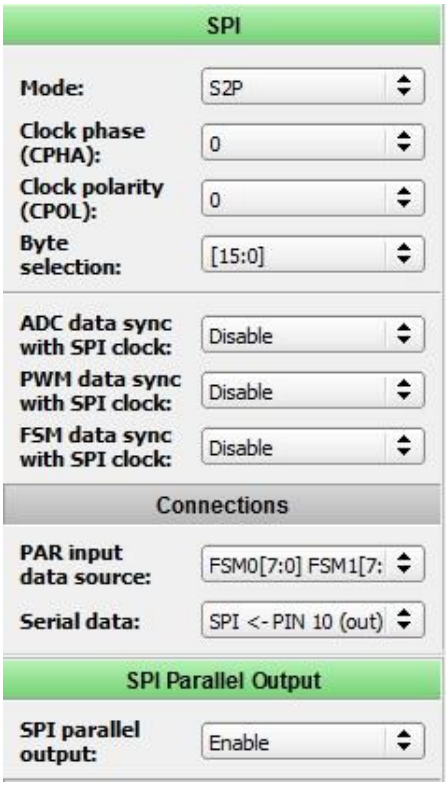
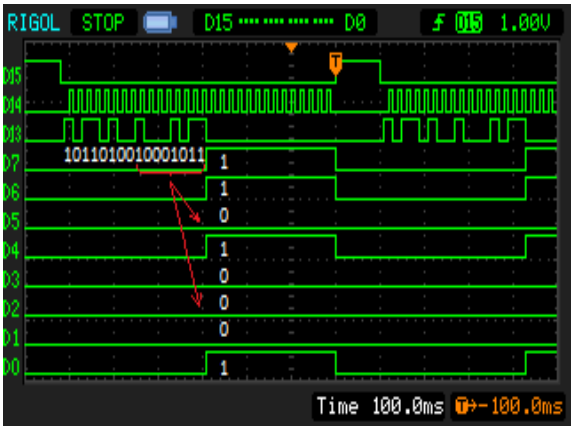


Figure 2. SPI and SPI Parallel Output block configuration

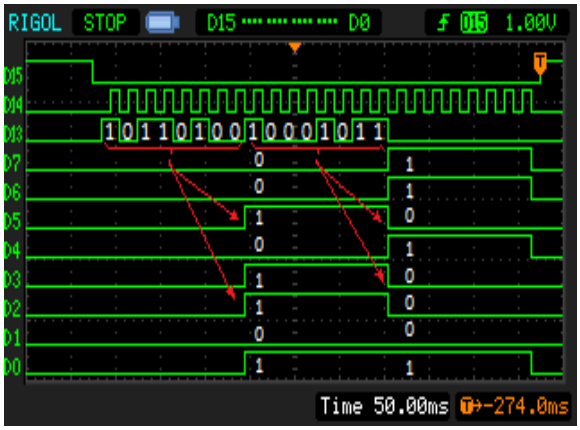
Byte selection option determines whether it will be 16-bit ([15:0] option) or 8-bit ([7:0] option) input. In the case of 16-bit serial input, the last 8-bit data will be presented on SPI Parallel Output after 16th SCLK pulse falling edge. The first 8-bit data will be ignored. (See figure 3).



(D15 – nCSB; D14 – SCLK; D13 – MOSI; D7..D0 – OUT0..OUT7)

Figure 3. SPI converter functional waveforms (Byte selection = [15:0])

Figure 4 shows the case when Byte selection value is [7;0]. In this case, parallel data output will be presented after the 8th SCLK pulse falling edge.



(D15 – nCSB; D14 – SCLK; D13 – MOSI; D7..D0 – OUT0..OUT7)

Figure 4. SPI converter functional waveforms (Byte selection = [7:0])

The parallel output data will hold until the next conversion begins, or when nCSB goes HIGH.

Second case (CPHA = 0; CPOL = 1)

In this case SCLK signal is inverted and MOSI input data are written by the falling edge of SCLK signal. See block configuration in Figure 5.

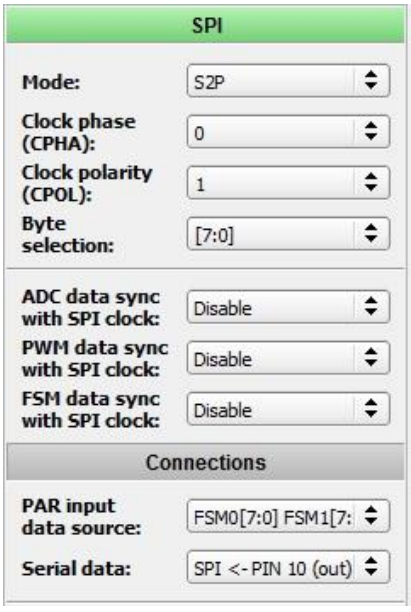
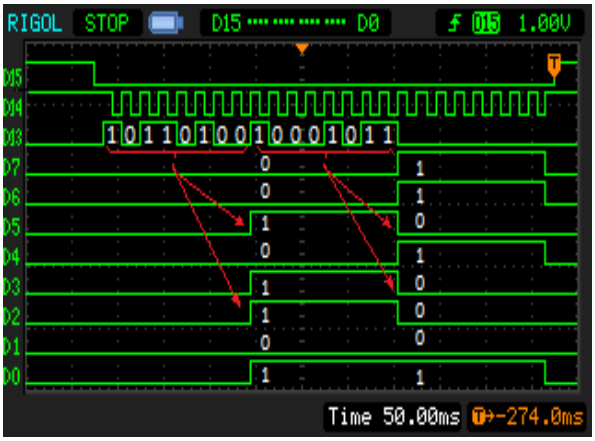


Figure 5. SPI block configuration

Parallel data output will be presented after the 8th SCLK pulse rising edge. (See Figure 6).



(D15 – nCSB; D14 – SCLK; D13 – MOSI; D7..D0 – OUT0..OUT7)

Figure 6. SPI converter functional waveforms

Third case (CPHA = 1; CPOL = 0)

In this case SCLK signal is not inverted and MOSI input data are written by the falling edge of SCLK signal. See block configuration in Figure 7.

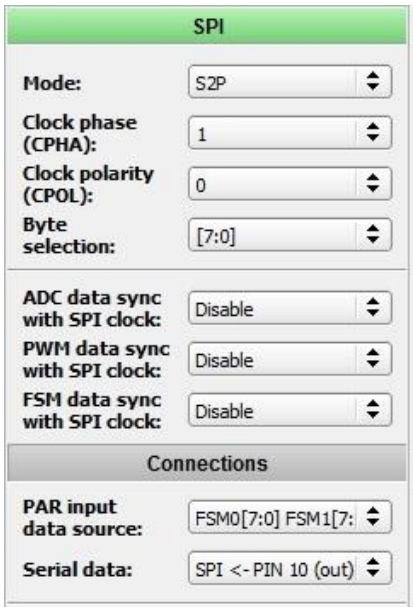
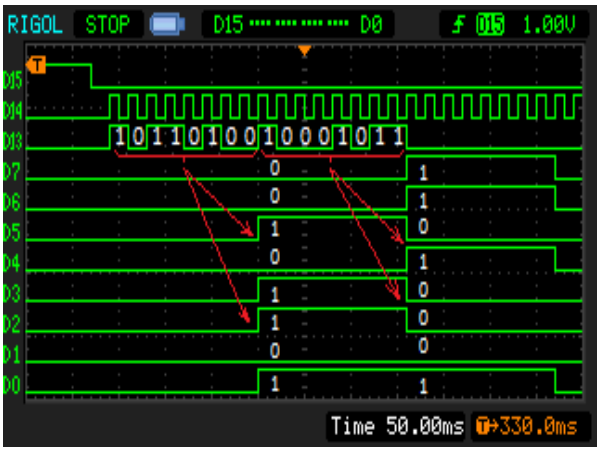


Figure 7. SPI block configuration

Parallel data output will be presented after the 9th SCLK pulse rising edge. (See Figure 8).



(D15 – nCSB; D14 – SCLK; D13 – MOSI; D7..D0 – OUT0..OUT7)

Figure 8. SPI converter functional waveforms

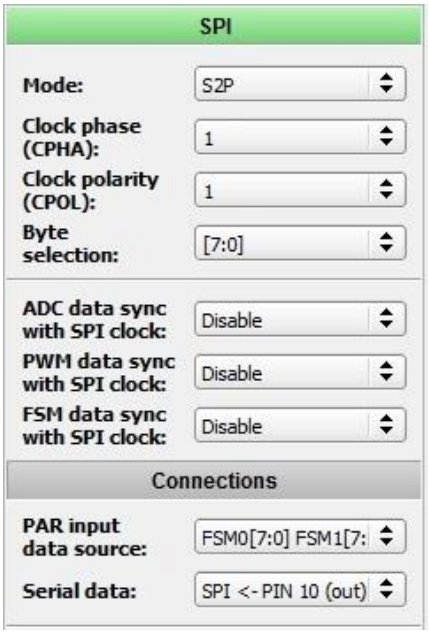
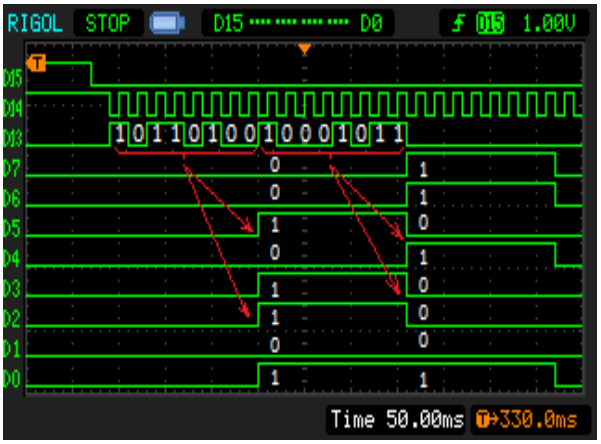


Figure 9. SPI block configuration

Fourth case (CPHA = 1; CPOL = 1)

In this case SCLK signal is inverted and MOSI input is written by the falling edge of SCLK signal. See block configuration in Figure 9.

Parallel data output will be presented after the 9th SCLK pulse falling edge. (See Figure 10).



(D15 – nCSB; D14 – SCLK; D13 – MOSI; D7..D0 – OUT0..OUT7)

Figure 10. SPI converter functional waveforms

Conclusion

This circuit performs conversion of a serial signal such as SPI, into parallel. Each of the parallel bits are then available for connection to other circuitry inside the SLG46620 IC, or driven to external pins for external device control.

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