QUALITY SEMICONDUCTOR, INC.

Board Assembly Techniques for 0.4mm Pin Pitch Surface Mount Packages

Application Note AN-20

The need for higher performance systems continues to push both silicon and packaging technologies to new advances. As an example, in 1991 Quality Semiconductor (QSI) introduced the QSOP (Quarter Size Outline Package) package that provided system designers with the highest density package for interface logic devices. The QSOP used a combination of existing technologies to provide a very small, cost effective solution for systems with limited board area. By using the same assembly mold tooling as the narrow body (150-mil) SOIC and designing a lead frame with a standard 25-mil pin pitch, QSI was able to provide the same functionality as a 300-mil wide SOIC in one fourth the space. All of this was accomplished without pushing the state of the art in circuit board assembly technology. Subsequent generations of QSI packages will maintain this philosophy, including the 40- and 48-pin QVSOP™ packages, which provide double width logic in the same form factor as the 28-pin QSOP. Another advanced package is the industry standard 120-pin TQFP for specialty memory devices. The 40-pin QVSOP has a pin pitch of 0.5mm which can be manufactured using standard surface mount techniques. However, because the pin pitch of the 48-pin QVSOP and the 120-pin TQFP is 0.4mm, additional care must be used in the printed circuit board (PCB) assembly process. The purpose of this application note is to outline the basic board assembly operation using fine pitch packages and provide detail on each portion of the operation as it pertains specifically to packages with 0.4mm pin pitch.

QSI's Packaging Uses Existing Manufacturing Tools

QSI's approach to new package development keeps in mind both the need to provide higher density packages to its customers and the need to minimize new package start up costs. The QSOP uses all of the same manufacturing equipment as the narrow SOIC from packaging assembly to placement on the circuit board. The assembly mold for the 20- and 24-pin QSOP, which is used to form the plastic around the silicon die, is the same mold used for the 14-pin narrow SOIC. This eliminated the cost, and time, of developing an entirely new mold for a non-standard body size. This savings of cost and time extends to test handlers and shipping tubes, during device test and to tape and reel equipment and lead scan equipment during final preparation for shipment. From the board assembly standpoint, component placement equipment need not be modified to accommodate a new body size.

This packaging development philosophy has extended to QSI's next generation of packaging. The 48-pin QVSOP utilizes the same body, hence assembly mold, as the 16-pin narrow SOIC and the 28-pin QSOP. The QVSOP uses the same manufacturing equipment as the QSOP as well. Using the existing manufacturing tools means lower development costs will be incurred and lower costs can be passed on to the end user.

By using a pin pitch of 0.4mm, a new level of system density can been achieved with the 48-pin QVSOP. This is illustrated in Figure 1. With this new level of system density comes a few new challenges during the board assembly process that can be overcome using some slightly different PCB manufacturing techniques.

SMT Board Manufacturing Primer

The simplified model of the board assembly process is divided into four sections and each will be discussed in detail. Board layout, the first portion, begins before the board is manufactured. Critical issues at this stage are design and layout philosophy, and board manufacturing capabilities. After the board has completed layout and manufacture, solder must be deposited on the board as the next step in the process. Once the solder is on the board, each component is placed on the board and the solder is reflowed to create reliable solder joints between the component leads and the circuit board. The last step in the process, rework, is necessary only if there are any soldering defects from the previous steps in the process. This article will start with the basic PCB manufacturing flow used with 25-mil pin pitch devices and will provide information to enhance this flow to incorporate the use of 15-mil (0.4mm) pin pitch devices.

Layout With Rework Capability Minimizes Cost

A common argument used against higher density packaging is that the smaller space is of no benefit because the vias used to interconnect between board layers no longer fit under the package. This argument is only valid if no rework capability is designed into the circuit. However, as package geometries shrink, circuit rework and testability issues become even more important. A PCB layout technique called cut, etch and rewire provides a low cost method for quickly modifying PCB's and takes full advantage of the board space savings that fine pitch packages such as the QVSOP provide. Cut, etch and rewire requires that there be a top layer etch run that separates the device pad from the PCB via. Any pin can then be removed from the circuit and rewired to either a bond pad or a via. This technique is described in detail in QSI's application note AN-19.

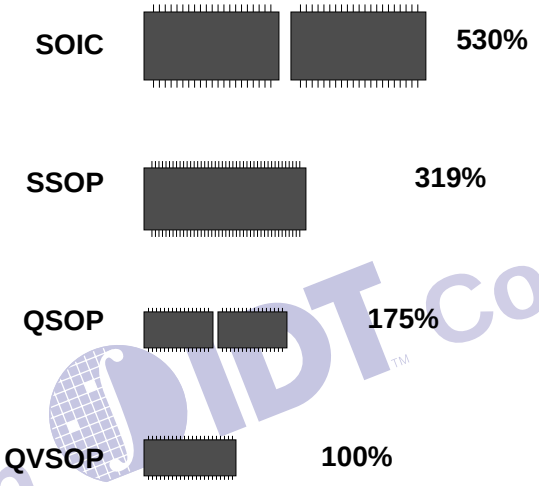

Figure 1. Relative Area of 16 Bit Packaging Solutions

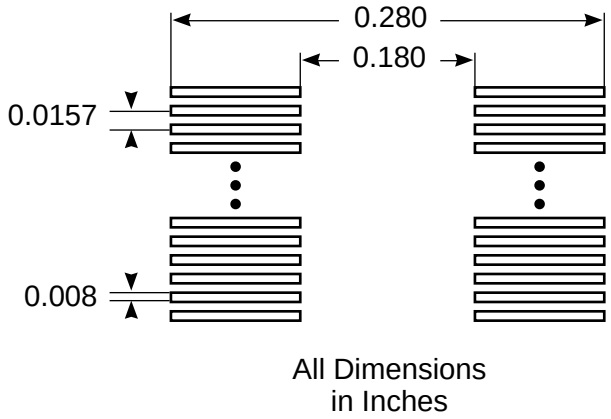

Figure 2. 48-pin QVSOP Footprint

Old Methods of Solder Deposition Limited

After the PCB is manufactured, solder must be deposited on the landing pads where the SMT device leads are to be placed. There are different ways to accomplish solder deposition onto the PCB for 0.4mm pin pitch devices. The standard method of solder deposition is stencil printing of solder paste. In this method a stencil, usually made of stainless steel, is placed over the PCB and solder paste is squeegeed through the holes of the stencil onto the SMT landing pads. Other techniques of solder deposition onto PCB's involve plating the board with solder during the manufacturing process. There are several methods used to accomplish this that will be discussed.

At 0.4mm pin pitch, there are issues with both the stencil thickness and the solder paste viscosity when using the solder paste method of deposition. When mixing fine pitch SMT devices and through hole components on the same board, it may be necessary to have a two pass stencil operation or a single pass with a stepped stencil, a single stencil with different thicknesses. This is necessary so that the larger pitch devices have taller solder columns for better, more reliable solder joints. As the SMT geometries shrink, the thickness of the stencil must also decrease because of the properties of the solder paste. For example, a small hole in a thick stencil will give very inconsistent deposition results. As a general rule for applying solder paste via stencils, reliable solder deposition results can be achieved by maintaining an aspect ratio (stencil aperture width divided by the stencil foil thickness) of between 1.5 and 2.0.[1] This may not always be possible when mixing SMT devices with standard and fine pitch leads. Using this rule, a 50-mil pin pitch SOIC would require a stencil thickness of approximately 8-mil and a 48-pin QVSOP would require a stencil thickness of about 5-mil. Data has shown, however, that when mixing standard and fine pitch SMT components, a uniform thickness stencil as thin as 4-mil will have no negative effect on the larger geometry solder joints.[2] This allows for relatively easy mixing of standard and fine pitch SMT components on the same PCB layout.

New Methods Ease Fine Pitch Solder Deposition

While 0.4mm pin pitch devices can be reliably manufactured using solder paste, other methods of solder deposition can be easier to manufacture as the PCB geometries shrink. There are at least three new solder deposition technologies[3], Optipad[4], Sipad[5], and Precision Pad Technology[6] (PPT), currently available. Board manufacturers, licensed to use these technologies, will apply a solid, reflowed solder deposit on the bare PCB. The additional cost in the PCB manufacturing process is offset by the elimination of several steps from the solder deposition process, improved yields in the PCB manufacturing process, and by the additional board space savings that the high-density packages provide.

The first of these processes, Optipad, uses a photoimageable temporary mask that takes the place of the stencil. This temporary mask is placed over the permanent solder mask and acts as a mold for the solder Because the mask is photographically formed, it is dimensionally more precise than a stencil which enables finer geometries to be more easily integrated into the PCB layout. After the temporary solder mask is applied, molten solder is then applied to the PCB through the open areas of the Optipad mask. When the solder has cooled, the temporary mask is removed and the solder is left encapsulating each pad on the PCB. The solder thickness is determined by the thickness of the temporary solder mask. The finished solder deposits in the Optipad process project above the surface of the permanent solder mask.

Sipad, another new method of solder deposition, relies on a permanent solder mask to act as the mold for the solder. In the case of Sipad, the thickness of the permanent solder mask will determine the final solder thickness. Solder is deposited via solder paste through a stencil, as in conventional solder deposition, but is then reflowed and flattened, filling the well formed by the permanent solder mask. The finished solder deposits in the Sipad process are flush with the solder mask.

The PPT process uses a permanent solder mask as well as an off-contact containing fixture to determine the final height of the deposited solder. As with Sipad, solder is applied via conventional stencil methods, then reflowed and molded into the well formed by the permanent solder mask. The finished solder deposits in the PPT process are thicker than the permanent solder mask by virtue of the additional containing fixture used in the solder deposition process.

The advantage of each of the processes is that solder deposition becomes part of the PCB manufacturing process and greatly simplifies the assembly operation. While this will result in an increase in the PCB

manufacturing costs, these costs will be offset by reduced PCB assembly costs, increased assembly yields and reduced board space used by fine pitch packages.

Optical Placement Needed for Best Results at 0.4mm Pin Pitch

Once the PCB has been prepared with the solder, it is ready to have the individual components placed and soldered. While devices with 0.635mm (25-mil) pin pitch can be placed with mechanical equipment, this may or may not be the case with 0.5mm (20-mil) pin pitch devices. This is because mechanical placement equipment relies on the body of the package for alignment. However, mold flash negatively affects package tolerances that limit the repeatability of mechanical placement equipment. Mold flash is residual plastic that is left both at the end of the package and between the leads during the mold injection portion of the package assembly operation and can vary by a few mils from package to package.

For devices of pin pitch 0.4mm (15-mil), such as the QVSOP, placement equipment that utilizes optics for component alignment is the most reliable method of placement. As the pin pitch of a device grows smaller, the variation in mold flash becomes more of a factor using mechanical placement equipment. For example, a 3 mil variation in mold flash for a 0.635 (25-mil) pin pitch device amounts to a maximum misalignment between the device lead and the landing pad of about 30% of the pad width. For a device with 0.4 mm pin pitch the misalignment grows to close to 50% of the pad width. With a small misalignment, the surface tension of the solder will self align the device. However, if the misalignment is too great, as is the case with 0.4mm pin pitch devices, the result can be excessive solder bridging.

Good Lead Conformity Improves PCB Assembly Yield

In addition to accurate solder deposition and component placement, another factor that affects PCB assembly yield is the conformity of the package leads. Two common measures of lead conformity are coplanarity and sweep. Lead coplanarity, the most common lead conformity parameter, is the measure of vertical misalignment of a lead from the horizontal seating plane. Lead sweep is the measure of device lead's side to side misalignment. Misalignment of the devices leads can lead to opens or shorts on the PCB which will result in a lower PCB assembly yield. Usually, devices with smaller lead pitches, have thinner, more fragile leads that bend more easily. The QVSOP, however, uses an 8-mil thick leadframe, the same thickness as the QSOP, to maintain excellent lead strength. Lead coplanarity and sweep can be improved significantly if component manufacturers institute not only a lead inspection operation but also a lead conditioning operation to realign any bent leads.

Lead coplanarity affects how well a device lead will make contact with the deposited solder column. The taller the solder column, the less stringent the lead coplanarity needs to be for a reliable solder connection. However, as lead pitches shrink, the thickness of the solder deposit, hence the solder column height tends to decrease which means that tighter coplanarity specifications are required to achieve the same solder connection reliability. When working with fine pitch devices, a coplanarity tolerance of 4-mil is about the maximum allowable for the device lead to make adequate contact with the solder column. In fact, the QVSOP package's lead coplanarity is a maximum of 3-mil.

Excessive lead sweep causes the device lead to be misaligned with respect to the PCB landing pad which in turn can lead to solder bridging to adjacent leads. Leads on the corners of the package are the most susceptible to lead sweep because these leads usually encounter the most mechanical stress. QSI performs lead scan and lead conditioning as a standard part of the manufacturing process to insure the best possible lead conformity of devices.

PCB Rework Techniques

The same issues that apply in the manufacturing of PCB's containing 0.4mm pin pitch devices are also important when it comes to rework and repair of PCB assemblies. If a device on a PCB must be replaced, first the solder must be heated and the device removed, then a new device must be placed onto the PCB and soldered in place. The solder operation for 0.4mm pin pitch devices, whether done manually or automatically, can use the same methods as with 20-mil or 25-mil pin pitch devices. These methods include hot bar, hot gas, or focused IR to name a few. During the soldering operation, it is important to maintain good direction control on the heat source as to not affect any adjacent devices. With smaller devices, this becomes even more critical. Device placement may also require additional care. In low volume applications, removal, replacement and sol-

dering can be done manually, but this does require a great deal of expertise and very steady hands when working with devices with 0.4mm pin pitch. In high-volume applications, the use of a vision placement system as in the standard production flow will provide the best placement accuracy and the highest rework yields.

Summary

Some portions of the surface mount PCB assembly process must change when using fine pitch packages such as the 48-pin QVSOP with 0.4mm pin pitch. While the board technology stays the same, solder deposition, component placement and rework require different assembly techniques than those used with larger pin pitch SMT devices. This is shown in Table 1. Solder deposition can be accomplished using standard surface mount methods, but new deposition methods performed during PCB manufacturing may be more cost effective. Component placement of 0.4mm pin pitch devices requires a vision placement system for best results. Rework and repair can use much of the same processing as standard fine pitch devices but a vision placement system may be required in high-volume applications.

Table 1. Recommended Methods of SMT Manufacturing

Pin Pitch	PCB Technology	Solder Deposition	Component Placement	Repair/ Rework
0.65mm (25-mil)	Standard fine pitch techniques	Solder paste applied with stencil	Mechanical	Standard fine pitch techniques
0.5mm (20-mil)	Standard fine pitch techniques	Solder paste applied with stencil	Mechanical placement usually OK	Standard fine pitch techniques
0.4mm (15-mil)	Standard fine pitch techniques	Solder paste applied with stencil*	Vision system for best results	Vision may be needed for placement

* Other techniques described in the text may yield better results

For specific information on contract manufacturers that can assemble PCB's with 0.4mm pin pitch components or to obtain a list of equipment and material used in the fine pitch manufacturing process, please contact a Quality Semiconductor field applications engineer.

[1] Coleman, Dr. William E. "Photochemically Etched Stencils for Ultra-Fine-Pitch Printing." Surface Mount Technology, June 1993.
[2] Latta, Richard and Alsa, Jess. "Reducing Solder Volume." Circuits Assembly, April 1993.
[3] Payne, Bradley and Holzmann, Damian. "A Step in the Right Direction." Circuits Assembly, February 1993.
[4] Developed by SMW Electronik, Germany
[5] Developed by Siemens AG, Germany
[6] Developed by Mask Technology, Inc., Santa Ana, CA