To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

38D2 Group
List of Registers

1. Abstract

The following article introduces and shows the SFR registers of the 38D2 Group.

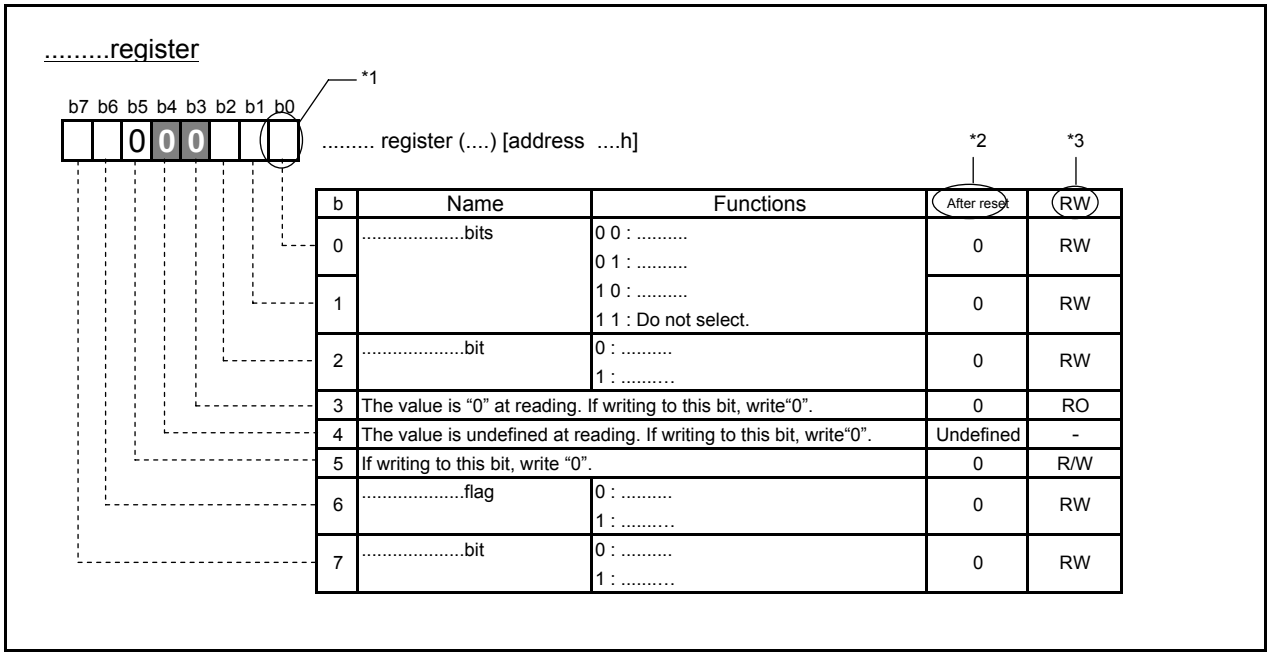
2. Introduction

The explanation of this issue is applied to the following MCU:

Applicable MCU: 38D2 Group

3. Structure of Register

The following is an example of the SFR register structure figure used in this application note and definitions of codes or abbreviations used in this figure are explained below.



b	Name	Functions	After reset	RW
0	.....bits	0 0 : ..... 0 1 : ..... 1 0 : ..... 1 1 : Do not select.	0	RW
1			0	RW
2	.....bit	0 : ..... 1 :	0	RW
3	The value is “0” at reading. If writing to this bit, write“0”.		0	RO
4	The value is undefined at reading. If writing to this bit, write“0”.		Undefined	-
5	If writing to this bit, write “0”.		0	R/W
6	.....flag	0 : ..... 1 :	0	RW
7	.....bit	0 : ..... 1 :	0	RW

*1

Blank	: Set “1” or “0” to this bit according to use.
0	: If writing to this bit, write "0".
1	: If writing to this bit, write "1".
×	: This bit is not used in the specific mode or state.
	: Nothing is arranged for this bit.

*2

0	: “0” after reset
1	: “1” after reset
Undefined	: Undefined after reset

*3

RW	: Read enabled. Write enabled.
RO	: Read enabled. This value depends on each bit at writing.
WO	: Write enabled. Undefined at reading.
-	: Undefined at reading. This value depends on each bit at writing.

4. List of Registers

Port Pi Register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi register (Pi) (i = 0 to 5) [addresses 0000h, 0002h, 0004h, 0006h, 0008h, 000Ah]

b	Name	Function	After reset	RW
0	Port P_{i0}	• In output mode Write: Port latch Read: Port latch or output of peripheral function (Note) • In input mode Write: Port latch Read: Value of pin	0	RW
1	Port P_{i1}		0	RW
2	Port P_{i2}		0	RW
3	Port P_{i3}		0	RW
4	Port P_{i4}		0	RW
5	Port P_{i5}		0	RW
6	Port P_{i6}		0	RW
7	Port P_{i7}		0	RW

Note: The output value is read when shared output function is selected at the following ports.
$P3_5/TX_{OUT1}$, $P3_6/T2_{OUT}$/CKOUT, $P4_0/O_{OUT0}$, $P4_1/O_{OUT1}$, $P4_6$/RTP0, $P4_7$/RTP1, $P5_2/T3_{OUT}$/PWM0, $P5_3/T4_{OUT}$/PWM1

Fig. 4.1 Structure of Port Pi register (i = 0 to 5)

Port P6 register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0

Port P6 register (P6) [address 000Ch]

b	Name	Functions	After reset	RW
0	Port $P6_0$	• In output mode Write: Port latch Read: Port latch • In input mode Write: Port latch Read: Value of pin	0	RW
1	Port $P6_1$		0	RW
2	Port $P6_2$		0	RW
3	The values are undefined at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.2 Structure of Port P6 register

Port Pi direction register

b7 b6 b5 b4 b3 b2 b1 b0

Port Pi direction register (PiD) (i = 0 to 5) [addresses 0001h, 0003h, 0005h, 0007h, 0009h, 000Bh]

b	Name	Functions	After reset	RW
0	Port Pi_0 direction register	0: Input mode 1: Output mode	0	WO
1	Port Pi_1 direction register	0: Input mode 1: Output mode	0	WO
2	Port Pi_2 direction register	0: Input mode 1: Output mode	0	WO
3	Port Pi_3 direction register	0: Input mode 1: Output mode	0	WO
4	Port Pi_4 direction register	0: Input mode 1: Output mode	0	WO
5	Port Pi_5 direction register	0: Input mode 1: Output mode	0	WO
6	Port Pi_6 direction register	0: Input mode 1: Output mode	0	WO
7	Port Pi_7 direction register	0: Input mode 1: Output mode	0	WO

Notes: 1. In port(s) P0 to P2 set to input mode, pull-up resistor can be controlled by segment output disable registers 0 to 2 (addresses 0FF4h to 0FF6h) (refer to Fig. 4.54).
In port(s) set to output mode, pull-up resistor is not connected
In ports P3 to P5, pull-up resistor can be controlled by PULL register (address 0FF0h).
In port(s) set to output mode, each corresponding pull-up control bit becomes invalid and pull-up resistor is not connected.

2. In output mode, output structure of port $P5_6$ pin can be selected at $P5_5/TXD_1$ P-channel output disable bit (bit 4 at UART1 control register (address 001Bh)).

3. In output mode, output structure of port $P3_2$ pin can be selected at $P3_2/TXD_2$ P-channel output disable bit (bit 4 at UART2 control register (address 0FF1h)).

4. When VL pin input selection bit (bit 5 at LCD power control register (address 0014h)) is set to "1", settings of $P2_6$ and $P2_7$ become invalid.

Fig. 4.3 Structure of Port Pi direction register (i = 0 to 5)

Port P6 direction register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

Port P6 direction register (P6D) [address 000Dh]

b	Name	Functions	After reset	RW
0	Port $P6_0$ direction register	0: Input mode 1: Output mode	0	WO
1	Port $P6_1$ direction register	0: Input mode 1: Output mode	0	WO
2	Port $P6_2$ direction register	0: Input mode 1: Output mode	0	WO
3	The values are "0" at reading. If writing to these bits, write "0".		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: In port P6, pull-up resistor can be controlled by PULL register (address 0FF0h).
In port(s) set to output mode, each corresponding pull-up control bit becomes invalid and pull-up resistor is not connected.

Fig. 4.4 Structure of Port P6 direction register

Oscillation output control register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0 0 _ _ Oscillation output control register (OSCOUT) [address 0010h]

b	Name	Functions	After reset	RW
0	$P4_0$/$P4_1$ oscillation output control bits	b1 b0 0 0: $P4_1$, $P4_0$ = Normal port 0 1: $P4_1$ = Normal port, $P4_0$ = X_{OUT}	0	RW
1		1 0: $P4_1$ = Normal port, $P4_0$ = X_{COUT} 1 1: $P4_1$ = X_{COUT}, $P4_0$ = X_{OUT}	0	RW
2	If writing to these bits, write “0”. Do not write "1".		0	RW
3			0	RW
4			0	RW
5			0	RW
6			0	RW
7			0	RW

Notes: 1. X_{COUT} external output signal becomes "H" when the sub clock stops oscillating or is in stop mode while the function to output the signal from the X_{COUT} pin externally is selected.
2. X_{OUT} external output signal becomes "H" when the main clock stops oscillating or is in stop mode while the function to output the signal from the X_{OUT} pin externally is selected.

Fig. 4.5 Structure of oscillation output control register

CPU mode register 2

b7 b6 b5 b4 b3 b2 b1 b0

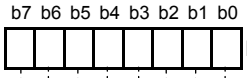
0 0 0 0 0 0 0 _ CPU mode register 2 (CPUM2) [address 0011h]

b	Name	Functions	After reset	RW
0	On-chip oscillator stop bit (Note 1)	0: Oscillating 1: Stop oscillating	(Note 2)	RW
1	If writing to this bit, write “0”. Do not write “1”.		0	RW
2	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6	If writing to these bits, write “0”. Do not write “1”.		0	RW
7			0	RW

Notes: 1. When the on-chip oscillator is selected by the watchdog timer count source selection bit 2 (bit 5 of watchdog timer control register (address 0029_{16})), the on-chip oscillator does not stop even when the on-chip oscillator stop bit is set to “1”. Also, when the low-speed mode is set, the on-chip oscillator stops regardless of the value of this bit in the QzROM version. The on-chip oscillator does not stop in the flash memory version, so set this bit to “1” to stop the oscillation. In on-chip oscillator mode, even if this bit is set to "1", the on-chip oscillator does not stop in the flash memory version, but stops in the QzROM version.
2. Flash memory version, the OSCSEL pins of the QzROM version = L: 1, the OSCSEL pin of the QzROM version = H: 0.

Fig. 4.6 Structure of CPU mode register 2

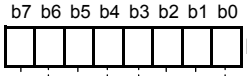
RRF register



b	Functions	After reset	RW
0	DB4 data storage	0	RW
1	DB5 data storage	0	RW
2	DB6 data storage	0	RW
3	DB7 data storage	0	RW
4	DB0 data storage	0	RW
5	DB1 data storage	0	RW
6	DB2 data storage	0	RW
7	DB3 data storage	0	RW

Fig. 4.7 Structure of RRF register

LCD mode register



b	Name	Functions	After reset	RW
0	Duty ratio selection bits	b1 b0 0 0: Do not select. 0 1: 2 (Use COM_0, COM_1) 1 0: 3 (Use COM_0 to COM_2) 1 1: 4 (Use COM_0 to COM_3)	0	RW
1			0	RW
2	Bias control bit	0: 1/3 bias 1: 1/2 bias	0	RW
3	LCD enable bit	0: LCD OFF 1: LCD ON	0	RW
4	LCD drive timing selection bit	0: Type A 1: Type B	0	RW
5	LCD circuit divider division ratio selection bits	b6 b5 0 0: Clock input 0 1: 2 division of clock input 1 0: 4 division of clock input 1 1: 8 division of clock input	0	RW
6			0	RW
7	LCDCK count source selection bit (Note)	0: f(X_{CIN})/32 1: ϕSOURCE/8192 ϕSOURCE : f(X_{IN}) (frequency/2, 4, or 8 mode) f(X_{CIN}) (low-speed mode) f(OCO)/4 (on-chip oscillator mode)	0	RW

Note: LCDCK is a clock for LCD timing controller.

Fig. 4.8 Structure of LCD mode register

LCD power control register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 LCD power control register (VLCON) [address 0014h]

b	Name	Functions	After reset	RW
0	Dividing resistor for LCD power control bit	0: Internal dividing resistor disconnected from LCD power circuit 1: Internal dividing resistor connected to LCD power circuit	0	RW
1	Dividing resistor for LCD power selection bits (Note 1)	b2 b1 1 0: ↑ Larger value of resistance 0 1 : 0 0 : 1 1 : ↓ Smaller value of resistance	0	RW
2			0	RW
3	If writing to these bits, write “0”. Do not write "1".		0	RW
4			0	RW
5	VL pin input selection bit	0: Input invalid 1: VL input function valid (Note 2)	0	RW
6	V_{L3} connection bit	0: Connect LCD internal V_{L3} to V_{CC} 1: Connect LCD internal V_{L3} to V_{L3} pin	0	RW
7	If writing to this bit, write “0”. Do not write "1".		0	RW

Notes: 1. When voltage is applied to V_{L1} to V_{L3} using the external resistor, write "10b" to dividing resistor for LCD power selection bit (RSEL).
2. Setting of VL pin input selection bit (VLSEL) = "1" has higher priority than settings of port 2 direction register (address 0005h) and segment output disable register 2 (address 0FF6h).

Fig. 4.9 Structure of LCD power control register

AD control register

b7 b6 b5 b4 b3 b2 b1 b0

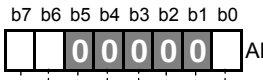
AD control register (ADCON) [address 0015h]

b	Name	Functions	After reset	RW
0	Analog input pin selection bits	b2 b1 b0 0 0 0: $P4_0/AN_0$ 0 0 1: $P4_1/AN_1$ 0 1 0: $P4_2/AN_2$ 0 1 1: $P4_3/AN_3$ 1 0 0: $P4_4/AN_4$ 1 0 1: $P4_5/AN_5$ 1 1 0: $P4_6/AN_6$ 1 1 1: $P4_7/AN_7$	0	RW
1			0	RW
2			0	RW
3	AD conversion completion bit	0: Conversion in progress 1: Conversion completed	1	RW (Note 1)
4	AD conversion clock selection bit	0: ϕSOURCE/2 1: ϕSOURCE/8 ϕSOURCE: f(X_{IN}) (frequency/2, 4, or 8 mode) f(OCO)/4 (low-speed mode, on-chip oscillator mode)	0	RW
5	ADKEY enable bit (Note 2)	0: Disabled 1: Enabled	0	RW
6	10-bit or 8-bit conversion switch bit	0: 10-bit AD 1: 8-bit AD	0	RW
7	ADKEY selection bit	0: Disabled 1: Enabled	0	RW

Notes: 1. This bit can be set to “0” but not to “1” by program.
2. When ADKEY enable bit is set to “1”, analog input pin selection bit becomes invalid.
Do not execute A/D conversion by program while ADKEY is enabled.
Values in analog input pin selection bits are not changed by enabling ADKEY.

Fig. 4.10 Structure of AD control register

AD conversion register (low-order)



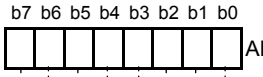
AD conversion register (low-order) (ADL) [address 0016h]

b	Name	Functions	After reset	RW
0	V_{REF} input switch bit	0: Automatic 1: ON	0 (Note 2)	RW
1	The values are “0” at reading. If writing to these bits, write "0".		0	RO
2			0	RO
3			0	RO
4			0	RO
5			0	RO
6	A/D conversion results in 10-bit AD mode can be read. The values at reading in 8-bit AD mode are undefined.	In 10-bit AD mode b7 b0 b1 b0	Undefined	RO
7	If writing to these bits, write "0".		Undefined	RO

Notes: 1. Do not read this register while A/D conversion is executed.
2. The value is undefined at reading.

Fig. 4.11 Structure of AD conversion register (low-order)

AD conversion register (high-order)



AD conversion register (high-order) (ADH) [address 0017h]

b	Functions	After reset	RW
0	A/D conversion results can be read.	Undefined	RO
1	If writing to these bits,	Undefined	RO
2	write “00h”.	Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

In 10-bit AD mode
b7 b0
b9 b8 b7 b6 b5 b4 b3 b2

In 8-bit AD mode
b7 b0
b7 b6 b5 b4 b3 b2 b1 b0

Notes: Do not read this register while A/D conversion is executed.

Fig. 4.12 Structure of AD conversion register (high-order)

Transmit buffer register 1

b7 b6 b5 b4 b3 b2 b1 b0

Transmit buffer register1 (TB1) [address 0018h]

b	Functions	After reset	RW
0	Transmit data is written to this buffer register.	Undefined	WO
1	Write transmit data.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This resister is located at the same address as receive buffer register 1.
This register is write-only.

Receive buffer register 1

b7 b6 b5 b4 b3 b2 b1 b0

Receive buffer register 1 (RB1) [address 0018h]

b	Functions	After reset	RW
0	Receive data is read in this buffer register.	Undefined	RO
1	Read receive data.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is located at the same address as transmit buffer register 1.
This register is read-only.

Fig. 4.13 Structures of transmit buffer register 1 and receive buffer register 1

Serial I/O 1 status register

b7 b6 b5 b4 b3 b2 b1 b0

1 | | | | | | | |

Serial I/O 1 status register (SIO1STS) [address 0019h]

b	Name	Functions	After reset	RW
0	Transmit buffer empty flag (TBE) (Note 1)	0: Buffer register full 1: Buffer register empty	0	RO
1	Receive buffer full flag (RBF) (Note 1, 2)	0: Buffer register empty 1: Buffer register full	0	RO
2	Transmit shift completion flag (TSC) (Note 1)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note 3)	0: No overrun error 1: Overrun error	0	RO
4	Parity error flag (PE) (Note 3)	0: No parity error 1: Parity error	0	RO
5	Framing error flag (FE) (Note 3)	0: No framing error 1: Framing error	0	RO
6	Summing error flag (SE) (Note 3)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	RO
7	The value is “1” at reading. If writing to this bit, write “1”.		1	RO

Notes: 1. If writing to these bits, write "0".
2. This bit becomes "0" when receive buffer register 1 is read.
3. These bits become "0" by writing to this register. If writing to these bits, write "0".

Fig. 4.14 Structure of serial I/O 1 status register

Serial I/O 1 control register

b7 b6 b5 b4 b3 b2 b1 b0

Serial I/O 1 control register (SIO1CON) [address 001Ah]

b	Name	Functions	After reset	RW
0	BRG1 count source selection bit (CSS)	0: ϕSOURCE 1: ϕSOURCE/4 ϕSOURCE: f(XIN) (frequency/2, 4 or 8 mode) f(XCIN) (low-speed mode) f(OCO)/4 (on-chip oscillator mode)	0	RW
1	Serial I/O 1 synchronous clock selection bit (SCS)	In clock synchronous serial I/O Mode 0: BRG1 output divided by 4 1: External clock input In UART mode 0: BRG1 output divided by 16 1: External clock input divided by 16	0	RW
2	$\overline{SRDY1}$ output enable bit (SRDY)	0: Output disabled (Pin $P5_7$: I/O port) 1: Output enabled (Pin $P5_7$: $\overline{SRDY1}$ output pin)	0	RW
3	Transmit interrupt source selection bit (TIC)	0: When transmit buffer has become empty (TBE = 1) 1: When transmit shift operation is completed (TSC = 1)	0	RW
4	Transmit enable bit (TE)	0: Transmission disabled 1: Transmission enabled	0	RW
5	Receive enable bit (RE)	0: Reception disabled 1: Reception enabled	0	RW
6	Serial I/O 1 mode selection bit (SIOM)	0: UART mode 1: Clock synchronous serial I/O Mode	0	RW
7	Serial I/O 1 enable bit (SIOE)	0: Serial I/O 1 disabled (Pins $P5_4$ to $P5_7$: I/O ports) 1: Serial I/O 1 enabled (Pins $P5_4$ to $P5_7$: Serial I/O1 pins)	0	RW

Fig. 4.15 Structure of serial I/O 1 control register

UART1 control register

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1					

UART1 control register (UART1CON) [address 001Bh]

b	Name	Functions	After reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	$P5_5/TxD_1$ P-channel output disable bit (POFF)	In output mode 0: CMOS output 1: N-channel open drain output In input mode, this bit is invalid.	0	RW
5	The values are "1" at reading. If writing to these bits, write "1".		1	RO
6			1	RO
7			1	RO

Fig. 4.16 Structure of UART1 control register

Baud rate generator 1

b7	b6	b5	b4	b3	b2	b1	b0

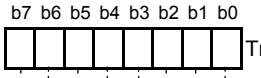
Baud rate generator 1 (BRG1) [address 001Ch]

b	Functions	After reset	RW
0	Set the frequency divide value of BRG count source.	Undefined	RW
1	Baud rate generator divides the frequency of the count source by (n + 1)	Undefined	RW
2	when n is the value written to BRG.	Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: Write to this register only while transmit/receive operation is stopped.

Fig. 4.17 Structure of Baud rate generator 1

Transmit buffer register 2

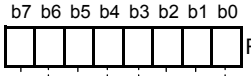


Transmit buffer register 2 (TB2) [address 001Dh]

b	Functions	After reset	RW
0	Transmit data is written to this buffer register.	Undefined	WO
1	Write transmit data to this register.	Undefined	WO
2		Undefined	WO
3		Undefined	WO
4		Undefined	WO
5		Undefined	WO
6		Undefined	WO
7		Undefined	WO

Note: This register is located at the same address as receive buffer register 2.
This register is write-only.

Receive buffer register 2



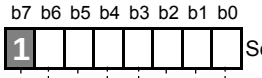
Receive buffer register 2 (RB2) [address 001Dh]

b	Functions	After reset	RW
0	Receive data is read from this buffer register.	Undefined	RO
1	Read receive data from this register.	Undefined	RO
2		Undefined	RO
3		Undefined	RO
4		Undefined	RO
5		Undefined	RO
6		Undefined	RO
7		Undefined	RO

Note: This register is located at the same address as transmit buffer register 2.
This register is read-only.

Fig. 4.18 Structure of Transmit buffer register 2/Receive buffer register 2

Serial I/O 2 status register



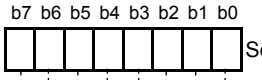
Serial I/O 2 status register (SIO2STS) [address 001Eh]

b	Name	Functions	After reset	RW
0	Transmit buffer empty flag (TBE) (Note 1)	0: Buffer register full 1: Buffer register empty	0	RO
1	Receive buffer empty flag (RBF) (Note 1, 2)	0: Buffer register empty 1: Buffer register full	0	RO
2	Transmit shift completion flag (TSC) (Note 1)	0: Transmit shift in progress 1: Transmit shift completed	0	RO
3	Overrun error flag (OE) (Note 3)	0: No overrun error 1: Overrun error	0	RO
4	Parity error flag (PE) (Note 3)	0: No parity error 1: Parity error	0	RO
5	Framing error flag (FE) (Note 3)	0: No framing error 1: Framing error	0	RO
6	Summing error flag (SE) (Note 3)	0: (OE) U (PE) U (FE) = 0 1: (OE) U (PE) U (FE) = 1	0	RO
7	The value is “1” at reading. If writing to this bit, write “1”.		**1**	RO

Notes: 1. If writing to these bits, write "0".
2. This bit becomes "0" when receive buffer register 2 is read.
3. These bits become "0" by writing to this register. If writing to these bits, write "0".

Fig. 4.19 Structure of Serial I/O 2 status register

Serial I/O 2 control register



Serial I/O 2 control register (SIO2CON) [address 001Fh]

b	Name	Functions	After reset	RW
0	BRG2 count source selection bit (CSS)	0: ϕSOURCE 1: ϕSOURCE/4 ϕSOURCE: f(XIN) (frequency/2, 4, or 8 mode) f(XCIN) (low-speed mode) f(OCO)/4 (on-chip oscillator mode)	0	RW
1	Serial I/O 2 synchronous clock selection bit (SCS)	In clock synchronous serial I/O Mode 0 : BRG output divided by 4 1 : External clock input In UART Mode 0 : BRG output divided by 16 1 : External clock input divided by 16	0	RW
2	$\overline{SRDY2}$ output enable bit (SRDY)	0: Transmission disabled (Pin P30: I/O port) 1: Transmission enabled (Pin P30: $\overline{SRDY2}$ output pin)	0	RW
3	Transmit interrupt source selection bit (TIC)	0: When transmit buffer has become empty (TBE=1) 1: When transmit shift operation is completed (TSC=1)	0	RW
4	Transmit enable bit (TE)	0 : Transmission disabled 1 : Transmission enabled	0	RW
5	Receive enable bit (RE)	0 : Reception disabled 1 : Reception enabled	0	RW
6	Serial I/O 2 mode selection bit (SIOM)	0 : UART mode 1: Clock synchronous serial I/O Mode	0	RW
7	Serial I/O 2 enable bit (SIOE)	0: Serial I/O 2 disabled (Pins P30 to P33: I/O port) 1: Serial I/O 2 enabled (Pins P30 to P33: Serial I/O 2 pins)	0	RW

Fig. 4.20 Structure of Serial I/O 2 control register

Timer 1 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 1 register (T1) [address 0020h]

b	Functions	After reset	RW
0	· Set the count initial value. This register counts (n + 1) times when the set value is n . · Write value to both latch and timer simultaneously at writing. · The value is the count value of timer 1 at reading.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Note: This register is used to generate waiting time After reset and exiting from stop mode.

Fig. 4.21 Structure of Timer 1 register

Timer 2 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 2 register (T2) [address 0021h]

b	Functions	After reset	RW
0	· Set the count initial value. This register counts (n + 1) times when the set value is n . · This register operate as follows at writing. When timer 2 write control bit = “0”: Write value to both latch and timer simultaneously. When timer 2 write control bit = “1”: Write value to latch only. · The value is the count value of timer 2 at reading.	1	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Notes: 1. This register is used to generate waiting time at reset and exiting from stop mode.
2. When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to timer latch.

Fig. 4.22 Structure of Timer 2 register

Timer 3 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 3 register (T3) [address 0022h]

b	Functions	After reset	RW
0	· Set the count initial value. This register counts (n + 1) times when the set value is n .	1	RW
1		1	RW
2	· This register operate as follows at writing. When timer 3 write control bit = “0”: Write value to both latch and timer simultaneously. When timer 3 write control bit = “1”: Write value to latch only.	1	RW
3		1	RW
4		1	RW
5	· The value is the count value of timer 3 at reading.	1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to timer latch.

Fig. 4.23 Structure of Timer 3 register

Timer 4 register

b7 b6 b5 b4 b3 b2 b1 b0

Timer 4 register (T4) [address 0023h]

b	Functions	After reset	RW
0	· Set the count initial value. This register counts (n + 1) times when the set value is n .	1	RW
1		1	RW
2	· This register operates as follows. When timer 4 write control bit = “0”: Write value to both latch and timer simultaneously. When timer 4 write control bit = “1”: Write value to latch only.	1	RW
3		1	RW
4		1	RW
5	· The value is the count value of timer 4 at reading.	1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to timer latch.

Fig. 4.24 Structure of Timer 4 register

PWM01 register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 | | | | | PWM01 register (PWM01) [address 0024h]

b	Name	Functions	After reset	RW
0	PWM0 set bits	b1 b0 0 0: Not extended 0 1: Extended once in four periods 1 0: Extended twice in four periods 1 1: Extended three times in four periods	0	RW
1			0	RW
2	PWM1 set bits	b3 b2 0 0: Not extended 0 1: Extended once in four periods 1 0: Extended twice in four periods 1 1: Extended three times in four periods	0	RW
3			0	RW
4	The value is “0” at reading. If writing to this bit, write “0”.		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.25 Structure of PWM01 register

Timer 12 mode register

b7 b6 b5 b4 b3 b2 b1 b0

| | | | | | | | | Timer 12 mode register (T12M) [address 0025h]

b	Name	Functions	After reset	RW
0	Timer 1 count stop bit	0: Count 1: Stop count	0	RW
1	Timer 2 count stop bit	0: Count 1: Stop count	0	RW
2	Timer 1 count source selection bits	b3 b2 0 0: Frequency divider for timer 1 0 1: f(XCIN) 1 0: Underflow of timer Y 1 1: Do not select.	0	RW
3			0	RW
4	Timer 2 count source selection bits	b5 b4 0 0: Underflow of timer 1 0 1: f(XCIN) 1 0: Frequency divider for timer 2 1 1: Do not select.	0	RW
5			0	RW
6	Timer 2 output selection bit	0: Pin P36 = I/O port 1: Pin P36 = Timer 2 output	0	RW
7	T2OUT output edge switch bit	0: Start at “L” output 1: Start at “H” output	0	RW

Fig. 4.26 Structure of Timer 12 mode register

Timer 34 mode register

b7 b6 b5 b4 b3 b2 b1 b0

0 Timer 34 mode register (T34M) [address 0026h]

b	Name	Functions	After reset	RW
0	Timer 3 count stop bit	0: Count 1: Stop count	0	RW
1	Timer 4 count stop bit	0: Count 1: Stop count	0	RW
2	Timer 3 count source selection bit	0: Frequency divider for timer 3 1: Underflow of timer 2	0	RW
3	Timer 4 count source selection bits	b4 b3 0 0: Frequency divider for timer 4	0	RW
4		0 1: Underflow of timer 3 1 0: Underflow of timer 2 1 1: f(X_{IN})	0	RW
5	Timer 3 operation mode selection bit	0: Timer mode 1: PWM mode	0	RW
6	Timer 4 operation mode selection bit	0: Timer mode 1: PWM mode	0	RW
7	The value is “0” at reading. If writing to this bit, write “0”.		0	RO

Fig. 4.27 Structure of Timer 34 mode register

Timer 1234 mode register

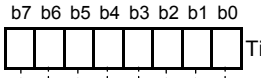
b7 b6 b5 b4 b3 b2 b1 b0

0 Timer 1234 mode register (T1234M) [address 0027h]

b	Name	Functions	After reset	RW
0	T_{3OUT} output edge switch bit	0: Start at ”L” output 1: Start at ”H” output	0	RW
1	T_{4OUT} output edge switch bit	0: Start at ”L” output 1: Start at ”H” output	0	RW
2	Timer 3 output selection bit	0: Pin $P5_2$ = I/O port 1: Pin $P5_2$ = Timer 3 output	0	RW
3	Timer 4 output selection bit	0: Pin $P5_3$ = I/O port 1: Pin $P5_3$ = Timer 4 output	0	RW
4	Timer 2 write control bit	0: Write value to both latch and timer simultaneously 1: Write value to latch only	0	RW
5	Timer 2 write control bit	0: Write value to both latch and timer simultaneously 1: Write value to latch only	0	RW
6	Timer 2 write control bit	0: Write value to both latch and timer simultaneously 1: Write value to latch only	0	RW
7	The value is “0” at reading. If writing to this bit, write “0”.		0	RO

Fig. 4.28 Structure of Timer 1234 mode register

Timer 1234 frequency division selection register



Timer 1234 frequency division selection register (PRE1234) [address 0028h]

b	Name	Functions	After reset	RW
0	Timer 1 frequency division selection bits	b1 b0 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
1			0	RW
2	Timer 2 frequency division selection bits	b3 b2 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
3			0	RW
4	Timer 3 frequency division selection bits	b5 b4 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
5			0	RW
6	Timer 4 frequency division selection bits	b7 b6 0 0: 1/16 × ϕSOURCE 0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE	0	RW
7			0	RW

Note: ϕSOURCE: f(X_{IN}) in frequency/2, 4, or 8 mode
f(X_{CIN}) in low-speed mode
f(OCO)/4 in on-chip oscillator mode

Fig. 4.29 Structure of Timer 1234 frequency division selection register

Watchdog timer control register

b7 b6 b5 b4 b3 b2 b1 b0

Watch dog timer control register (WDTCON) [address 0029h]

b	Name	Functions	After reset	RW
0	Watchdog timer H		1	RO
1			1	RO
2			1	RO
3			1	RO
4			1	RO
5	Watchdog timer count source selection bit 2 (Note1)	0: ϕSOURCE 1: f(OCO)/4 (Note 2) ϕSOURCE: f(X_{IN}) (frequency/2, 4, or 8 mode) f(X_{CIN}) (low-speed mode) f(OCO)/4 (on-chip oscillator mode)	0	RW
6	STP instruction function selection bit (Note 1,2)	0: Enter stop mode by execution of STP instruction 1: Internal reset by execution of STP instruction	0	RW
7	Watchdog timer count source selection bit (Note1)	0: ϕSOURCE/1024 1: ϕSOURCE/4	0	RW

Notes: 1. These bits can be written only once after reset is released.
After being written once, these bits are locked and can not be rewritten.
2. When selecting on-chip oscillator by setting "1" to watchdog timer count source selection bit 2, on-chip oscillator is forced to oscillate and can not be stopped.
At this time, set STP instruction function selection bit to "1".
3. Watchdog timer is set to “FFh” by writing to this register.

Fig. 4.30 Structure of Watch dog timer control register

Timer X register (low-order, high-order)

b7 b6 b5 b4 b3 b2 b1 b0

Timer X register (low-order, high-order) (TXL, TXH) [addresses 002Ah, 002Bh]

b	Functions	After reset	RW
0	· Set the count initial value. These registers count (n + 1) times when the set value is n . When timer X register (expansion) is set, timer X operates as 18-bit counter.	1	RW
1	· These registers operate as follows at writing. When timer X write control bit = "0": Write value to both latch and timer simultaneously. When timer X write control bit = "1": Write value to latch only.	1	RW
2		1	RW
3	This operation is not affected by timer X count stop bit. · Write order in timer mode, pulse output mode, event counter mode and pulse width measurement mode: Expansion, low-order, and high-order. Write order in IGBT output mode and PWM mode: Compare registers 1, 2 and 3, expansion, low-order, and high-order. (Write order of compare registers (low-order and high-order) is not determined).	1	RW
4		1	RW
5		1	RW
6	· The value is the count value of timer X at reading. · Read order: Expansion, high-order and low-order. (Read order of compare registers is not determined).	1	RW
7		1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to the high-order timer latch.

Fig. 4.31 Structure of Timer X register (high-order, low-order)

Timer X register (expansion)

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0		

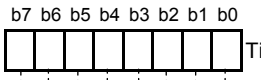
Timer X register (expansion) (TXEX) [address 002Ch]

b	Functions	After reset	RW
0	· Set the count initial value. These registers count (n + 1) times when the set value is n . · This register operates as follows at writing. When timer X write control bit = "0": Write value to expansion latch and expansion counter simultaneously. When timer X write control bit = "1": Write value to expansion latch only. This operation is not affected by timer X count stop bit. · Write order in timer mode, pulse output mode, event counter mode and pulse width measurement mode: Expansion, low-order, and high-order. Write order in IGBT output mode and PWM mode: Compare registers 1, 2 and 3, expansion, low-order, and high-order. (Write order of compare registers (low-order, high-order) is not determined). · The value is the count value of timer X at reading. · Read order: Expansion, high-order and low-order. (Read order of compare registers is not determined).	0	RW
1		0	RW
2	The values are "0" at reading. If writing to these bits, write "0".	0	RO
3		0	RO
4		0	RO
5		0	RO
6		0	RO
7		0	RO

Notes: 1. Timer X operates as 18-bit counter when values are set to this register after reset.
2. Do not write "1" to this register in IGBT output mode and PWM mode.
When "1" has already written to this register, make sure to write "0" to this register before use.

Fig. 4.32 Structure of Timer X register (expansion)

Timer X mode register



Timer X mode register (TXM) [address 002Dh]

b	Name	Functions	After reset	RW
0	Timer X operating mode bits	b2 b1 b0 0 0 0: Timer mode	0	RW
1		0 0 1: Pulse output mode 0 1 0: IGBT output mode	0	RW
2		0 1 1: PWM mode 1 0 0: Event counter mode 1 0 1: Pulse width measurement mode 1 1 0: Do not select. 1 1 1: Do not select.	0	RW
3	Timer X write control bit	0: Write value to both latch and timer simultaneously 1: Write value to latch only	0	RW
4	Timer X count source selection bit	0: Frequency divider output 1: f(X_{CIN})	0	RW
5	Data for control of event counter window	0: Event count enabled 1: Event count disabled	0	RW
6	Timer X count stop bit	0: Count 1: Stop count	0	RW
7	Timer X output 1 selection bit	0: Pin $P3_5$ = I/O port 1: Pin $P3_5$ = Timer X output 1	0	RW

Fig. 4.33 Structure of Timer X mode register

Timer X control register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer X control register 1 (TXCON1) [address 002Eh]

b	Name	Functions	After reset	RW
0	Noise filter sampling clock selection bit	0 : f(XIN)/2 1 : f(XIN)/4	0	RW
1	External trigger delay time selection bits	b2 b1 0 0: Not delayed	0	RW
2		0 1: (4/f(XIN))µs 1 0: (8/f(XIN))µs 1 1: (16/f(XIN))µs	0	RW
3	Timer X output control bit 1	0: P51/INT1 interrupt signal not used 1: P51/INT1 interrupt signal used	0	RW
4	Timer X output control bit 2	0: P34/INT2 interrupt signal not used 1: P34/INT2 interrupt signal used	0	RW
5	Timer X output 1 edge switch bit	0: Start at "L" output 1: Start at "H" output	0	RW
6	CNTR0 active edge switch bits	Depends on timer X operation mode	0	RW
7		(Refer to table 4.1 below)	0	RW

Fig. 4.34 Structure of Timer X control register 1

Table 4.1 Function of CNTR0 active edge switch bits

Timer X operation mode	Set value b7 b6	Timer function/CNTR0 pin function	CNTR0 Interrupt request occurrence source
Timer mode	0 0	External interrupt pin	CNTR0 input signal falling edge (No influence on timer count)
	0 1		CNTR0 input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
Pulse output mode	0 0		Input signal falling edge (No influence on timer count)
	0 1		Input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
IGBT output mode	0 0		Input signal falling edge (No influence on timer count)
	0 1		Input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
PWM mode	0 0		Input signal falling edge (No influence on timer count)
	0 1		Input signal rising edge (No influence on timer count)
	1 0		Input signal falling edge and rising edge (No influence on timer count)
	1 1		
Event counter mode	0 0	Count at rising edge	Input signal falling edge
	0 1	Count at falling edge	Input signal rising edge
	1 0	Count at both edges	Input signal falling edge and rising edge
	1 1	Count at both edges	Input signal falling edge and rising edge
Pulse width measurement mode	0 0	Measure "H" width	Input signal falling edge
	0 1	Measure "L" width	Input signal rising edge
	1 0	Do not select.	
	1 1		

Note: Set bit 7 to "0" in pulse width measurement mode.

Timer X control register 2

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 | | | | | |

Timer X control register 2 (TXCON2) [address 002Fh]

b	Name	Functions	After reset	RW
0	Timer X output 2 selection bit ($P3_7$)	0: Pin $P3_7$ = I/O port 1: Pin $P3_7$ = Timer X output 2	0	RW
1	Timer X output 2 active edge switch bit	0: Start at "L" output 1: Start at "H" output	0	RW
2	Timer X dividing frequency selection bits	b3 b2 0 0: 1/16 × ϕSOURCE	0	RW
3		0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE ϕSOURCE : f(X_{IN}) (frequency/2, 4 or 8 mode) f(X_{CIN}) (low-speed mode) f(OCO)/4 (on-chip oscillator mode)	0	RW
4	Trigger for IGBT input control bit	0: Noise filter sampling clock × 1 External trigger delay time ×1 1: Noise filter sampling clock × 2 External trigger delay time ×2	0	RW
5	The values are "0" at reading. If writing to these bits, write "0".		0	RO
6			0	RO
7			0	RO

Fig. 4.35 Structure of Timer X control register 2

Compare register 1, 2, 3 (low-order, high-order)

b7 b6 b5 b4 b3 b2 b1 b0

Compare register 1 (low-order, high-order) (COMP1L,COMP1H) [addresses 0030h, 0031h]

Compare register 2 (low-order, high-order) (COMP2L,COMP2H) [addresses 0032h, 0033h]

Compare register 3 (low-order, high-order) (COMP3L,COMP3H) [addresses 0034h, 0035h]

b	Functions	After reset	RW
0	· Set values of compare registers.	0	RW
1	· Write order in IGBT output mode and PWM mode:	0	RW
2	Compare registers 1, 2 and 3, expansion, low-order, and high-order	0	RW
3	(Write order of compare registers (high-order, low-order) is not determined).	0	RW
4	· Read order: Expansion, high-order, and low-order	0	RW
5	(Read order of compare registers is not determined).	0	RW
6		0	RW
7		0	RW

Note: Set the smaller value than the timer X register setting value. Do not set 00h.

Fig. 4.36 Structure of Compare register 1, 2, 3 (high-order, low-order)

Timer Y register (low-order, high-order)

b7 b6 b5 b4 b3 b2 b1 b0

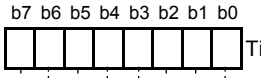
Timer Y register (low-order, high-order) (TYL, TYH) [addresses 0036h, 0037h]

b	Functions	After reset	RW
0	· Set the count initial value. These registers count (n + 1) times when the set value is n . · These registers operate as follows at writing. When timer Y write control bit = "0": Write value to latch and timer simultaneously. When timer Y write control bit = "1": Write value to latch only. Write from high-order to low-order. This operation is not affected by timer Y count stop bit. · The value is the count value of timer Y at reading. Read from high-order to low-order.	1	RW
1		1	RW
2		1	RW
3		1	RW
4		1	RW
5		1	RW
6		1	RW
7		1	RW

Note: When underflow and writing to high-order timer latch occur almost at the same time while selecting writing to timer latch only, the value is set to timer and timer latch simultaneously. At this time, counting is stopped during writing to the high-order timer latch.

Fig. 4.37 Structure of timer Y register (low-order, high-order)

Timer Y mode register



Timer Y mode register (TYM) [address 0038h]

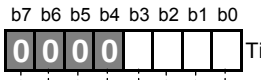
b	Name	Functions	After reset	RW
0	Real time port control bit	b1 b0 0 0: Real time port function of pins $P4_6/RTP_0$, $P4_7/RTP_1$ invalid	0	RW
1		0 1: Do not select 1 0: Do not select 1 1: Real time port function of pins $P4_6/RTP_0$, $P4_7/RTP_1$ valid	0	RW
2	RTP_0 data for real time port	0: "L" output from pin $P4_6/RTP_0$ 1: "H" output from pin $P4_6/RTP_0$	0	RW
3	RTP_1 data for real time port	0: "L" output from pin $P4_7/RTP_1$ 1: "H" output from pin $P4_7/RTP_1$	0	RW
4	Timer Y operation mode bits	b5 b4 0 0: Timer mode	0	RW
5		0 1: Period measurement mode 1 0: Event counter mode 1 1: Pulse width HL continuous measurement mode	0	RW
6	$CNTR_1$ active edge switch bit	Depends on timer Y operation mode (Refer to table 4.2 below)	0	RW
7	Timer Y count stop bit	0: Count 1: Stop count	0	RW

Fig. 4.38 Structure of timer Y mode register

Table 4.2 Function of $CNTR_1$ active edge switch bit

Timer Y operation mode	Set value	Timer function/$CNTR_1$ pin function	$CNTR_1$ Interrupt request occurrence source
Timer mode	"0"	External interrupt pin	$CNTR_1$ input signal falling edge (No influence on timer count)
	"1"		$CNTR_1$ input signal rising edge (No influence on timer count)
Period measurement mode	"0"	Measure the period from falling edge to falling edge	Input signal falling edge
	"1"	Measure the period from rising edge to rising edge	Input signal rising edge
Event counter mode	"0"	Count at rising edge	Input signal falling edge
	"1"	Count at falling edge	Input signal rising edge
Pulse width HL continuous measurement mode	"0"	Measure "H" and "L" pulse widths	Input signal falling and rising edges
	"1"		

Timer Y control register



b	Name	Functions	After reset	RW
0	Timer Y write control bit	0: Write value to latch and timer simultaneously 1: Write value to latch only	0	RW
1	Timer Y count source selection bit	0: Frequency divider output 1: f(XCIN)	0	RW
2	Timer Y frequency division selection bits	b3 b2 0 0: 1/16 × ϕSOURCE	0	RW
3		0 1: 1/1 × ϕSOURCE 1 0: 1/2 × ϕSOURCE 1 1: 1/256 × ϕSOURCE ϕSOURCE: f(XIN) (frequency/2, 4, or 8 mode) f(XCIN) (low-speed mode) f(OCO)/4 (on-chip oscillator mode)	0	RW
4	The values are "0" at reading. If writing to these bits, write "0".		0	RO
5			0	RO
6			0	RO
7			0	RO

Fig. 4.39 Structure of timer Y control register

Interrupt edge selection register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 | | | | | |

Interrupt edge selection register (INTEDGE) [address 003Ah]

b	Name	Functions	After reset	RW
0	INT_0 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
1	INT_1 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
2	INT_2 interrupt edge selection bit	0: Falling edge active 1: Rising edge active	0	RW
3	INT_2/key input interrupt switch bit	0: INT_2 interrupt 1: Key input interrupt	0	RW
4	Timer Y/$CNTR_1$ interrupt switch bit	0: Timer Y interrupt 1: $CNTR_1$ interrupt	0	RW
5	If writing to this bit, write “0”. Do not write “1”.		0	RW
6	The values are "0" at reading. When writing to these bits, write "0".		0	RO
7			0	RO

Fig. 4.40 Structure of interrupt edge selection register

CPU mode register

b7 b6 b5 b4 b3 b2 b1 b0

CPU mode register (CPUM) [address 003Bh]

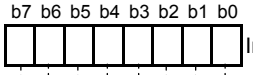
b	Name	Functions	After reset	RW
0	Processor mode bits	b1 b0 0 0: Single-chip mode	0	RW
1		0 1: Do not select. 1 0: Do not select. 1 1: Do not select.	0	RW
2	Stack page selection bit	0: 0 page 1: 1 page	0	RW
3	Internal system clock selection bit	0: Select main clock (including OCO, X_{IN}) 1: Select X_{CIN} - X_{COUT}	0	RW
4	Port X_C switch bit (Note 4)	0: I/O port function (stop oscillating) 1: X_{CIN} - X_{COUT} oscillation function	0	RW
5	X_{IN} - X_{OUT} oscillation stop bit (Note 5)	0: Oscillating 1: Stop oscillating	(Note 1)	RW
6	Main clock division ratio selection bits	0 0: f (X_{IN})/2 (frequency/2 mode) (Note 3) 0 1: f (X_{IN})/8 (frequency/8 mode)	1	RW
7	(Note 2)	1 0: f (X_{IN})/4 (frequency/4 mode) 1 1: On-chip oscillator	(Note1)	RW

Notes: 2. Flash memory version, the OSCSEL pins of the QzROM version = L: 1, the OSCSEL pin of the QzROM version = H: 0.

2. Valid only when internal system clock selection bit (bit 3) is set to "0".
3. 12.5MHz < f(X_{IN}) ≤16MHz is not available in frequency/2 mode.
4. In low-speed mode, the X_{CIN} - X_{COUT} oscillation stops if the port X_C switch bit is set to “0”.
5. In X_{IN} mode, the X_{IN} - X_{OUT} oscillation does not stop even if the X_{IN} - X_{OUT} oscillation stop bit is set to “1”.

Fig. 4.41 Structure of CPU mode register

Interrupt request register 1



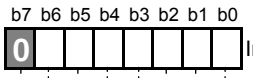
Interrupt request register 1 (IREQ1) [address 003Ch]

b	Name	Functions	After reset	RW
0	INT_0 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
1	INT_1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
2	INT_2/Key input interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
3	$CNTR_0$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
4	Timer X interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
5	Timer 1 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
6	Timer 2 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
7	Timer 3 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)

Note: Each bit can be set to “0” but not to “1” by program.

Fig. 4.42 Structure of Interrupt request register 1

Interrupt request register 2



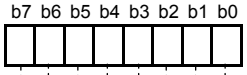
Interrupt request register 2 (IREQ2) [address 003Dh]

b	Name	Functions	After reset	RW
0	Timer 4 interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
1	Serial I/O1 receive interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
2	Serial I/O1 transmit interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
3	Serial I/O2 receive interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
4	Serial I/O2 transmit interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
5	Timer Y/$CNTR_1$ interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
6	AD conversion interrupt request bit	0: No interrupt request issued 1: Interrupt request issued	0	RW (Note)
7	The value is “0” at reading. If writing to this bit, write “0”.		0	RO

Note: Each bit can be set to “0” but not to “1” by program.

Fig. 4.43 Structure of Interrupt request register 2

Interrupt control register 1

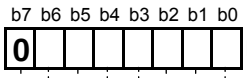


Interrupt control register 1 (ICON1) [address 003Eh]

b	Name	Functions	After reset	RW
0	INT_0 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	INT_1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	INT_2/Key input interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	$CNTR_0$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	Timer X interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	Timer 1 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	Timer 2 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	Timer 3 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW

Fig. 4.44 Structure of Interrupt control register 1

Interrupt control register 2



Interrupt control register 2 (ICON2) [address 003Fh]

b	Name	Functions	After reset	RW
0	Timer 4 interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
1	Serial I/O1 receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
2	Serial I/O1 transmit interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
3	Serial I/O2 receive interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
4	Serial I/O2 transmit interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
5	Timer Y/$CNTR_1$ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
6	AD conversion interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	0	RW
7	If writing to this bit, write “0”. Do not write “1” to this bit.		0	RW

Fig. 4.45 Structure of Interrupt control register 2

LCD display RAM

address		bit 7	6	5	4	3	2	1	0	After reset	RW
		COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0		
0040h	LRAM0	SEG_1				SEG_0				Undefined	RW
0041h	LRAM1	SEG_3				SEG_2				Undefined	RW
0042h	LRAM2	SEG_5				SEG_4				Undefined	RW
0043h	LRAM3	SEG_7				SEG_6				Undefined	RW
0044h	LRAM4	SEG_9				SEG_8				Undefined	RW
0045h	LRAM5	SEG_{11}				SEG_{10}				Undefined	RW
0046h	LRAM6	SEG_{13}				SEG_{12}				Undefined	RW
0047h	LRAM7	SEG_{15}				SEG_{14}				Undefined	RW
0048h	LRAM8	SEG_{17}				SEG_{16}				Undefined	RW
0049h	LRAM9	SEG_{19}				SEG_{18}				Undefined	RW
004Ah	LRAM10	SEG_{21}				SEG_{20}				Undefined	RW
004Bh	LRAM11	SEG_{23}				SEG_{22}				Undefined	RW

Fig. 4. 46 LCD display RAM

Flash memory control register 0

b7 b6 b5 b4 b3 b2 b1 b0

0 Flash memory control register 0 (FMCR0) [address 0FE0h]

b	Name	Functions	After reset	RW
0	RY/$\overline{BY}$ status flag	0: Busy (During automatic writing/erasing) 1: Ready	1	RO
1	CPU rewrite mode select bit (Note 1)	0: CPU rewrite mode invalid 1: CPU rewrite mode valid	0	RW
2	User block 1 E/W enable bit (Notes 1, 2)	0: E/W disabled (1800h - 7FFFh) 1: E/W enabled (1800h - 7FFFh)	0	RW
3	Flash memory reset bit (Notes 3, 4)	0: Flash memory in operation 1: Flash memory reset	0	RW
4	If writing to this bit, write “0”. Do not write “1”.		0	RW
5	User ROM area select bit (Note 5)	0: Access to boot ROM area 1: Access to user ROM area	0	RW
6	Program status flag	0: Ends normally 1: Ends in error	0	RO
7	Erase status flag	0: Ends normally 1: Ends in error	0	RO

Notes. 1. In order to set this bit to "1", write this bit to "1" continuously after writing "0" .
In order to set this bit to "0", write this bit to "0" .
2. This bit can be written only when the CPU rewrite mode select bit is set to "1".
3. The flash memory can be reset only when the CPU rewrite mode select bit (bit 1) is set to "1".
Fix this bit to "0" when the CPU rewrite mode select bit is set to "0".
4. When this bit is set to "1" (reset the flash memory control circuit), access to the flash memory is impossible for 10 μs.
5. Write to this bit by program on the RAM.
6. This register is only in the flash memory version.

Fig.4.46 Structure of Flash memory control register 0

Flash memory control register 1

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0 0 Flash memory control register 1 (FMCR1) [address 0FE1h]

b	Name	Functions	After reset	RW
0	Erase suspend enable bit (Note 1)	0: Suspend invalid 1: Suspend valid	0	RW
1	Erase suspend request bit (Note 1)	0: Erase restart (No request) 1: Erase suspend (Request issued)	0	RW
2	If writing to this bit, write “0”. Do not write “1”.		0	RO
3			0	RO
4			0	RO
5			0	RO
6	Erase suspend flag	0: Erase active 1: Erase inactive (Erase suspend mode)	1	RO
7	If writing to this bit, write “0”. Do not write “1”.		0	RW

Notes: 1. In order to set this bit to "1", write this bit to "1" continuously after writing "0" .
In order to set this bit to "0", write this bit to "0" .
2. Valid only when the erase suspend enable bit (bit 0) is set to "1".
3. This register is only in the flash memory version.

Fig.4.47 Structure of Flash memory control register 1

Flash memory control register 2

b7	b6	b5	b4	b3	b2	b1	b0
0	1	0		0	1	0	1

Flash memory control register 2 (FMCR2) [address 0FE2h]

b	Name	Functions	After reset	RW
0	If writing to this bit, write “1”. Do not write “0”.		1	RO
1	If writing to this bit, write “0”. Do not write “1”.		0	RO
2	If writing to this bit, write “1”. Do not write “0”.		1	RO
3	If writing to this bit, write “0”. Do not write “1”.		0	RO
4	User block 0 E/W enable bit (Notes 1, 2)	0: E/W disabled (8000h - FFFFh) 1: E/W enabled (8000h - FFFFh)	0	RW
5	If writing to this bit, write “0”. Do not write “1”.		0	RO
6	If writing to this bit, write “1”. Do not write “0”.		1	RO
7	If writing to this bit, write “0”. Do not write “1”.		0	RO

Notes: 1. In order to set this bit to "1", write this bit to "1" continuously after writing "0" .
In order to set this bit to "0", write this bit to "0" .
2. This bit can be written only when the CPU rewrite mode select bit (bit 1 in the flash memory control register 0 (address 0FE0h)) is set to "1"
3. This register is only in the flash memory version.

Fig.4.48 Structure of Flash memory control register 2

PULL register

b7 b6 b5 b4 b3 b2 b1 b0

0 | | | | | | | | PULL register (PULL) [address 0FF0h]

b	Name	Functions	After reset	RW
0	$P3_0$ to $P3_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
1	$P3_4$ to $P3_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
2	$P4_0$ to $P4_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
3	$P4_4$ to $P4_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
4	$P5_0$ to $P5_3$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
5	$P5_4$ to $P5_7$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
6	$P6_0$ to $P6_2$ pull-up control bit	0: No pull-up 1: Pull-up	0	RW
7	The value is “0” at reading. If writing to this bit, write “0”.		0	RO

Note: In port(s) set to output mode, each corresponding bit becomes invalid and pull-up register is not connected.

Fig. 4.47 Structure of PULL register

UART2 control register

b7 b6 b5 b4 b3 b2 b1 b0

1 1 1 | | | | | | UART2 control register (UART2CON) [address 0FF1h]

b	Name	Functions	After reset	RW
0	Character length selection bit (CHAS)	0: 8 bits 1: 7 bits	0	RW
1	Parity enable bit (PARE)	0: Parity checking disabled 1: Parity checking enabled	0	RW
2	Parity selection bit (PARS)	0: Even parity 1: Odd parity	0	RW
3	Stop bit length selection bit (STPS)	0: 1 stop bit 1: 2 stop bits	0	RW
4	$P3_2$/TxD_2 P-channel output disable bit (POFF)	In output mode 0: CMOS output 1: N-channel open drain output In input mode, this bit is invalid.	0	RW
5	The values are “1” at reading. If writing to these bits, write “1”.		1	RO
6			1	RO
7			1	RO

Fig. 4.48 Structure of UART2 control register

Baud rate generator 2

b7 b6 b5 b4 b3 b2 b1 b0

Baud rate generator 2 (BRG2) [address 0FF2h]

b	Functions	After reset	RW
0	Set the frequency divide value of BRG count source.	Undefined	RW
1	Baud rate generator divides the frequency of the count source by (n + 1)	Undefined	RW
2	when n is the value written to BRG.	Undefined	RW
3		Undefined	RW
4		Undefined	RW
5		Undefined	RW
6		Undefined	RW
7		Undefined	RW

Note: Write to this register only while transmit/receive operation is stopped.

Fig. 4.49 Structure of Baud rate generator 2

Clock output control register

b7 b6 b5 b4 b3 b2 b1 b0

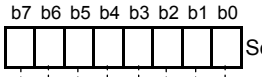
0 0 0 0 0 0 0 _

Clock output control register (CKOUT) [address 0FF3h]

b	Name	Functions	After reset	RW
0	$P3_6$ clock output control bit	0: Timer 2 output 1: System clock ϕ output	0	RW
1	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
2			0	RO
3	If writing to these bits, write “0”. Do not write “1”.		0	RW
4			0	RW
5			0	RW
6			0	RW
7			0	RW

Fig. 4.50 Structure of Clock output control register

When port P0 direction register is in output mode:
Segment output disable register 0

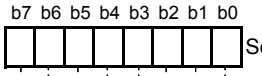


Segment output disable register 0 (SEG0) [address 0FF4h]

b	Name	Functions	After reset	RW
0	Segment output disable bit 0	0: Segment output SEG_0 1: Output port $P0_0$	1	RW
1	Segment output disable bit 1	0: Segment output SEG_1 1: Output port $P0_1$	1	RW
2	Segment output disable bit 2	0: Segment output SEG_2 1: Output port $P0_2$	1	RW
3	Segment output disable bit 3	0: Segment output SEG_3 1: Output port $P0_3$	1	RW
4	Segment output disable bit 4	0: Segment output SEG_4 1: Output port $P0_4$	1	RW
5	Segment output disable bit 5	0: Segment output SEG_5 1: Output port $P0_5$	1	RW
6	Segment output disable bit 6	0: Segment output SEG_6 1: Output port $P0_6$	1	RW
7	Segment output disable bit 7	0: Segment output SEG_7 1: Output port $P0_7$	1	RW

Fig. 4.51 Structure of Segment output disable register 0

When port P1 direction register is in output mode:
Segment output disable register 1



Segment output disable register 1 (SEG1) [address 0FF5h]

b	Name	Functions	After reset	RW
0	Segment output disable bit 8	0: Segment output SEG_8 1: Output port $P1_0$	1	RW
1	Segment output disable bit 9	0: Segment output SEG_9 1: Output port $P1_1$	1	RW
2	Segment output disable bit 10	0: Segment output SEG_{10} 1: Output port $P1_2$	1	RW
3	Segment output disable bit 11	0: Segment output SEG_{11} 1: Output port $P1_3$	1	RW
4	Segment output disable bit 12	0: Segment output SEG_{12} 1: Output port $P1_4$	1	RW
5	Segment output disable bit 13	0: Segment output SEG_{13} 1: Output port $P1_5$	1	RW
6	Segment output disable bit 14	0: Segment output SEG_{14} 1: Output port $P1_6$	1	RW
7	Segment output disable bit 15	0: Segment output SEG_{15} 1: Output port $P1_7$	1	RW

Fig. 4.52 Structure of Segment output disable register 1

When port P2 direction register is in output mode:
Segment output disable register 2

b7 b6 b5 b4 b3 b2 b1 b0

Segment output disable register 2 (SEG2) [address 0FF6h]

b	Name	Functions	After reset	RW
0	Segment output disable bit 16	0: Segment output SEG_{16} 1: Output port $P2_0$	1	RW
1	Segment output disable bit 17	0: Segment output SEG_{17} 1: Output port $P2_1$	1	RW
2	Segment output disable bit 18	0: Segment output SEG_{18} 1: Output port $P2_2$	1	RW
3	Segment output disable bit 19	0: Segment output SEG_{19} 1: Output port $P2_3$	1	RW
4	Segment output disable bit 20	0: Segment output SEG_{20} 1: Output port $P2_4$	1	RW
5	Segment output disable bit 21	0: Segment output SEG_{21} 1: Output port $P2_5$	1	RW
6	Segment output disable bit 22 (Note)	0: Segment output SEG_{22} 1: Output port $P2_6$	1	RW
7	Segment output disable bit 23 (Note)	0: Segment output SEG_{23} 1: Output port $P2_7$	1	RW

Note: When VL pin input selection bit (bit 5 at LCD power control register (address 0014h)) is set to "1", these bits become invalid.

Fig. 4.53 Structure of Segment output disable register 2

When port Pj (j = 0 to 2) direction register is in input mode:
Segment output disable register i (i = 0 to 2)

b7 b6 b5 b4 b3 b2 b1 b0

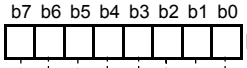
Segment output disable register i (SEGi) (i = 0 to 2) [addresses 0FF4h, 0FF5h, 0FF6h]

b	Name	Functions	After reset	RW
0	Port Pi_0 Pull-up control	0: No pull-up 1: Pull-up	1	RW
1	Port Pi_1 Pull-up control	0: No pull-up 1: Pull-up	1	RW
2	Port Pi_2 1. When the on-chip oscillator is se	0: No pull-up 1: Pull-up	1	RW
3	Port Pi_3 Pull-up control	0: No pull-up 1: Pull-up	1	RW
4	Port Pi_4 Pull-up control	0: No pull-up 1: Pull-up	1	RW
5	Port Pi_5 Pull-up control	0: No pull-up 1: Pull-up	1	RW
6	Port Pi_6 Pull-up control	0: No pull-up 1: Pull-up	1	RW
7	Port Pi_7 Pull-up control	0: No pull-up 1: Pull-up	1	RW

Note: When VL pin input selection bit (bit 5 at LCD power control register (address 0014h)) is set to "1", settings of $P2_6$ and $P2_7$ become invalid.

Fig. 4.54 Structure of Segment output disable register i (i = 0 to 2)

Key input control register



Key input control register (KIC) [address 0FF7h]

b	Name	Functions	After reset	RW
0	$P5_4$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
1	$P5_5$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
2	$P5_6$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
3	$P5_7$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
4	$P0_0$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
5	$P0_1$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
6	$P0_2$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW
7	$P0_3$ key input control bit	0: Key input interrupt disabled 1: Key input interrupt enabled	0	RW

Fig. 4.55 Structure of Key input control register

ROM correction address 1 high-order register
ROM correction address 1 low-order register

b7 b6 b5 b4 b3 b2 b1 b0

ROM correction address 1 high-order register (RCA1H) [address 0FF8h]

ROM correction address 1 low-order register (RCA1L) [address 0FF9h]

b	Functions	After reset	RW
0	Set the start address of the program to be corrected.	0	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Notes: 1. Specify the start address of each instruction (Op code address) as ROM correction address.
2. Do not set any addresses other than those located in ROM area to ROM correction address registers. Do not set the same addresses to both ROM correction address 1 registers and ROM correction address 2 registers.

Fig. 4.56 Structure of ROM correction address 1 high-order register and ROM correction address 1 low-order register

ROM correction address 2 high-order register
ROM correction address 2 low-order register

b7 b6 b5 b4 b3 b2 b1 b0

ROM correction address 2 high-order register (RCA2H) [address 0FFAh]

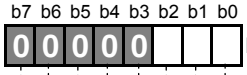
ROM correction address 2 low-order register (RCA2L) [address 0FFBh]

b	Functions	After reset	RW
0	Set the start address of the program to be corrected.	0	RW
1		0	RW
2		0	RW
3		0	RW
4		0	RW
5		0	RW
6		0	RW
7		0	RW

Notes: 1. Specify the start address of each instruction (Op code address) as ROM correction address.
2. Do not set any addresses other than those located in ROM area to ROM correction address registers. Do not set the same addresses to both ROM correction address 1 registers and ROM correction address 2 registers.

Fig. 4.57 Structure of ROM correction address 2 high-order register and ROM correction address 2 low-order register

ROM correction enable register



ROM correction enable register (RCR) [address 0FFCh]

b	Name	Functions	After reset	RW
0	ROM correction address 1 enable bit (RC0)	0: Disabled 1: Enabled	0	RW
1	ROM correction address 2 enable bit (RC1)	0: Disabled 1: Enabled	0	RW
2	ROM correction memory selection bit (RC2)	0: Branch to RAM area 1: Branch to ROM area	0	RW
3	The values are “0” at reading. If writing to these bits, write “0”.		0	RO
4			0	RO
5			0	RO
6			0	RO
7			0	RO

Note: When using ROM correction function, make sure to enable address enable bits after setting ROM correction address registers.

Fig. 4.58 Structure of ROM correction enable register

5. Reference

Datasheet
38D2 Group Datasheet
(Use the most recent version of the document on the Renesas Technology Website.)

Technical News/Technical Update
(Use the most recent version of the document on the Renesas Technology Website.)

Website and Support

Renesas Technology Corporation website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
csc@renesas.com

REVISION HISTORY	38D2 Group List of Registers

Rev.	Date	Description	
		Page	Summary
1.00	Jan 17, 2007	—	First edition issued
2.00	April 20, 2007	5	Figure 4.6 CPU mode register 2: Notes revised
		27	Figure 4.36 Compare register 1, 2, 3(low-order, high-order): Notes revised
		31	Figure 4.41 CPU mode register: Notes revised
		35, 36	Figures 4.46 to 48 Flash memory control registers added.
4.00	Aug 08, 2007	5	Figure 4.6 CPU mode register 2: Note 1 revised
		29	Figure 4.38 Bits 1 and 0 in timer Y mode register: revised
		31	Figure 4.41 CPU mode register: Notes 4 and 5 added

Notes regarding these materials

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (http://www.renesas.com)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guaranties regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
   (1) artificial life support devices or systems
   (2) surgical implantations
   (3) healthcare intervention (e.g., excision, administration of medication, etc.)
   (4) any other purposes that pose a direct threat to human life
   Renesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.