Introduction

This application note provides an overview of PCI Express (PCIe) reference clocking for Generations 1, 2 and 3. PCIe is a major architecture improvement over the parallel half-duplex PCI bus to a dual-simplex serial bus. This was designed to increase data throughput while minimizing the number of bus IO pins for PCs. The first generation, introduced in 2005, operated at a 2.5GBit/sec raw data rate with 8B/10B encoding for an effective data rate of 2GBit/sec. Generation 2 was introduced in 2006 and extended the raw data rate to 5Gbit/sec, also with 8B/10B encoding for an effective bit rate of 4 Gbit/sec. Generation 3 was finalized in 2010 and supports a raw bit rate of 8Gbit/Sec but using scrambling with 129B/130B encoding for an effective bit rate of 7.88Gbit/sec.

Three PCI Special Interest Group (PCISIG) documents were used as the basis for this document. The first document is a white paper, *PCI Express Jitter and BER, Revision 1.0*, which provides background information regarding the following three important factors that define the link BER. The first factor, jitter, is partitioned into a random Gaussian components, Root Sum Squares (RSS) Dj and a deterministic component, Dj. These two different types of jitter are summed in accordance with the Double Delta function method. Second, a bit error is defined "… as the accumulation of phase jitter, y, such that the total phase difference between the data and the sampling clock exceeds ½ the unit interval (UI)." Third is a simple link phase noise model to define the random and deterministic components of the jitter budget.

The link phase noise model is developed to define the random and deterministic components of the jitter budget and a procedure to measure the jitter of a specific link. Compliance of a particular RefClock with the PCIe jitter specifications has been further developed from this initial white paper and is determined indirectly through a three-step process. First a phase transfer function model for the particular clock architecture is defined. Second the phase noise at the model output is calculated when driven by a particular RefClock oscillator phase noise spectrum. Third the model output jitter spectrum is processed for comparison to the PCIe high and low band specs. For rms jitter the phase noise is integrated over the appropriate frequency bands. For peak-to-peak jitter the filtered clock spectrum must be transformed back into the time domain to find the two specific instants at which the eye closure function deviates to the positive and negative phase extremes.

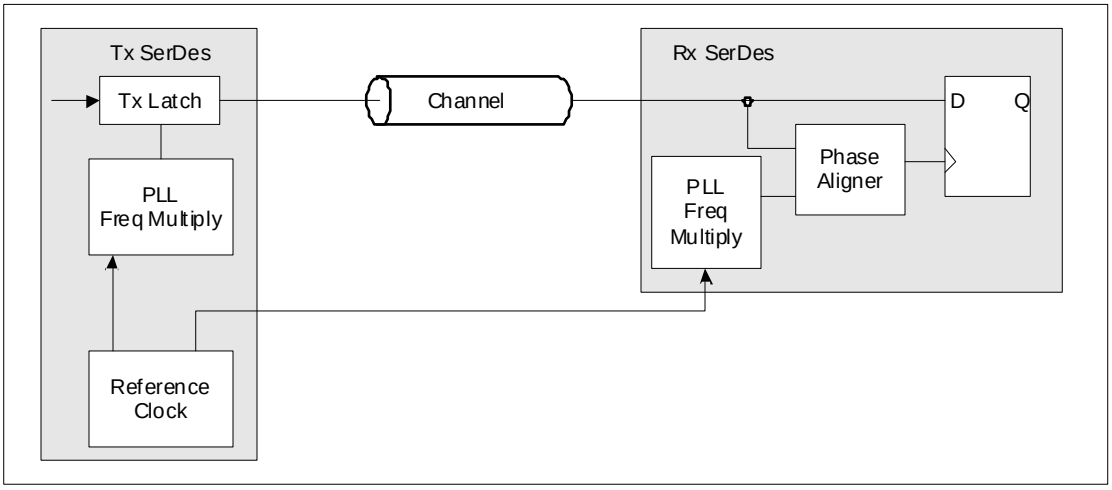
The second document is the *CARD ELECTROMECHANICAL SPECIFICATION, REV. 2.0*, which provides the Gen 1 reference clock architectures, modeling parameters and requirements. Third is the *PCI Express BASE SPECIFICATION, REV. 3.0*, which contains the reference clock architectures, modeling parameters and requirements for Gen 2 and Gen 3.

This note is concerned only with the jitter requirements for the Reference Clock partition of the jitter budget and its associated jitter transfer model. PCISIG has made an effort to maintain the phase noise performance requirements on the Reference Clock oscillator as each new PCIe generation has been introduced. The objective is to minimize the design effort necessary to guarantee jitter compliant Reference Clock designs, which places the bulk of the low noise design burden on the PCIe transmitters and receivers.

PCIe Reference Clock Architectures

PCIe defines three types of clocking architectures: Common Clock, Data Clock and Separate Clock which are depicted in the figures below.

Figure 1. Common Clock Architecture



This document is focused on the Common clock architecture which is described in detail in Section *Common Clock Architecture*. The Common Clock architecture results in the lowest cost while simply and robustly implementing Spread Spectrum Clocking (SSC), which is described in Section *Spread Spectrum Clocking*.

Figure 2. Physical Implementation of Common Clock Architecture

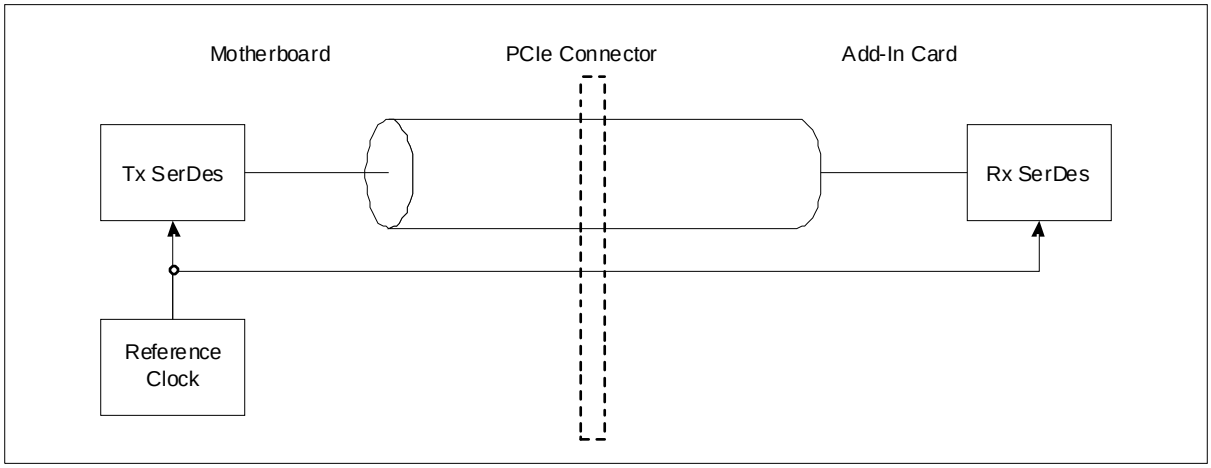
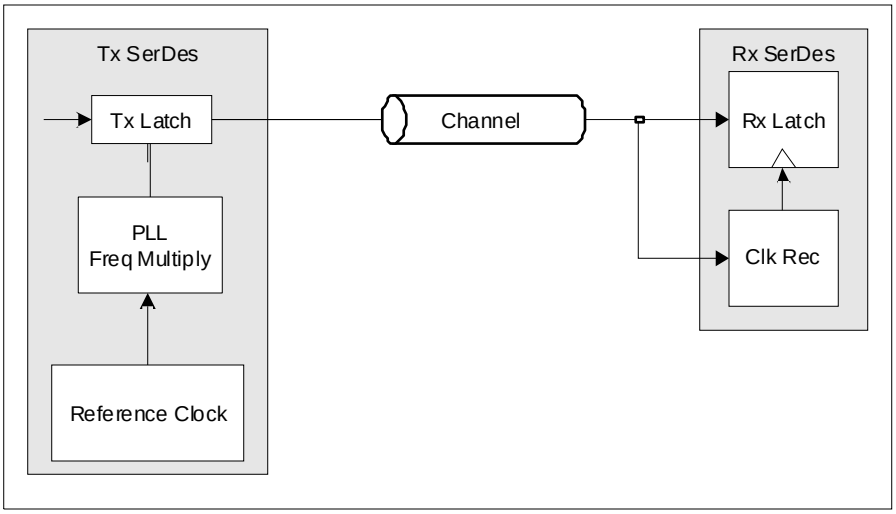


Figure 2 above shows a physical implementation of the common clock architecture. The Reference clock is fanned out to both the motherboard Tx serializer/deserializer (serdes) and the add-in card Rx serdes. Nominally there is no relative phase difference between the data embedded clock and the receiver data latch clock. This lack of relative phase difference between the data embedded clock and the Rx data latch clock makes the Common Clock architecture relatively impervious to transmission errors when the Reference clock spectrum is spread. The PCI Express Jitter and BER white paper reviews that bit errors only result when there is eye closure via the relative mis-alignment of the data embedded clock and the receiver reference clock that exceeds ½ of a UI.

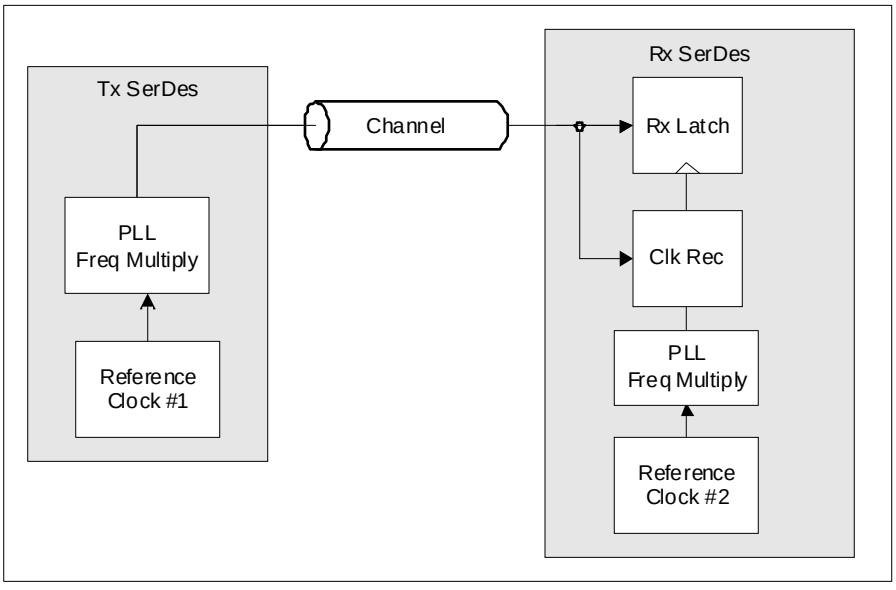
The Data Clocked architecture, shown below is specified at 5.0 Gb/S in Section 4.3.7.3.4. and at 8.0 Gb/S in Section 4.3.8.3. of *PCI Express BASE SPECIFICATION, REV. 3.0*. This is a much simpler architecture, but has poorer jitter performance since the H2 and H3 filtering functions are excluded.

Figure 3. Data Clock Architecture



The Separate Clock architecture for 5.0 Gb/S is covered in Section 4.3.7.4. and at 8.0Gb/s in Section 4.3.8.4 of *PCI Express BASE SPECIFICATION, REV. 3.0*. It is recommended to consult these sections of this document for further information such as transfer functions. The unattractive feature of this architecture is that a separate Refclk adapter will not interoperate with a root complex driving data with SSC. Separate clock architecture will therefore work only if SSC is turned off on both the root and adapter clocks. Further the frequency mismatch due to the tolerances of the separate clocks further degrades link BER margin.

Figure 4. Separate Clock Architecture

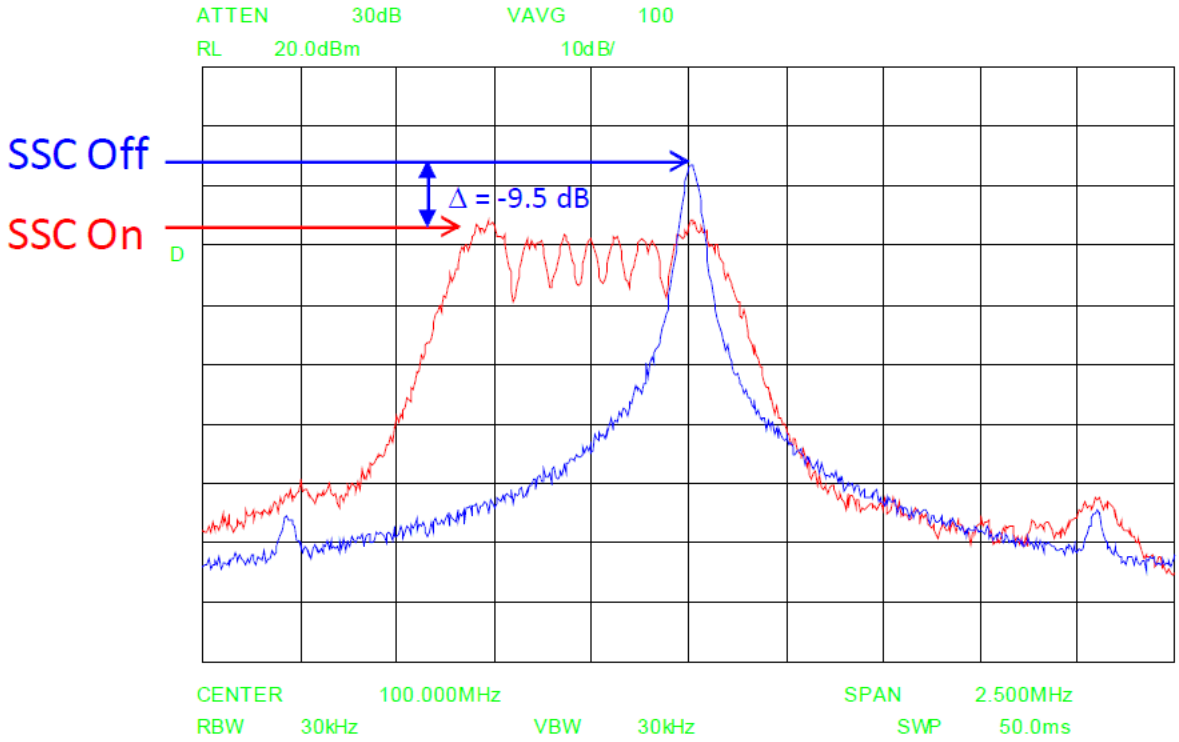


Spread Spectrum Clocking

PCIe provides the option to modulate the spectrum of the reference clock at a rate of 30kHz – 33kHz and a magnitude between 0% and -0.5%. As the Reference Clock is a single frequency and EMI constraints are on the maximum radiated power at any frequency rather than total power in a frequency band, spreading distributes the total clock power across multiple frequencies. The fact that this also spreads the data is irrelevant for EMI purposes because data modulation fully fills the spectrum before the embedded clock is spread.

The spectrum analyzer plot of Figure 5 shows how SSC reduces peaking. The blue plot shows the clock spectrum with SSC turned off and the red plot shows SSC turned on. Note that the modulation primarily reduces the clock frequency. This is done to avoid increasing the instantaneous bit rate and incurring a BER penalty through a reduction in timing margin.

Figure 5. Spread Spectrum Clock Modulation



Since the Refclock phase noise sensitivity of the three architectures are different, it is not possible to specify one phase noise profile for the RefClock oscillator with the spread spectrum option that will guarantee satisfactory data link performance for all architectures; to do so would overly constrain the Refclock.

Beginning in Gen 2.0, PCIe specified the jitter requirements by Refclock architecture and jitter frequency band to relax the Refclock requirements. Spread spectrum jitter is deliberately generated at low frequencies that are within the jitter tracking range of the receiver data recovery, which leads to a natural partition of the Refclock jitter into two frequency regions; a low band and a high band. The low band jitter requirement is impressed between 10kHz to 1.5MHz. The high frequency jitter band is between 1.5MHz and the Nyquist rate of 50MHz and limits the intrinsic jitter of the reference clock for frequencies that the data recovery cannot filter. These bands are used to separate the requirements for EMI and jitter compliance specification because spread spectrum frequency modulation is below 1.5MHz, typically between 30-33kHz, and the data Tx, Rx and CR PLL bandwidths range from 1.5MHz - 22MHz.

Common Clock Architecture

The PCI Express physical architecture that accomplishes the transmission and reception is shown in Figure 6.

Figure 6. Physical Link Jitter Architecture

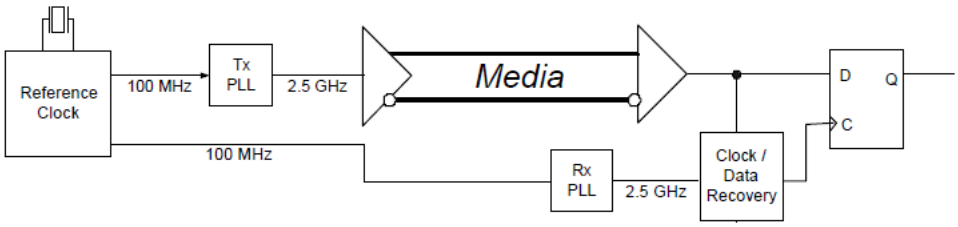
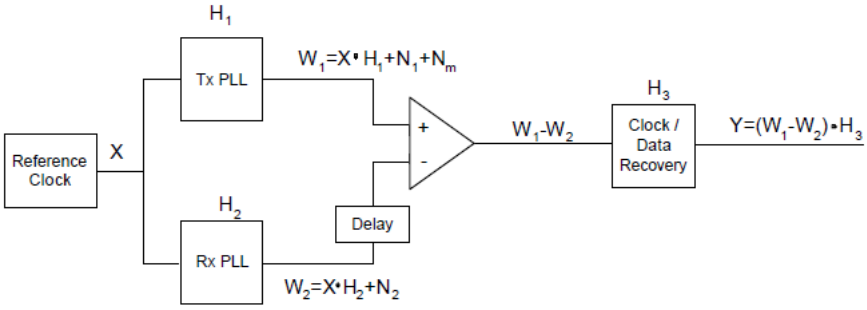


Figure 7. Equivalent Common Clock Phase Noise Transfer Function



The calculation of the displacement between the center of the data eye and the sampling clock is illustrated with a mathematical equivalent model of the link. In Figure 3, the reference clock (100MHz) phase jitter, X, is sent to both the transmitter and the receiver. Each device has it's own phase transfer function and injects some amount of phase jitter that is independent of the reference clock jitter. This is shown in Figure 3 as N1 and N2. The media (traces on the PCB, cable s, and connectors) adds some additional phase jitter due to the effects of dispersion, ISI, crosstalk and reflections. Finally, there is a delay between the two paths of the Tx and the reference clock that causes X to add to Y, due to the fixed phase offset. Since N2 is already uncorrelated this delay acts only on H2 and does not amplify N2. Moving forward, we will assume that the delay has been absorbed into the phase transfer function of H2.

As shown in Figure 3, the phase mismatch at the receiver, Y, between the center of the data eye and the sampling clock is given by equation (1). In the time domain, y is the time difference between the edge of the data and the edge of the sampling clock and is the eye closure. See *PCI Express™ Jitter and BER Revision 1.0* for further details.

Figure 7 above is the phase transfer function used to both model and specify clock performance by PCIe. The development of this equivalent model from a physical model of a PCIe link with observations targeted to developing a more physical understanding of jitter propagation in the Common Clock architecture is contained in Section, “Appendix 1–Derivation of Equivalent Phase Transfer Function”.

Filtering Functions Applied to the Common Refclk Architecture

High Band Model Parameters

Gen 1–2.5Gb/S

The model parameters in Table 1 below are from the CEM 2.0, page 21, Section 2.1.4. There is only one transfer function that is applied to the reference clock. The bandwidth of H1 is about 15X that of H2, which is very different from Gen 2 and Gen 3, where the bandwidth of H2 is greater than H1. SSC separation is performed exclusively by H3. Gen 2 and Gen 3 specify the H1 and H2 PLL in terms of Natural Frequency and damping factor. Gen 1 specifies the H1 and H2 PLL in terms of -3dB bandwidth and damping factor.

Unlike the Reference Clock model used for Gen 2 and Gen 3, the Differential Transport Delay in Gen 1 is considered as being in the Rx PLL path as below.

$$H_{CC}(s) = H3(s)\left[H1(s) - H2(s)e^{-sT}\right]$$

Table 1: Gen 1 Jitter Model Parameters

Model Element	-3db Frequency (MHz)	Peaking (dB)	Natural Frequency (MHz)	Damping Factor	High Pass	Time (nS)
H1 $_{22\_3}$	22.0	3.0	11.83	0.54		
H2 $_{1.5\_3}$	1.5	3.0	0.81	0.54		
H3					$\frac{s}{s + 2\pi * 1.5\text{MHz}}$	
Transport Delay*						10

* Gen 2 and 3 spec 12 nS, but this 12 nS spec includes 2nS internal to the Tx and Rx functions. This leaves 10 nS for the device pin to device pin delay.

Gen 2–5.0 Gb/S

H1, H2 and T jitter model parameters in Table 2 below are from the PCI EXPRESS BASE SPECIFICATION, REV. 3.0 page 404. The H3 specification is from the March 4, 2009 Base Specification 2.1, Section 4.3.3.1 on page 266. The output of the jitter model is separated by the SSC Filtering functions described in Section, “Low Band Model Parameters”.

Table 2: Gen 2 Jitter Model Parameters

Model Element	-3db Frequency (MHz)	Peaking (dB)	Natural Frequency (MHz)	Damping Factor	High Pass	Time (nS)
H1 $_{5\_1}$ H1 $_{8\_3}$	5.0 8.0	1.0 3.0	1.82 4.31	1.16 0.54		
H2 $_{16\_3}$ H2 $_{23\_1}$ H2 $_{32\_0.5}$	16.0 23.6 32.6	3.0 1.0 0.5	8.61 8.61 8.61	0.54 1.16 1.75		
H3					If(f $\geq$ 1.5 MHz) then 1 else 10^{-3}	
Transport Delay*						12

For any given Refclock, the worst-case total jitter occurs when Hcc has the widest bandwidth and that bandwidth coincides with the frequencies of largest Refclock jitter spectral density. Since H1 is the smaller bandwidth PLL transfer function and H2 is the larger PLL bandwidth function, this will occur when H1 is at its minimum bandwidth and H2 is at its maximum bandwidth. The natural frequency of H2 is specified at 8.61MHz, but the H2 damping factor can be between 0.54 and 1.75. Smaller damping factors emphasize lower frequencies through greater peaking at the natural frequency. Larger damping factors at the same natural frequency reduce peaking but extend the -3dB frequency of the PLL.

It is expected that all three H2 transfer functions should be considered when forming the PLL difference function because the total jitter under the mask will depend on the product of the clock phase noise density and the frequency mask. Since this requires any given clock to be measured with all masks to find the worst case mask for the particular clock, the selection of masks to use for this document is determined on the basis of the masks with highest noise equivalent bandwidth.

It should also be noted that IDT did not agree with the PCISIG procedure of essentially deleting the SSC modulation components in 5 Gb/s signaling. A real system does not delete the SSC modulation components; rather it responds to the SSC modulation. It was our position that the system transfer function correctly weights the effects of SSC and that the SSC components should be retained like in 2.5 Gb/s signaling. The end result would not be that much different because the system is indeed rather

insensitive to low frequency modulation components like SSC (because they are almost equally tracked by Tx and Rx), but the issue at hand in this case is to avoid compounding the limitations of a basic model by an additional approximation.

Gen 3–8.0 Gb/S

The Base Specification, Rev 3.0, Section 4.3.8.2, page 409 defines the Tx and Rx PLL bandwidth for 8.0 GT/s signaling as between 2 – 5MHz. As shown below, peaking may be from 0 to 2 dB for bandwidths up to 4MHz and 0 to 1 dB for bandwidths up to 5MHz. The 8.0 GT/s PLL BW range is substantially lower than the PLL bandwidths specified for 5.0 GT/s or 2.5 GT/s operation to reduce the amount of Refclock jitter at the sample latch of the receiver. H3 is specified in Section 4.3.4.3.4 on pdf page 369.

Table 3: Gen 3 Jitter Model Parameters

Model Element	-3db Frequency (MHz)	Peaking (dB)	Natural Frequency (MHz)	Damping Factor	High Pass	Time (nS)
H1 2_.01 H1 2_2 H1 4_.01 H1 4_2	2.2 2.0 3.9 4.0	0.01 2.0 0.01 2.0	0.078 0.96 0.14 1.92	14 0.73 14 0.73		
H2 2_.01 H2 2_1 H2 5_.01 H2 5_1	2.2 2.0 5.0 5.0	0.01 1.0 0.01 1.0	0.078 0.74 0.18 1.84	14 1.15 14 1.15		
H3					$\frac{s}{s+2\pi*10MHz}$	
Transport Delay						12

It is recommended by PCISIG that "*when characterizing TREFCLK-RMS-CC it is recommended that all unique combinations of bandwidth and peaking be included when computing H(s) and H'(s)*." The SSC Filtering functions are also to be applied. Table 3 above defines fifteen unique pairs of H1-H2 pairs of transfer functions. When T is included there are thirty unique transfer functions.

Since in general a PCIe link is full duplex, there is another half duplex link to model carrying data in the opposing direction. If the Transport delay is assigned as being in H1 in one direction, then the same delay should be assigned to the H2 leg in the opposite direction.

Low Band Model Parameters

As discussed previously, jitter is classified by PCISIG into to a low frequency band for Refclock SSC jitter and a high frequency band for Refclock jitter that closes the eye at the receiver data latch. For Gen 1, this separation was done exclusively by the high pass characteristic of Hcc.

For Gens 2 and 3, separate filters are explicitly defined and used to separate the bands. These filters remove the spread spectrum components of the Refclock jitter before the H1, H2 and H3 transfer functions are applied. In addition, Gens 2 and 3 use multiple transfer functions for H1 and H2 and define different functions for H3. The designer is to test with specific combinations of these filters to ensure compliance.

The Common Clock architecture filters for Gens 2 and 3 are as follows.

1. **SSC separation:** A 1.5 MHz brick wall low pass used to remove the low frequency band containing the SSC components from the Refclock spectrum, allowing one to define separate low frequency Rj and low frequency Dj components.
2. **0.01- 1.5 MHz step BPF:** If (f < 10kHz) then 10-3, elseif (f<1.5MHz) then 1.0, else 10-3.

   The lower edge of filter, below 10k, removes 1/f jitter contributions that are completely trackable by the CDR. The stop band above 1.5MHz removes high frequency jitter components.
3. **1.5 MHz HPF:** This is H3. It removes the low frequency jitter components that are trackable by the CDR, allowing one to define those jitter components not trackable by the CDR.
4. **PLL difference functions:** The between Tx and Rx PLLs and the impact of T, the transport delay. Different PLL models are used to characterize different cases of PLL mismatch.
5. **Edge filtering:** Minimizes test equipment measurement artifacts caused by finite sampling/voltage resolution aperture. This is a voltage averaging process that is applied at a frequency of 5 or 8 GHz and is used in the post processing of the raw Refclock data as part of the de-embedding procedure.

These filters are applied in accordance with the following table.

Table 4: Gen 2 and 3 Jitter Filter Functions

Band	Applied Filters
Low (<1.5MHz, SSC)	SSC Separation PLL Difference functions 0.01 –1.5MHz Step BPF
High (> 1.5MHz, Tracking Data Eye)	PLL Difference functions H3 HPF Edge Filtering

Reference Clock Compliance Parameters

Gen 1–2.5Gb/S

Table 2-2: Maximum Allowed Phase Jitter When Applied to Fixed Filter Characteristic

BER[2]	Maximum Peak-Peak Phase Jitter Value (ps)
10^{-6}	86
10^{-12}	108

Gen 2–5.0 Gb/S

PCI EXPRESS BASE SPECIFICATION, REV. 3.0

4.3.7.3.3. Compliance Parameters for Common Refclk Rx Architecture

Table 4-31 defines the compliance parameters for the common Refclk Rx architecture.

Table 4-31: Refclk Parameters for Common Refclk Rx Architecture at 5.0 GT/s

Symbol	Description	Limits		Units	Note
		Min	Max		
$T_{REFCLK-HF-RMS}$	> 1.5 MHz to Nyquist RMS jitter after applying Equation 4.3.3		3.1	ps RMS	1
$T_{REFCLK-SSC-RES}$	SSC residual		75	ps	1
$T_{REFCLK-LF-RMS}$	10 kHz - 1.5 MHz RMS jitter		3.0	ps RMS	2
$T_{SSC-FREQ-DEVIATION}$	SSC deviation		+0.0/-0.5	%	
$T_{SSC-MAX-PERIOD-SLEW}$	Maximum SSC df/dt		0.75	ps/UI	3

Notes:

1. $T_{REFCLK-HF-RMS}$ is measured at the far end of the test circuit illustrated in Figure 4-88 after the filter function defined in Table 4-29 for Common Refclk Rx for >1.5 MHz jitter components has been applied.
2. $T_{REFCLK-SSC-RES}$ and $T_{REFCLK-LF-RMS}$ are measured after the filter function defined in Table 4-29 for Common Refclk Rx for >1.5 MHz jitter components has been applied.

Gen 3–8.0 Gb/S

PCI EXPRESS BASE SPECIFICATION, REV. 3.0

Table 4-34: Parameters for Common Refclk Rx Architecture at 8.0 GT/s

Symbol	Description	Limits		Units
		Min	Max	
F_{REFCLK}	Refclk frequency[1]	99.97	100.03	MHz
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk Rx architecture[3]		1.0	ps RMS
F_{SSC}	SSC frequency range	30	33	kHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation[2]		+0.0/-0.5	%
$T_{TRANSPORT-DELAY}$	Tx-Rx transport delay	12		ns

Notes:

1. Before application of SSC.
2. It is sufficient to define SSC deviation only without specifying anything about the shape of the modulation envelope. Envelopes with very large df/dt will fail the $T_{REFCLK-RMS-CC}$ parameter.
3. The Refclk jitter is measured after applying the jitter filtering function defined in Figure 4-93.

Jitter Limits

Gen 1–.5 Gb/s

The total system jitter budget is 399.13ps which is approximately one unit interval (1/2.5GHz = 400ps) which cannot be exceeded more that once every 10^{12} cycles. The clock gets approximately 1/4 of the system budget–108ps to be exact. This number is an accumulated peak-peak phase jitter which has been filtered by the system transfer function as previously discussed in Section, “Reference Clock Compliance Parameters”. Because the clock phase information must be collected to verify compliance, real-time oscilloscopes are normally used but they have limited memory depth, which makes evaluation of a 10^{12} sample periods impossible. Therefore, a specification of 86ps peak-to-peak phase jitter is provided for a smaller sample size of 10^6 samples. This scaling of 108ps peak-to-peak for 10^{12} samples to 86ps peak-to-peak for 10^6 samples assumes a Gaussian random jitter distribution. But even 10^6 samples can be an overly large sample set for the memory depth of many real time oscilloscopes, so it is acceptable to obtain this sample set over multiple acquisitions, the sum of which must total at least 10^6 samples. The highest observed filtered peak-to-peak accumulated phase jitter across the multiple acquisitions is reported.

Table 5: PCI Express Clock Phase Jitter Limits, 2.5 Gb/s[1]

	10^{12} Samples	10^6 Samples
Max Phase Jitter	108ps	86ps

1. Peak-to-Peak phase jitter after application of the system transfer function

For reference purposes, the Table 6 is an excerpt from Table 4-3 of CEM 2.0 showing jitter budgets of the system components, including the reference clock.

Table 6: Total System Jitter Budget, 2.5 Gb/s

Jitter Contribution	Random Jitter Rj ps	Deterministic Jitter Dj ps	Tj (Total Jitter) ps 10^{12} samples	Tj ps 10^{6} samples
Reference Clock	4.7	41.9	108	86
Tx	2.8	60.6	100	87
Media	0.0	90	90	90
Rx	2.8	120.4	160	147
Linear Total Tj			458	410
Root Sum Square (RSS) Tj[1]			399.13	371.52

Note 1: RSS Calculated per the below equations.

$$Tj = \sum Dj_n + 14.069 \cdot \sqrt{\sum Rj_n^n}$$

$$Tj = \sum Dj_n + 9.507 \cdot \sqrt{\sum Rj_n^n}$$

The above table has been reworded slightly to minimize confusion. Table 4.3 from CEM 2.0 is shown below. Note that the right most column header says Tj (Total Jitter) at BER 10^{-6}. This implies that if the measured reference clock Tj is 86ps with a 10^6 sample size that the BER will be 10^{-6} and this is not true. If you measure 86ps Tj with a sample size of 10^6, extrapolating that to 10^{12} samples will yield 108ps Tj for the reference clock and a corresponding BER of 10^{-12}, assuming all the other jitter sources are less than or equal to their respective limits.

Table 4-3: Total System Jitter Budget For 2.5 GT/s Signaling

Jitter Contribution	Min Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)[3]	Tj at BER 10^{-6} (ps)
Tx	2.8	60.6	100	87
Ref Clock	4.7	41.9	108	86
Media	0	90	90	90
Rx	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

Notes:

Gen 2–5.0 Gb/s

For 5 Gb/s signaling, the system jitter budget scales 200ps, which is half the value of the jitter budget at 2.5 Gb/s Table 4-5 in CEM 2.0 shows the following budget.

Table 7: Total System Jitter Budget for 5 Gb/s Timing

Jitter Contribution	Max Dj ps	Tj at BER 10^{12} (ps)
Reference Clock	30.0	50
Tx	0.0	4306
Media	58	58
Rx	60	80
Linear Total Tj		231.6
Root Sum Square (RSS) Tj[1]		200

$$Tj = \sum Dj_n + 14.069 \cdot \sqrt{\sum Rj_n^n}$$

Other than the content in the above table, CEM 2.0 does not go into any more specifics on reference clock jitter. Rather, CEM 2.0 describes a 2-port method of simultaneously assessing the system board data and reference clock in section 4.7.5.

The PCI Express Base Specification 2.0 does go into more details on reference clock jitter and expresses the limit in terms of rms jitter rather than peak-to-peak phase jitter. The following table is from section 4.3.7.2.3 of the PCI Express Base Specification.

Table 8: 5 Gb/s Reference Clock Jitter Specification

Symbol	Description	Maximum Limit
TREFCLK-HF-RMS	> 1.5MHz to Nyquist Frequency rms jitter after applying system transfer function	3.1ps rms

The 3.1ps rms jitter is assumed to be all Rj and if you multiply this number by 14.069, you get 43.6ps peak-to-peak jitter as shown in CEM 2.0 specification.

Gen 3–8.0 Gb/s

For 8 Gb/s signaling, the total system jitter scales 125ps, which is slightly more than half the value of the jitter budget at 5 Gb/s. However, the rms jitter is 1.0ps, which is a third that of the RefClock jitter at 5 Gb/s. The burden of meeting this tighter requirement is primarily accommodated by the higher bandwidth of the phase interpolator, which discards jitter below 10MHz.

Table 9: 8 Gb/s Reference Clock Jitter Specification

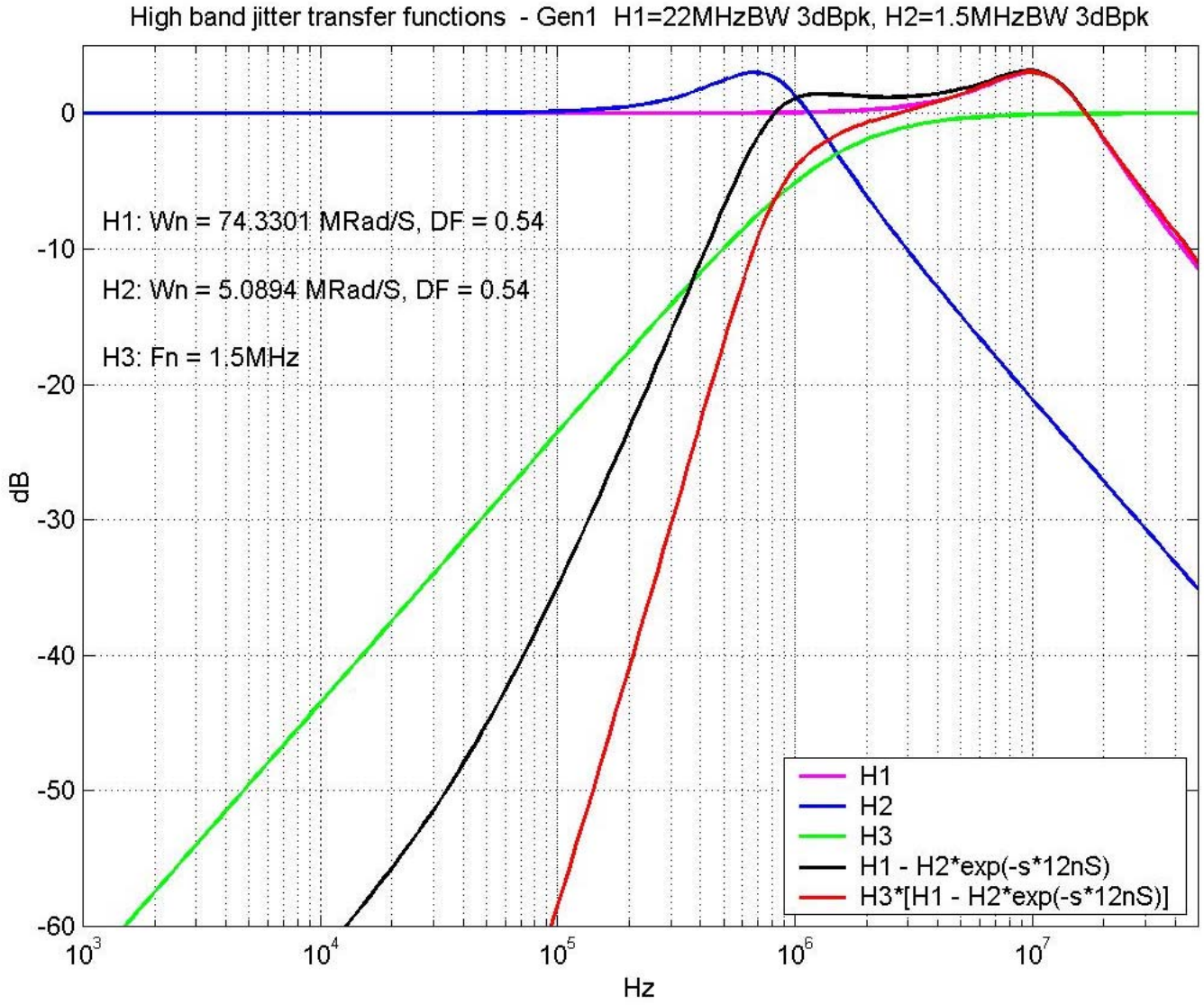
Symbol	Description	Maximum Limit
TREFCLK-HF-RMS	> 1.5MHz to Nyquist Frequency rms jitter after applying system transfer function	1.0ps rms

Characteristics of Jitter Filters

Gen 1–2.5 Gb/S

In Figure 8 below, H1, H2, H3, the PLL Difference Function and HCC are plotted for comparison, where these transfer functions are calculated using the jitter model parameters of Table 1.

Figure 8. Gen 1 Magnitude Bode Plot of Transfer Functions



The composite transfer function in red has an effectively three zeros in the high pass response above 100kHz and two zeros below 10kHz. This high pass response means the system is relatively insensitive to low frequency Refclock modulation effects such as spread spectrum and switching power supply noise, which is usually at about 200kHz. The other take away from this plot is that noise sources in the 10MHz range undergo jitter amplification and therefore merit attention.

Inspection of Figure 8 above shows that the -3dB corners of the overall band pass system transfer function for the common clock architecture are at 1.2MHz to 21.9MHz. These are different from the 1.5MHz -3dB bandwidth of H2 and H3 and the 22MHz -3dB bandwidth of H3 as can be seen by inspection of HCC. The pole positions of HCC are the same as the pole positions of H1, H2 and H3. However, -3dB bandwidth is also determined by the transfer function zeros. The zero positions move due to the subtraction of the Tx embedded clock and the Rx sampling clock at the receive latch.

Gen 2–5.0 Gb/S

Figure 9. Gen2 High Band Magnitude Bode Plot, H1=8MHz w 3dB Peak, H2=16MHz w 3dB pk, H1 Transport Delay = 12nS

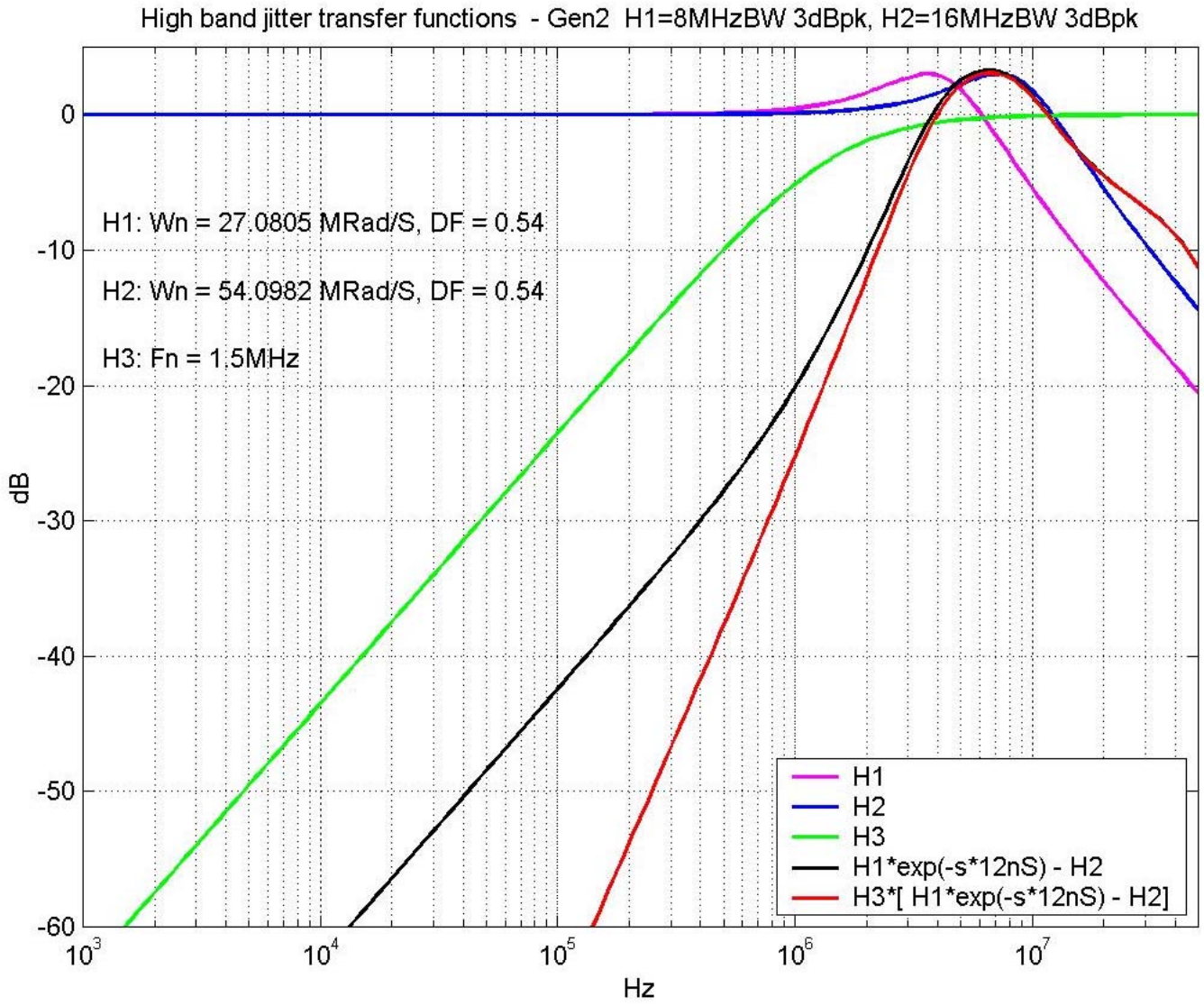


Figure 10. Gen2 High Band Magnitude Bode Plot, H1=8MHz w 3dB Peak, H2=32.6MHz w 0.5dB pk, H1 Transport Delay = 12nS

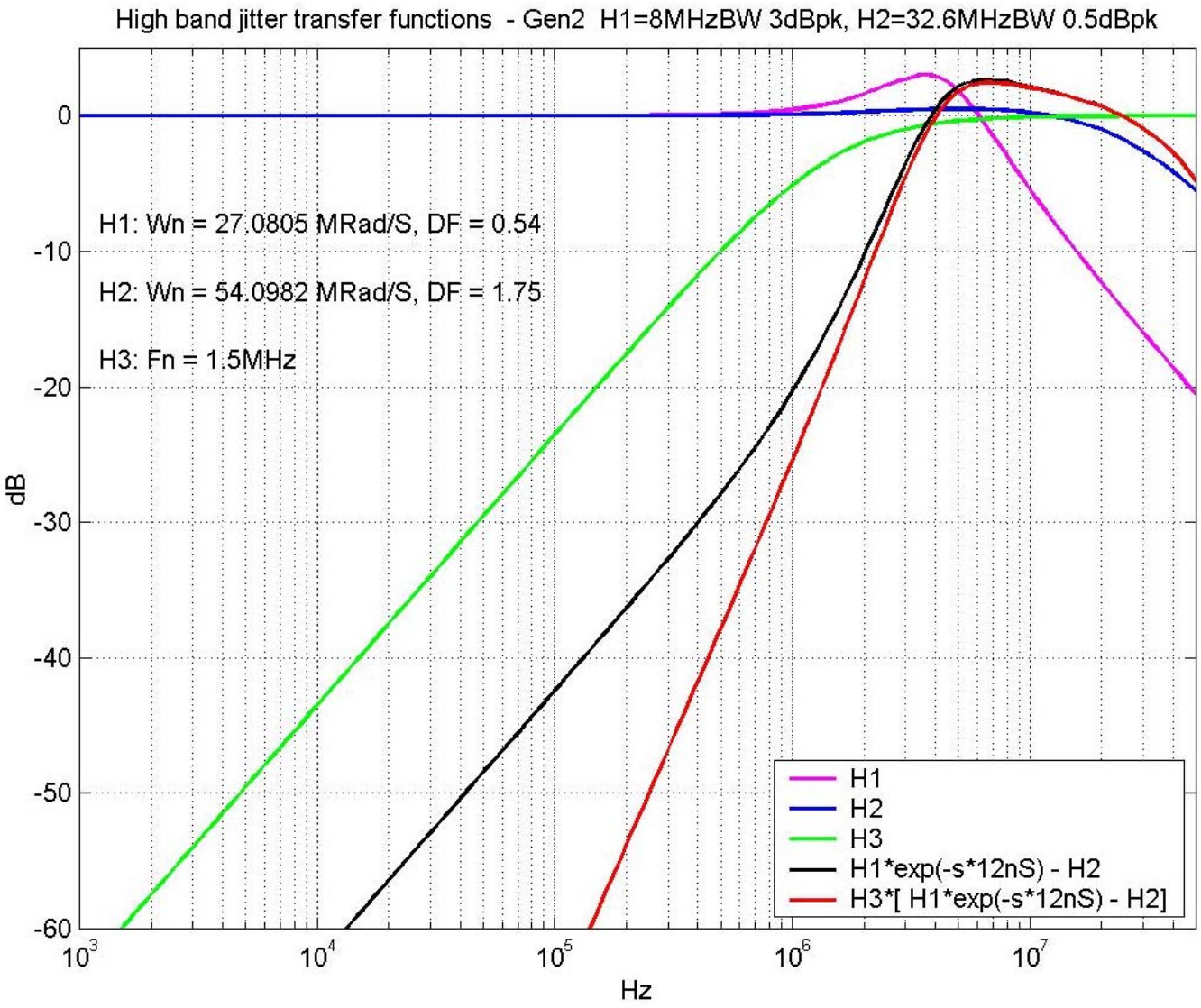


Figure 11. Gen2 Low Band RefClock Difference Function, H1=8MHz w 3dB Peak, H2=16MHz w 3dB pk,H1 Transport Delay = 12nS

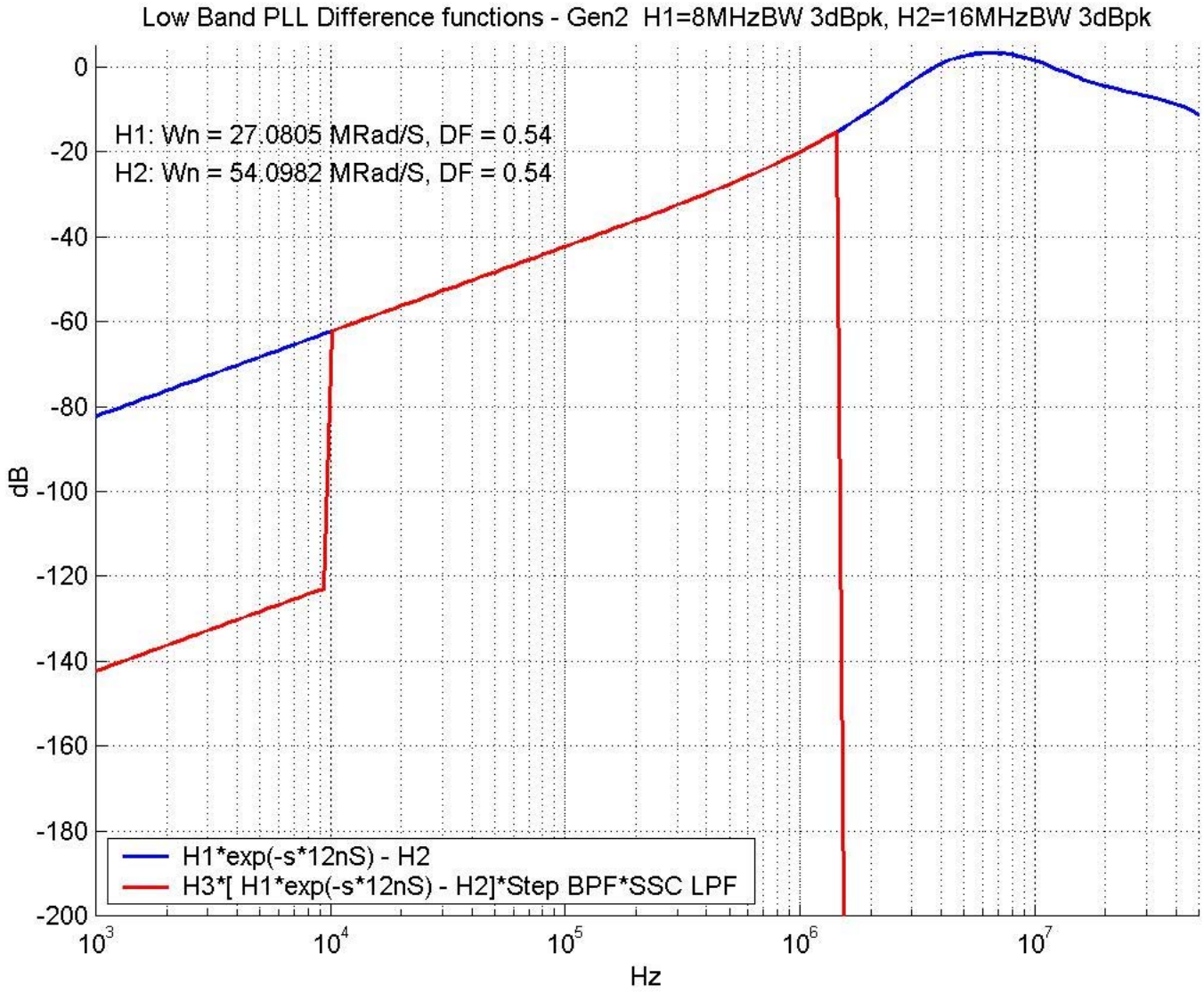


Figure 12. Gen2 Low Band RefClock Difference Function, H1=8MHz w 3dB Peak, H2=32.6MHz w 0.5dB pk, H1 Transport Delay = 12nS

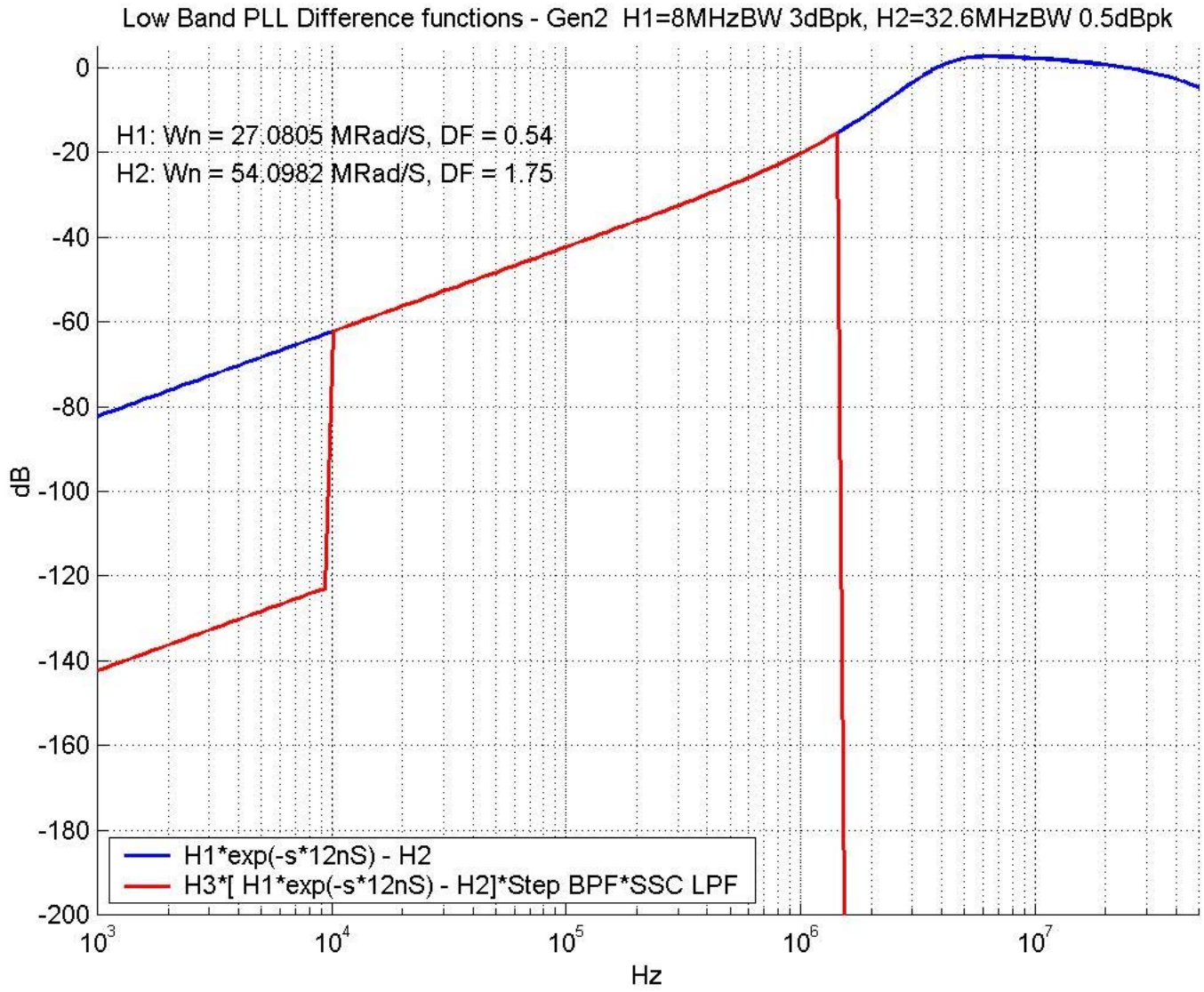


Figure 13. Gen3 High Band Magnitude Bode Plot, H1=2MHz w 2dB Peak, H2=5MHz w 0.01dB pk, H1 Transport Delay = 12nS

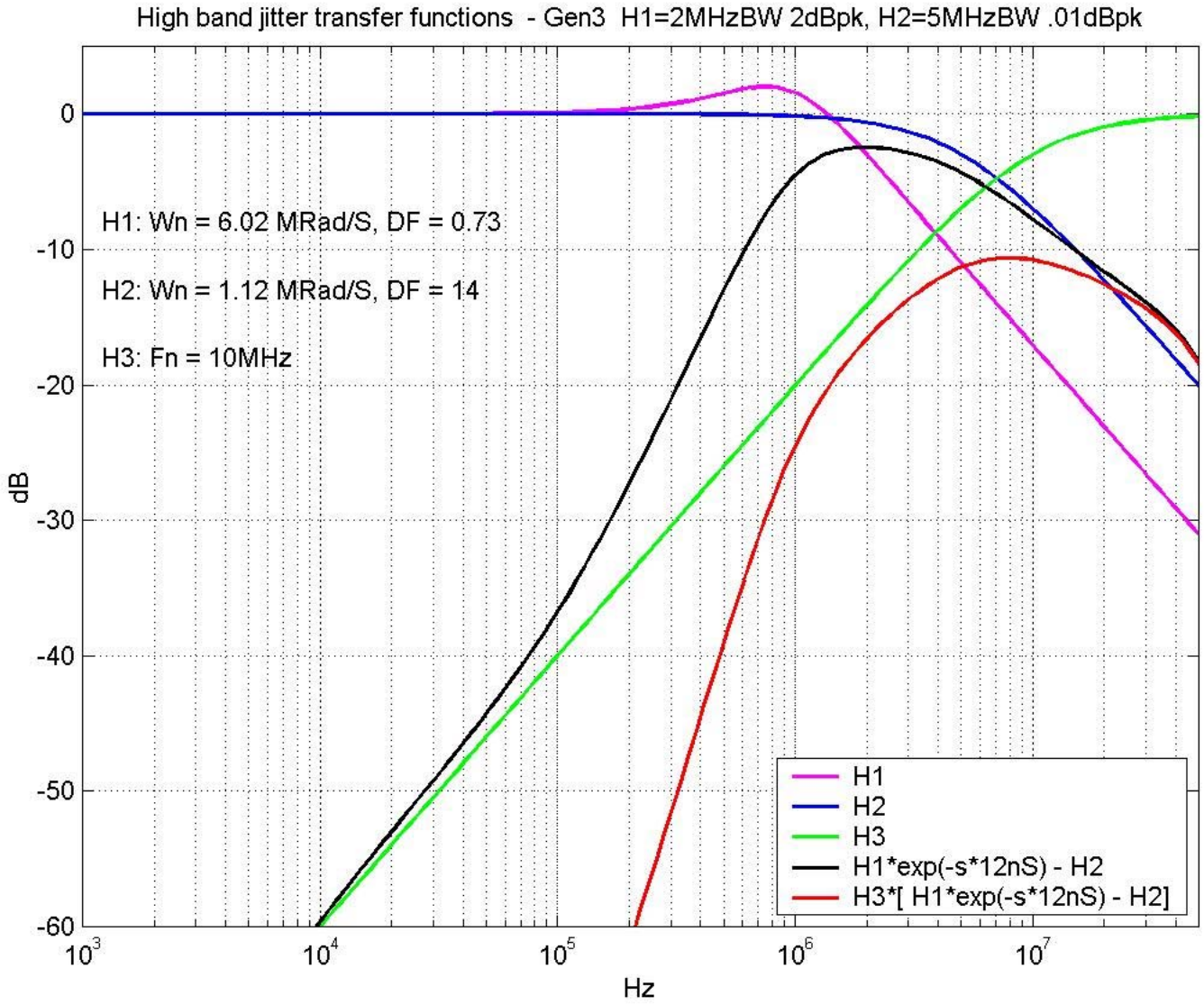


Figure 14. Gen3 High Band Magnitude Bode Plot, H1=4MHz w 2dB Peak, H2=5MHz w 0.01dB pk, H1 Transport Delay = 12nS

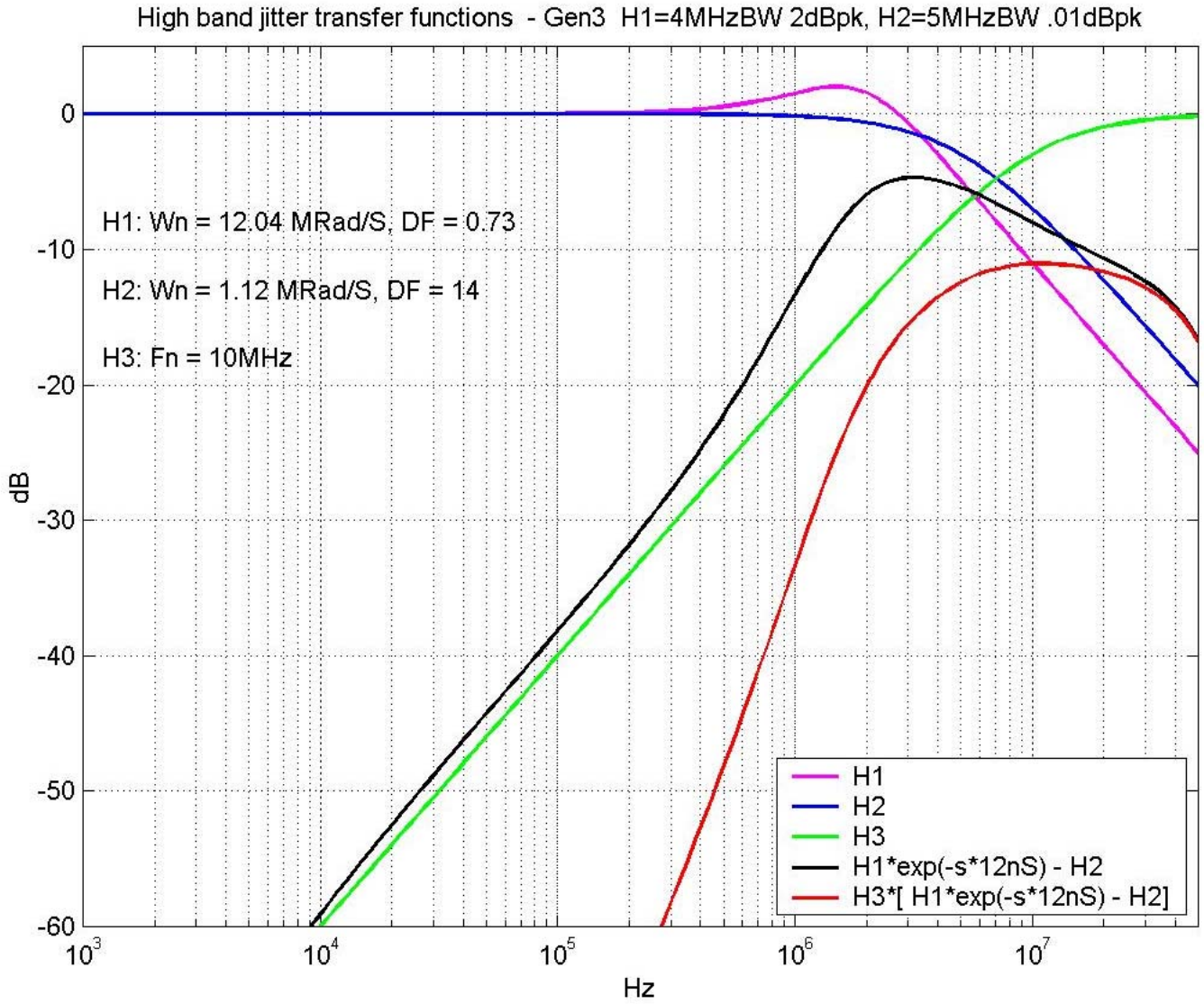


Figure 15. Gen3 Low Band RefClock Difference Function , H1=2MHz w 2dB Peak, H2=5MHz w 0.01dB pk, H1 Transport Delay = 12nS

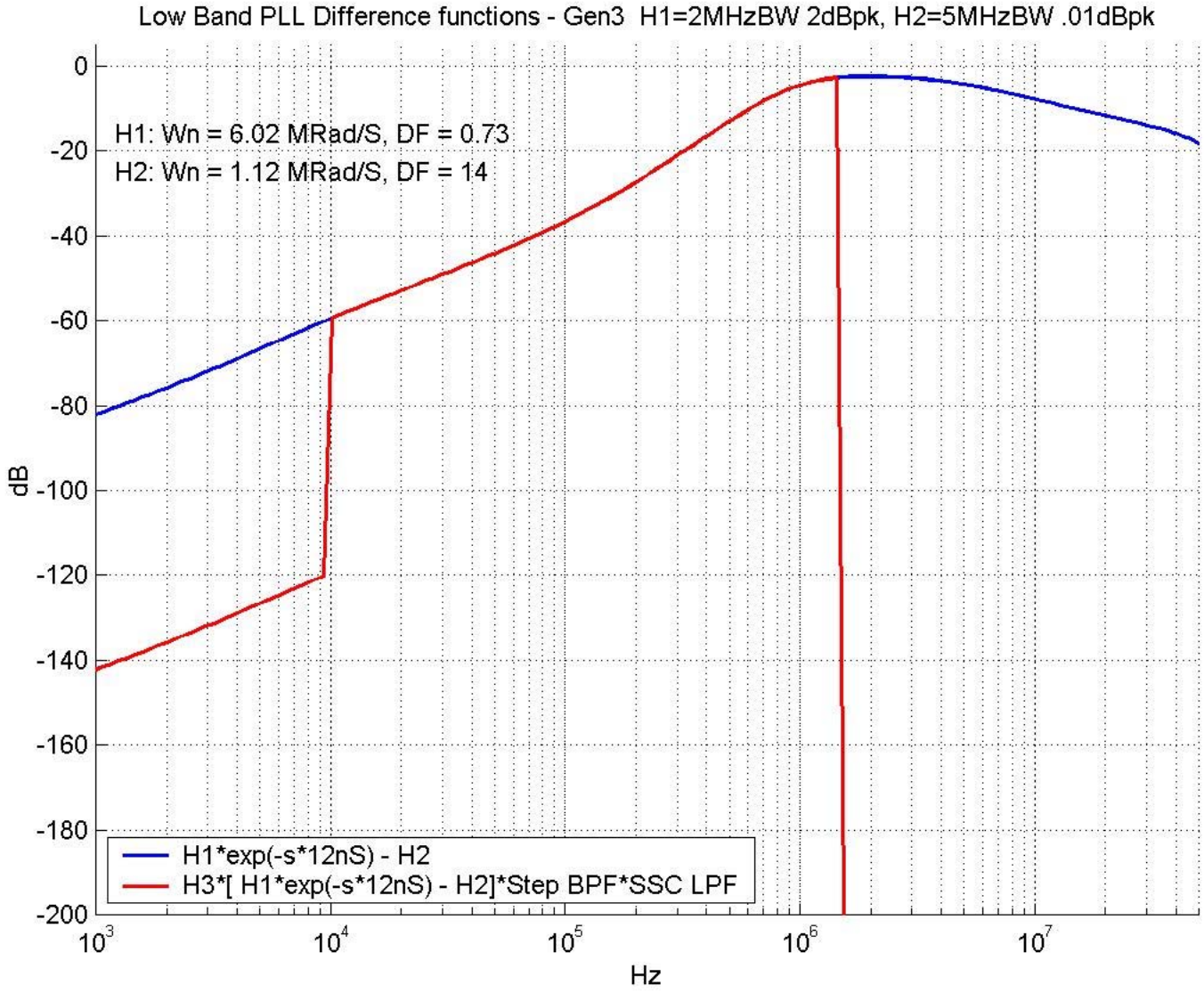
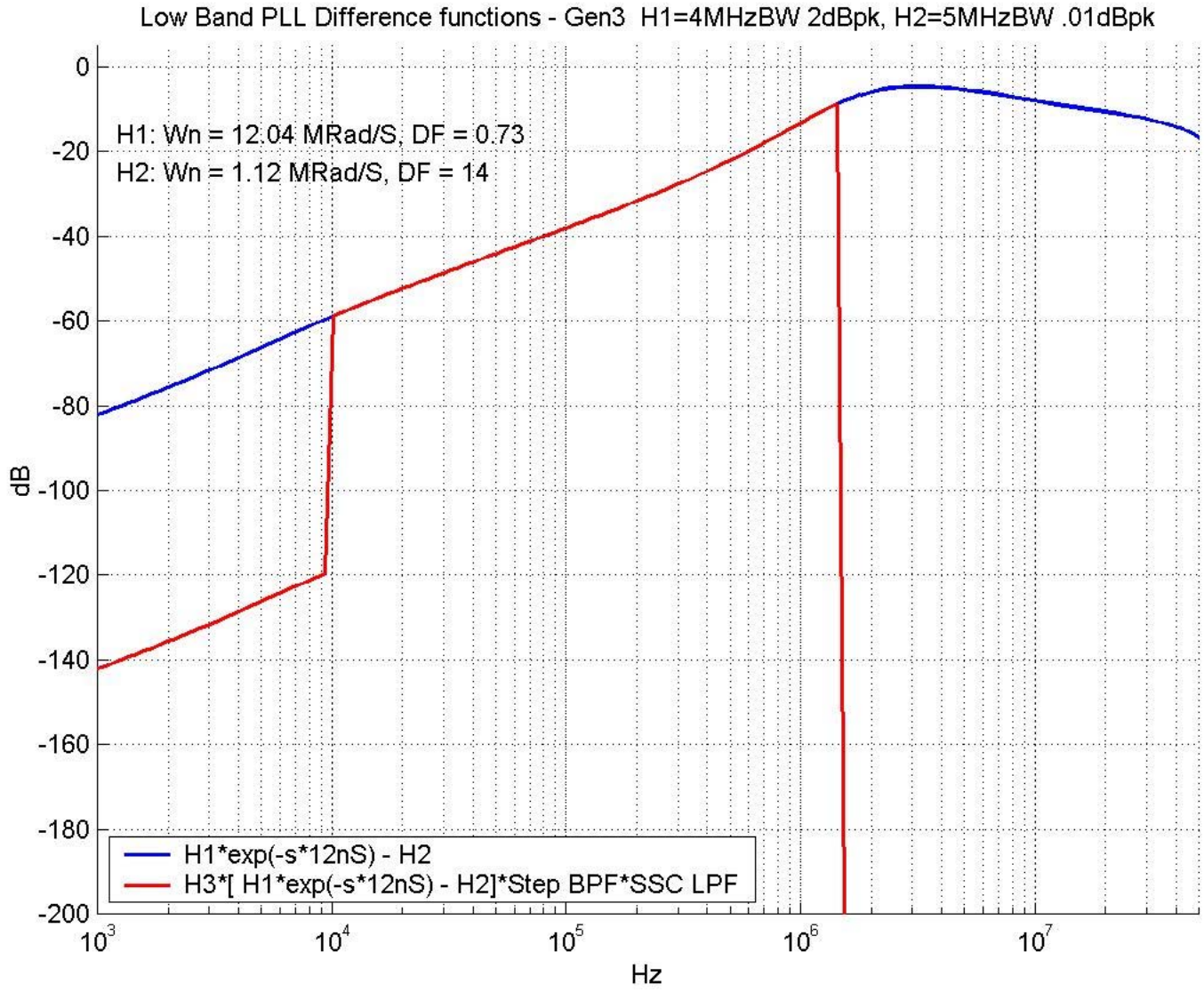


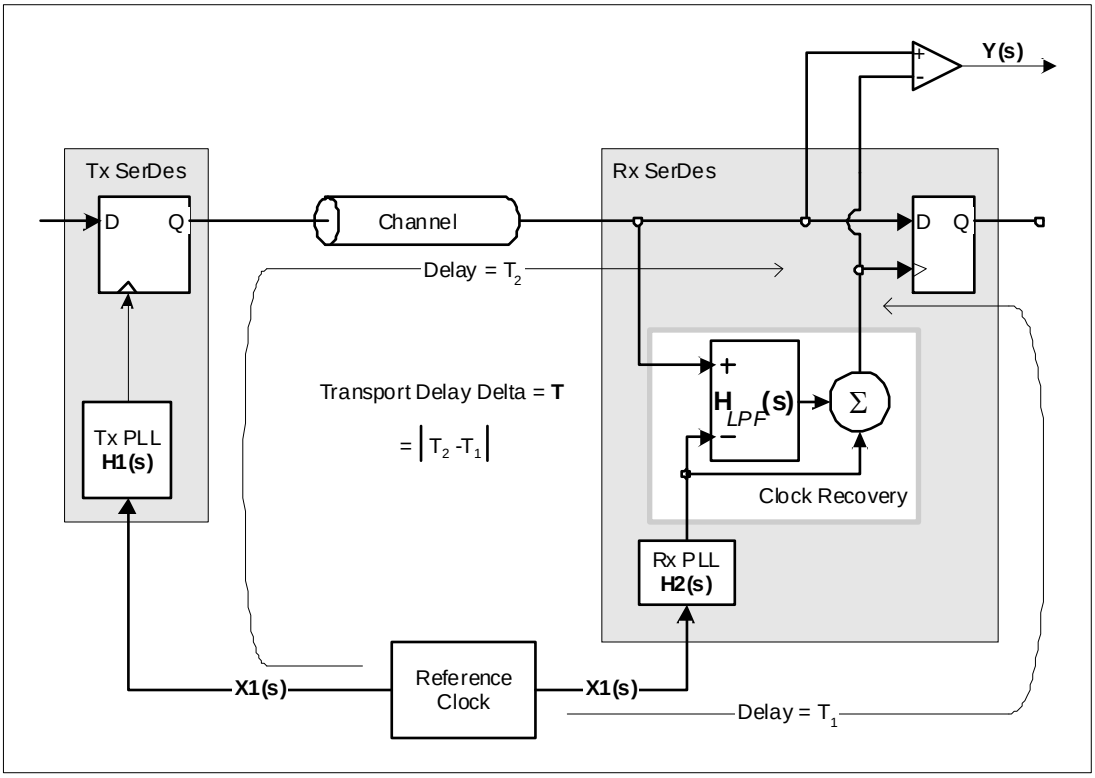
Figure 16. Gen3 Low Band RefClock Difference Function , H1=4MHz w 2dB Peak, H2=5MHz w 0.01dB pk, H1 Transport Delay = 12nS



Appendix 1–Derivation of Equivalent Phase Transfer Function

Figure 17 is a diagram of a simplex link showing the timing PLLs and their phase transfer functions. The reference clock is typically running at 100MHz and the PLL's inside the serdes multiply the reference clock to the line bit rate. The Clock Recovery function, shown implemented as a phase interpolator because the actual clock frequency is common across the data link, adjusts the phase of the receiver Reference Clock to align it with the embedded clock in the Rx serial data. The eye closure function Y(s) is the difference between the phase difference between the center of the data and the rising edge of the receiver D Latch sampling clock. H_{LPF} (s) is a single pole low pass filter in the Clock Recovery that generates a running average of the phase difference between the data embedded clock and the receiver reference clock. This averaged phase difference is added to the receiver reference clock to produce a latching clock at the receiver D clock port that is a half bit period delayed relative to the received data embedded clock in order to align the clock with the time center of each bit.

Figure 17. Phase Transfer Function Model for Common RefClock Architecture



Y(s) and its associated transfer function H_{CC}(s) are both readily determined by inspection of the model as below. The clock recovery function appears in the final model as a high pass filter H3(s) applied directly to the Reference Clock phase noise X1(s), after the simplifying model re-arrangement seen below. That H3 is a single pole high pass filter follows mathematically from the fact that when a single pole low pass filter is subtracted from unity, the result is a single pole high pass. Physically H3 is a high pass filter that models the fact that the phase aligner tracks out low frequency jitter more efficiently than high frequency jitter.

$$Y(s) = X1(s)\,H1(s)e^{-sT} - \left[\left(X1(s)\,H1(s)e^{-sT} - X1(s)H2(s)\right)H_{LPF}(s) + X1(s)H2(s)\right]$$

$$Y(s)/X1(s) = H1(s)e^{-sT} - \left[\left(H1(s)e^{-sT} - H2(s)\right)H_{LPF}(s) + H2(s)\right]$$

$$H_{CC}(s) = \left[H1(s)e^{-sT} - H2(s)\right] - \left[H1(s)e^{-sT} - H2(s)\right]H_{LPF}(s)$$

$$= \left\{1 - H_{LPF}(s)\right\}\left[H1(s)e^{-sT} - H2(s)\right]$$

$$= H3(s)\left[H1(s)e^{-sT} - H2(s)\right]$$

Several comments regarding this general model are in order.

1. H1 and H2 use equations for 2nd Order PLL's below:

$$H_{PLL}(s) = \frac{2s\xi\omega_n + \omega_n^2}{s^2 + 2s\xi\omega_n + \omega_n^2}$$

Specific values for damping factor and natural frequency are required inputs for the jitter model.

2. The PCIe Reference Clock specification is defined in terms of H3(s), not H_{LPF} (s). H3(s) is independent of the design details of the clock recovery function but does depend on the PCIe Generation.
3. The H1-H2 difference function below is important in its own right and is referred to by PCISIG as the PLL Difference Function. It is used instead of H_{CC} as the Refclock transfer function for the Low Band jitter model.

$$PLL\ DifferenceFunction = H_{PLLDiff} = \mathrm{H1}(s)e^{-s\mathrm{T}} - \mathrm{H2}(s)$$

or

$$H_{PLLDiff} = \mathrm{H1}(s) - \mathrm{H2}(s)e^{-s\mathrm{T}}$$

4. The PLL Difference function corresponds to the worst case mismatch between Tx and Rx PLLs for jitter modeling. Second order transfer functions are assumed, even though most PLL transfer functions are 3rd order or higher. Second order functions tend to yield a slightly conservative difference function vis-a-vis an actual PLL.
5. T is associated with either H1 or H2 depending on the Generation as below. For any given H1 and H2 pair, the noise equivalent bandwidth of Hcc is greatest when T is associated with the smallest bandwidth transfer function. Consider that the bandwidth of H2 is greater than H1. At a frequency in the transition band of H1, the H1 transfer function phasor will have a smaller magnitude and greater phase delay than the H2 transfer function. Therefore if the T phase delay is added to the H2 phasor, T will tend to phase align the H2 phasor to the H1 phasor and therefore reduce the vector difference of the two phasors. Conversely if T is added to the H1 phasor, it will increase the magnitude of the vector difference. This is true for all frequencies

   Proper selection of T to maximize the noise equivalent bandwidth is particularly important for Gen 3 because thirty combinations of H1 and H2 are specified by PICSIG. If T is assigned to the lowest bandwidth PLL function, the number of cases to be considered will be fifteen rather than thirty.

$$H_{CC} = \mathrm{H3}(s)\left[\mathrm{H1}(s)e^{-s\mathrm{T}} - \mathrm{H2}(s)\right] \qquad \text{Gen 1 and Gen 3}$$

$$H_{CC} = \mathrm{H3}(s)\left[\mathrm{H1}(s) - \mathrm{H2}(s)\,e^{-s\mathrm{T}}\right] \qquad \text{Gen 2 and Gen 3}$$

6. If the transport delay, T, is zero, then the PLL Difference Function behaves as a two pole high pass filter at low frequencies. However if T is non-zero, then the PLL Difference Function behaves as a single pole high pass. For the details of this, see Section, “Appendix 2–HPLLdiff Behavior at Low Frequencies”.

Appendix 2–$H_{PLLdiff}$ Behavior at Low Frequencies

The frequency behavior of $H_{PLLdiff}$ can be understood by taking only the zero and first order terms of the McLaurin expansion for the transfer function of the delay T and taking the limit as $s \rightarrow s_0$, where s_0 is a low frequency, but not zero. The transfer functions have been frequency normalized to simplify the algebra.

$$H_{PLLDiff} = \frac{2\,s_1\,\zeta_1+1}{s_1^2+2\,s_1\,\zeta_1+1} - \frac{2\,s_2\,\zeta_2+1}{s_2^2+2\,s_2\,\zeta_2+1}\exp\,(-sT)$$

$$\sim= \frac{2\,s_1\,\zeta_1+1}{s_1^2+2\,s_1\,\zeta_1+1} - \frac{2\,s_2\,\zeta_2+1}{s_2^2+2\,s_2\,\zeta_2+1}(1-sT)$$

$$= \left[\frac{2\,s_1\,\zeta_1}{s_1^2+2\,s_1\,\zeta_1+1} - \frac{2\,s_2\,\zeta_2}{s_2^2+2\,s_2\,\zeta_2+1}\right] + \left[\frac{1}{s_1^2+2\,s_1\,\zeta_1+1} - \frac{1}{s_2^2+2\,s_2\,\zeta_2+1}\right] - \frac{sT\,(2\,s_2\,\zeta_2+1)}{s_2^2+2\,s_2\,\zeta_2+1}$$

$$= \frac{N_{BP}}{D} + \frac{N_{LP}}{D} - \frac{s_2\,\omega_2\,T\,(2\,s_2\,\zeta_2+1)}{s_2^2+2\,s_2\,\zeta_2+1} \quad \textit{where} \quad D = (s_1^2+2\,s_1\,\zeta_1+1)(s_2^2+2\,s_2\,\zeta_2+1)$$

$$N_{BP} = 2\,s_1\,\zeta_1\,(s_2^2+2\,s_2\,\zeta_2+1) - 2s_2\zeta_2(s_1^2+2s_1\zeta_1+1)$$
$$= 2\,s_1\,\zeta_1\,(s_2^2+1) - 2\,s_2\,\zeta_2\,(s_1^2+1) + 2\,s_1\,\zeta_1\,2s_2\,\zeta_2 - 2\,s_2\,\zeta_2\,2\,s_1\,\zeta_1$$
$$= 2\,s_1\,\zeta_1\,(s_2^2+1) - 2\,s_2\,\zeta_2\,(s_1^2+1)$$

$$N_{LP} = (s_2^2+2\,s_2\,\zeta_2+1) - (s_1^2+2\,s_1\,\zeta_1+1)$$
$$= (s_2^2+2\,s_2\,\zeta_2) - (s_1^2+2\,s_1\,\zeta_1)$$
$$= s_2\,(s_2+2\zeta_2) - s_1(s_1+2\zeta_1)$$

$$N_{BP}+N_{LP} = [2\,s_1\,\zeta_1\,(s_2^2+1) - 2\,s_2\,\zeta_2\,(s_1^2+1)] + [s_2\,(s_2+2\zeta_2) - s_1\,(s_1+2\zeta_1)]$$
$$= 2\,s_1\,\zeta_1\,s_2^2 + 2\,s_1\,\zeta_1 - 2\,s_2\,\zeta_2\,s_1^2 - 2\,s_2\,\zeta_2 + s_2^2 + 2\,s_2\zeta_2 - s_1^2 - 2\,s_1\,\zeta_1$$
$$= 2\,s_1\,\zeta_1\,s_2^2 - 2\,s_2\,\zeta_2\,s_1^2 + s_2^2 - s_1^2$$
$$= s_2^2\,(2\,s_1\,\zeta_1+1) - s_1^2\,(2\,s_2\,\zeta_2+1)$$

We now take the limit as $s \rightarrow s_0$. This also limits s_1 and s_2 to small values since these variables are just s frequency scaled by the particular PLL natural frequency. The slope of the PLL Difference function follows.

$$\lim_{s\to s_0} H_{PLLDiff} = \lim_{s\to s_0} \frac{s_2^2\,(2\,s_1\,\zeta_1+1) - s_1^2\,(2\,s_2\,\zeta_2+1)}{D} - \frac{\omega_2\,T\,(2\,s_2^2\,\zeta_2+s_2)}{s_2^2+2\,s_2\,\zeta_2+1} = \lim_{s\to s_0} \frac{s^2\,\tau_2^2 - s^2\,\tau_1^2}{D} - \frac{\omega_2\,T\,s_2\,(2\,s_2\,\zeta_2+1)}{s_2^2+2\,s_2\,\zeta_2+1}$$

$$= \lim_{s\to s_0} \frac{s^2\,(\tau_2^2-\tau_1^2)}{(s_1^2+2\,s_1\,\zeta_1+1)(s_2^2+2\,s_2\,\zeta_2+1)} - \frac{s\,\omega_2\,T\,(2\,s_2\,\zeta_2+1)}{s_2^2+2\,s_2\,\zeta_2+1}$$

$$= s_0^{\,2}(\tau_2^2-\tau_1^2) - s_0\,\omega_2\,T$$

This last result shows that if T is zero, then the PLL difference function behaves as if there are two zeros at the origin. If T is non-zero, then the two zero response remains, but there is an additional one zero response that, by virtue of its larger amplitude at low frequencies, effectively suppresses the two zero response. At higher frequencies, but below the maximum of Hcc, the response behaves with either a 50dB/dec to 60 dB/dec slope depending on the peaking of the specific PLL transfer functions under consideration. When H3 and T are both included, Hcc behaves with a two zero response at low frequencies.

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