Introduction

The selection of the PLL loop filter components begins with a determination of the optimum bandwidth of the PLL. Often this bandwidth is not known at the initial design stage and must be determined empirically based on system performance. The determination of the final filter is then an iterative process. This application note is intended to guide the designer to an initial filter and utilize two simple scaling rules to adjust filter component values and bandwidth.

Determination of PLL Bandwidth

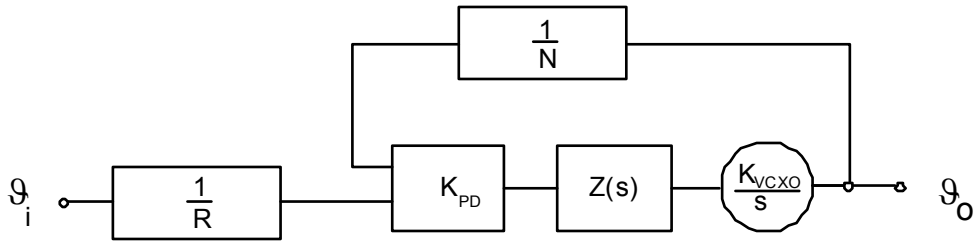
In many cases the bandwidth of a PLL is selected based on the minimum phase noise of the PLL output. This is determined by the trade-off between the phase noise that is translated to the output from the input reference and the noise generated internally by the PLL. In input reference dejitter applications, the spectrum of the noise of the input reference is higher than the internal noise of the PLL. In this case the loop bandwidth is set low so the input reference noise is rejected in the PLL loop filter. Conversely, if the noise of the reference is low relative to the PLL internal noise, then the loop gain of the PLL is increased to suppress internal noise, which also extends the PLL bandwidth. An example of this second case is when a clean reference such as a crystal oscillator is to be frequency translated.

The bandwidth of a PLL based on a VCXO is typically used for dejittering applications where the bandwidth is set in the range of 10–250Hz to provide attenuation of input reference clock jitter and to take advantage of the low VCXO noise realized by use of a narrow band crystal resonator.

Determination PLL Control Loop Overview

The basic PLL control loop is shown in Figure 1 below. The input reference divider is R, the feedback divider is N, the phase detector gain is K_{PD} (mA/rad), the loop filter is Z(s) (Ohms) and the VCXO is an integrator with a gain of K_{VCXO} (rad/V). The modulation bandwidth of the VCXO introduces another pole in the VCXO response, but this is assumed to be much higher in frequency than the closed loop response of the PLL and therefore ignored.

Figure 1. VCXO Based PLL Block Diagram



The phase transfer function of the PLL then is:

$$\frac{\vartheta_o}{\vartheta_i} = \frac{N}{R} \frac{\frac{K_{PD}K_{VCXO}}{N}\frac{Z(s)}{s}}{1+\frac{K_{PD}K_{VCXO}}{N}\frac{Z(s)}{s}}$$

The frequency response of the PLL is determined by the user with the selection of N and Z(s). Several general properties are to be noted.

1. R is outside the feedback loop and does not affect the PLL frequency response. R therefore does not play a role in the loop filter design.
2. All phase variables are in units of radians and all frequencies are in units of rad/sec. Bandwidth will also be in units of rad/sec. When calculating loop filter values based on the design target bandwidth, the factor of 2π must be included to be consistent with the LaPlace variable s. KPD is in units of mA/rad and K_{VCXO} is in units of rad/V. Since the phase detector and VCXO are cascaded in the PLL, the two terms always occur as a product. It is more intuitive to define K_{PD} in units of mA/Hz and K_{VCXO} in units of Hz/V since the factor of 2π cancels in the product.
3. The loop gain is:

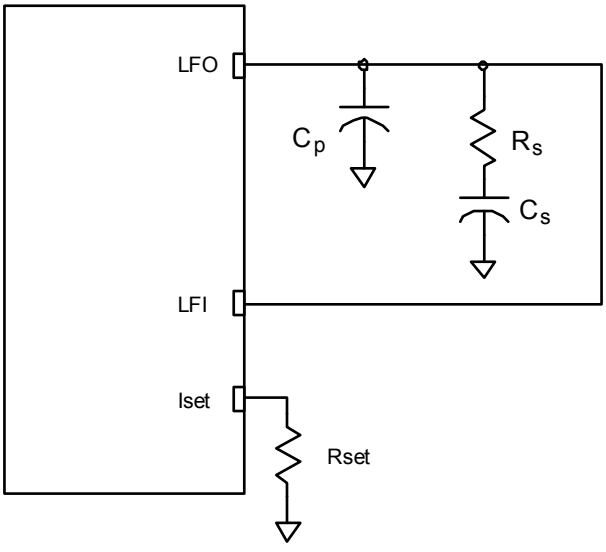
$$\frac{K_{PD}K_{VCXO}}{N}\frac{Z(s)}{s}$$

   The loop gain is composed of two parts, a constant factor and a frequency dependent factor. The constant factor contains four user selectable factors, N, the impedance level of the filter, K_{PD} and K_{VCXO}. K_{PD} is set by the charge pump current and K_{VCXO} weakly by the selection of external pullable crystal. The impedance level of the filter is set by the particular selection of external components.
4. The user selectable frequency dependent factors are composed of the capacitors and time constants in the loop filter impedance.
5. The phase transfer and the frequency translation factor of the PLL is N/R. Any common multiple of N and R will also result in the same frequency translation. Since increasing N will decrease the bandwidth of the PLL, the bandwidth of the PLL can be decreased without changing the frequency translation by increasing N and R by the same factor.
6. High values of loop gain suppress distortion and improve the low frequency input reference tracking performance of the PLL. There three ways to increase the loop gain: increase K_{PD} (by decreasing R_{SET}), by increasing the impedance of the loop filter (by increasing resistance and decreasing capacitance) and by selecting a crystal with greater pull range.

Second Order PLL Loop Filter

The simplest practical loop filter is depicted in Figure 2 below. LFO is the connection of the charge pump output of the PLL to the loop filter. LFI is the VCXO frequency control input pin and is driven from the output of the loop filter. The filter shown is second order, which when combined with the phase integrator of the VCXO, results in a third order PLL.

Figure 2. External PLL Filter Components



CS is effectively the loop error integrator that determines the ability of the PLL to track the input reference at low frequencies. RS set the impedance zero with CS that cancels the CS loop filter integrator pole so that the loop gain will cross over unity gain controlled primarily by the VCXO integrator pole. CP is much smaller than CS and serves to low pass filter the pulse width modulated charge pump output to a DC current. If the value of this capacitor is too small, the output spectrum of the PLL will contain spurious frequencies at the phase detector frequency.

The current through the RSET resistor determines ISET and therefore KPD. The ISET pin of the PLL outputs a nominal 1.1V across RSET.

The charge pump current sets the phase detector gain as follows where the factor of 2π has been factored out to convert to Hz.

$$K_{PD} = I_{CP} \qquad \text{(mA/Hz)}$$

The impedance of this filter is below:

$$Z(s) = \frac{1}{s(C_s + C_p)} \frac{sR_sC_s + 1}{\left(sR_s \frac{C_pC_s}{(C_s + C_p)} + 1\right)}$$

Higher order filters are possible with poles above the unity gain crossover to increase the low pass filtering of phase detector pulses.

PLL Transfer Function

The closed loop response with this filter is:

$$\frac{\vartheta_o}{\vartheta_i} = \frac{N}{R} \frac{sR_sC_s + 1}{s^3 \frac{NR_sC_pC_s}{K_{PD}K_{VCXO}} + s^2 \frac{N(C_s + C_p)}{K_{PD}K_{VCXO}} + sR_sC_s + 1}$$

Equation 1

Since the third order transfer function denominator of Equation 1 is inconvenient to factor for the roots, we reduce the order by first noting that CS is much larger than CP. Assume that CP is zero discards the third order term that sets the charge pump filtering pole above the unity gain crossover and simplifies the second order term. The resulting second order denominator is below.

$$\frac{\vartheta_o}{\vartheta_i} = \frac{N}{R} \frac{sR_sC_s + 1}{s^2 \frac{C_s}{K_{PD}K_{VCO}} + sR_sC_s + 1}$$

Equation 2

There are two poles at the origin in the loop gain, one due to the loop filter and the second due to the VCXO. RS creates the zero in the transfer function that cancels the pole at the origin introduced by CS. Therefore, the open loop frequency response at the unity gain crossover is determined by the VCXO pole.

An approximation that yields a first order closed loop response is to assume that CS is replaced by a short. The loop filter impedance is then RS and the single pole is provided by the VCXO. The VCXO PLL loop bandwidth can be approximated by the “normalized” loop bandwidth (denoted as “NBWVCXO”) which is approximately equal to the - 3dB bandwidth. NBW does not take into account the effects of damping factor or the increase in bandwidth due to the third pole generated by CP. The unity gain crossover condition is below, which will be used in the filter design procedure.

$$\frac{\frac{R_S * K_{PD} * K_{VCXO}}{2\pi NBW_{VCXO}}}{N} = 1$$

Equation 3

Equation 2 can be placed into standard frequency normalized form as below to make the damping factor explicit, which will be used in the design procedure.

Equation 4

$$\frac{\vartheta_o}{\vartheta_i} = \frac{N}{R}\frac{s_n R_s\sqrt{\frac{K_{PD}K_{VCXO}C_s}{N}}+1}{s_n^2 + s_n 2\left[\frac{R_s}{2}\sqrt{\frac{K_{PD}C_s K_{VCXO}}{N}}\right]+1}$$

$$= \frac{N}{R}\frac{s_n 2*DF+1}{s_n^2 + s_n 2*DF+1}$$

Simple Determination of Loop Filter Components

1. Make initial selections for N, the PLL target bandwidth, ICP and the Damping Factor. The K_{VCXO} will be fixed by the frequency of the crystal selected for the VCXO.
2. Use the PLL target bandwidth for NBW_{VCXO} in Equation 3 to calculate R_S.

$$R_S = \frac{2\pi NBW_{VCXO}\ N}{I_{CP}K_{VCXO}}$$

3. Use the Damping Factor (DF) expression from Equation 4, the fact that $I_{CP} = K_{PD}$ and the value of R_S from step 2 to calculate C_S.

$$C_S = \frac{N}{I_{CP}K_{VCXO}}\left(\frac{2\mathrm{DF}}{R_s}\right)^2$$

4. Use following relationship to select C_P:

$$C_p = \frac{C_s}{100}$$

This is based on keeping passband peaking less than 0.75 dB. This places the charge pump smoothing pole formed by C_P and R_S pole sufficiently above the unity gain crossover that the phase margin is not appreciably degraded. If greater passband peaking can be tolerated, then C_P can be made larger.

5. Calculate RSET based on I_{CP}.

$$R_{SET} = 2.2\ \mathrm{k\Omega}\ \frac{500\ \mu\mathrm{A}}{I_{CP}}$$

For most IDT PLLs, a 2.2kΩ R will set the charge pump current to 500µA. This conversion should be checked for each design.

6. To prevent jitter on the PLL output due to modulation of the VCXO PLL by the phase detector frequency, the following general rule should be observed:

$$NBW_{\mathrm{VCXO}} \le \frac{f_{\mathrm{Phase\ Detector}}}{100}$$

where

$$f_{\mathrm{Phase\ Detector}} = \frac{f_{\mathrm{Input\ Reference}}}{R} = \frac{f_{\mathrm{VCXO}}}{N}$$

7. The recommended range for the charge pump current is 10µA to 500µA. Below 10µA, charge pump leakage can become a problem. This loop filter leakage can cause locking problems, output clock cycle slips, or low frequency phase noise. As can be seen in the loop bandwidth and damping factor equations or by using the filter response software available from IDT, increasing charge pump current (I_{CP}) increases both bandwidth and damping factor.

8. For applications in which maintaining high loop gain at low frequencies to suppress VCXO noise it is useful to calculate the compensation zero frequency. For frequencies above the zero the loop gain depends on RS and for frequencies below the zero, it depends on C_S. An application where this is important is for clock wander, which is jitter when the jitter frequency is below 10Hz, in telecommunications networks. A similar case is the 10Hz timing jitter lower band edge defined in SMPTE 292M-1998, Bit Serial Digital Interface for High Definition Television Systems.
9. Component selection derived by this procedure can be checked and fine tuned for bandwidth and passband peaking by your IDT FAE.

There are cases where the conditions to select C_P based on the loop bandwidth and the phase detector frequency are not met. For example, a PLL to translate either 8kHz or 156.25MHz to 19.44MHz must use a 2kHz phase detector frequency. This is incompatible with a 100Hz bandwidth. There are three ways to handle this situation. The simplest is to drop the PLL bandwidth until the condition for C_P selection is met assuming wander generation is not a problem. The second way is to use a third or fourth order filter and the third is to do both. Proper design of the higher order filters requires exact calculation of the transfer function to ensure correct component selection.

Loop Filter Design Example

Consider an application to both dejitter a 77.76MHz input reference and translate the input reference frequency to 622.08MHz using the IDT843002-31. This part is a cascade of a VCXO and a FemtoClock. The VCXO is tuned for 19.44MHz and is typically operated at a 100Hz loop bandwidth. The FemtoClock PLL translates the 19.44MHz VCXO output to 622.08MHz with a nominal 500kHz loop bandwidth. This example will show use of the simplified design procedure for a first pass design of the loop filter for the VCXO and a second pass to realize more realistic component values.

Input Values	Pass 1	Pass 2
Input (MHz)	77.76	77.76
VCXO (MHz)	19.44	19.44
N	1	32
Kvcxo (Hz/V)	5000	5000
Icp (uA)	125	40
Damping Factor	4	4
Bandwidth (Hz)	100	100

Calculated Values	Pass 1	Pass 2
Rs (kohm)	1.01	100.53
Cs (uF)	101.32	1.01
Cp (uF)	1.01	0.01
Rset (kohm)	8.8	27.5
Phase Detector (MHz)	19.44	0.6075
Input Divider	4	128
Zero Frequency (Hz)	1.56	1.56

The first pass used a very low value of N and a large value of I_{CP}, which result in a very high loop gain. These high values were offset by the excessive value of 100µF to drop the impedance of the loop filter to achieve the 100Hz bandwidth. Pass 2 increases N and decreases I_{CP} to drop the loop gain so that a reasonable value of 1µF is obtained for C_S. When the three pole PLL is simulated exactly, the realized bandwidth is 135Hz and the Damping Factor is 4.01. The resulting filter is either sufficient for the final design or can be the initial filter used in a simulator for refinement of the PLL bandwidth and peaking.

Two PLL Bandwidth Scaling Rules

Given an existing PLL design, requirement changes can force a new loop filter design. As examples, a change the input or output frequency, selection of a new cost reduced VCXO that has a different K_{VCXO} or a different PLL chip with a different K_{PD}. These changes are made in the constant terms of the loop gain of Equation 1, K_{VCXO}, K_{PD} or N and a compensating change is to be made in the loop filter impedance to preserve the PLL frequency response.

1. Changes in frequency independent terms K_{PD}, K_{VCXO} and N are compensated by impedance scaling by α. Multiply all filter resistances by α and divide all capacitors by α.

The rule for frequency independent scaling is derived by requiring that the loop gain of the scaled PLL, denoted by primes, be equal to that of the original PLL.

$$\frac{K'_{PD}K'_{VCXO}}{N'}\frac{Z'(s)}{s} = \frac{K_{PD}K_{VCXO}}{N}\frac{Z(s)}{s}$$

$$Z'(s) = \frac{K_{PD}}{K'_{PD}}\frac{K_{VCXO}}{K'_{VCXO}}\frac{N'}{N}Z(s)$$

$$Z'(s) = \alpha\, Z(s)$$

This shows that impedance scaling of the loop filter can be used to compensate for changes in the composite constant factor of K_{PD}, K_{VCXO} and N. Since the order of Z(s) is not specified, this is true for loop filters of all orders.

The need for frequency scaling arises when the frequency response has the correct passband peaking and stop band slope but the bandwidth has to be adjusted. For example, a dejitter PLL is passing too much reference jitter to the output and the bandwidth has to be reduced. In this case we need to frequency scale the complex frequency variable, s, by a factor β.

2. To increase the PLL bandwidth in frequency by β, multiply all filter resistors by β and divide all capacitors by β^2.

$$\frac{K_{PD}K_{VCXO}}{N}\frac{Z'(s)}{s} = \frac{K_{PD}K_{VCXO}}{N}\frac{Z\left(\frac{s}{\beta}\right)}{\left(\frac{s}{\beta}\right)}$$

$$Z'(s) = \beta\, Z\left(\frac{s}{\beta}\right)$$

This shows that frequency scaling of the loop filter requires simultaneously scaling both the loop filter impedance and the frequency variable s. Frequency scaling s in the VCXO pole is equivalent to scaling the loop filter impedance by β, exactly as was done by α in Rule 1 above. Frequency scaling s in the loop filter impedance Z(s) is accomplished by dividing all capacitor values by β. Multiplying resistors by β and dividing capacitors by β^2 combines these two scalings.

PLL Bandwidth Scaling Examples

Consider two consecutive scalings, the first is to divide the output frequency by 2, which requires a new value for N, but maintaining the bandwidth of the PLL. Secondly, the bandwidth of the resulting design with the new N is to be scaled by a factor of ½.

	Original Design	Frequency Independent Scale	Frequency Dependent Scale
α		0.5	
β			½
N	32	16	16
Bandwidth (Hz)	35	135	67.5
Damping Factor	4	4	4
Rs (kohm)	100	50	25
Cs (µF)	1	2	8
CP (µF)	0.01	0.02	0.08
ICP (µA)	40	40	40

References

1. Giovanni Bianchi, "Phase-Locked Loop Synthesizer Simulation", McGraw-Hill Companies
2. Roland Best, "Phase-Locked Loops", McGraw-Hill Companies

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