ClockMatrix™

Aligning 1PPS Clocks in Larger Chassis Systems

Abstract

This document explains how to configure multiple ClockMatrix devices to align one pulse-per-second (PPS) signal between a master and multiple line cards in a system using Pulse-Width Modulation (PWM), DPLL alignment mode (frame and sync), phase measurement, and output phase adjustments.

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Related Documents

For more information, visit our website: ClockMatrix™ Timing Solutions

1. Introduction

Commonly, a chassis system must align one pulse-per-second (1PPS or 1Hz) clock edges on different line cards with the 1PPS input of the master. As a chassis system has different types of cards plugged into a common backplane, the accuracy of the 1PPS alignment for modern applications requires compensating for the delay between the cards over the backplane. A chassis system can align two ClockMatrix devices with a pair of clocks (high and low speed) or a single Pulse-Width Modulation (PWM) encoded high-speed clock. Using PWM in signature mode, the 1PPS phase is encoded within the high-speed clock on the master by changing the pulse width in a set pattern to mark the 1PPS phase in the high-speed signal. On the line card, a PWM decoder in ClockMatrix extracts the 1PPS pulse phase signature from the PWM signal and uses it to drive a 1PPS output.

See Figure 1 for the configuration of a chassis system with paired clocks.

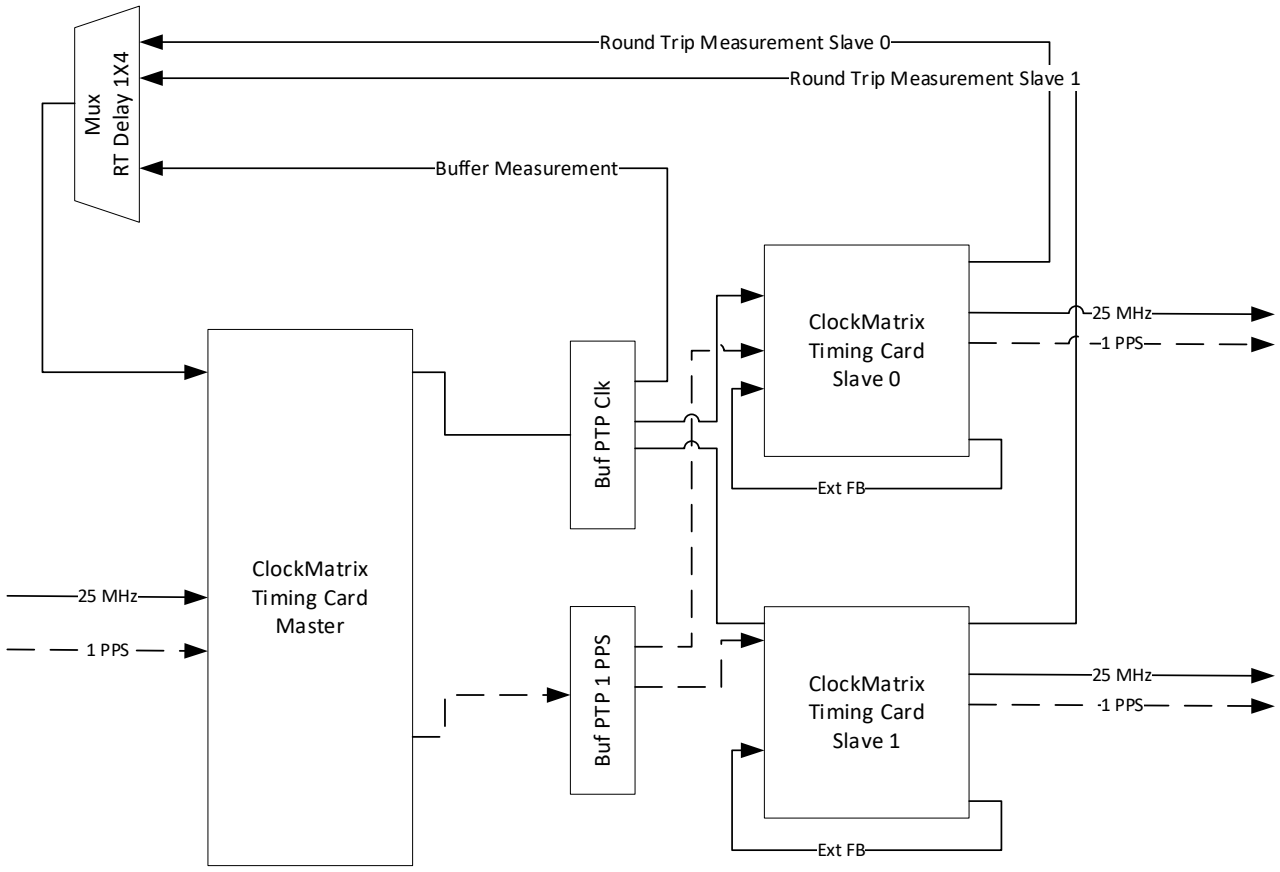

Figure 1. Example System using Paired Clocks

In Figure 1, the solid lines are high-speed clock signals; the dotted lines are 1PPS (1Hz) signals.

First, 25MHz and 1PPS external signals are fed into DPLL0 on the master timing card; next, the output from DPLL0 at 25MHz and 1PPS are fed through buffers. For the 25MHz signal, one output from the buffer connects to the mux to compensate for the delay through the buffer and the mux. From the buffer, another output feeds through the backplane to the DPLLs on the line cards. For ref-sync pulse alignment mode, the DPLL is configured to align the input 1PPS signal to both the output 1PPS signal and an edge of the output 25MHz signal. The 1PPS clock is fed through the second buffer to the DPLLs on the line cards. A 25MHz output from DPLL0 on each line card feeds back to the master timing card for a round-trip delay measurement. (The measurement assumes that the one-way delay across the backplane is half of the measured phase difference.) The measured phase offset sets the phase adjustment separately on each line card to adjust both the 25MHz and 1PPS outputs on each line card so that the 1PPS outputs from each line card is aligned to the 1PPS input to the master with the required accuracy.

The system measures the round-trip delay for each line card as required to compensate for delay changes through the backplane, and for comparison, the system measures the delay through the buffer before the backplane. (For a constant temperature, the delay through the backplane should not change, and the system should choose to measure only at start-up.) Because the delay is measured using a 25MHz signal, any delay over one period of this signal (40ns for 25MHz) must be manually compensated for by delaying the outputs by the measured delay pulse of the number of full cycles.

External feedback is used on the slave ClockMatrix devices to provide the lowest input-to-output delay variation for this system. This method requires two inputs per line card and one output per line card on the backplane.

Figure 2Figure 2 shows an alternate method for distributing the clocks through the system using the PWM signature mode. The main advantage of using this rather than paired clocks is that there is only two clocks per line card (one high-speed output clock with PWM to each line card and one high-speed output clock from the line card). In many designs, high-speed clocks are easier to route on each card and through the backplane.

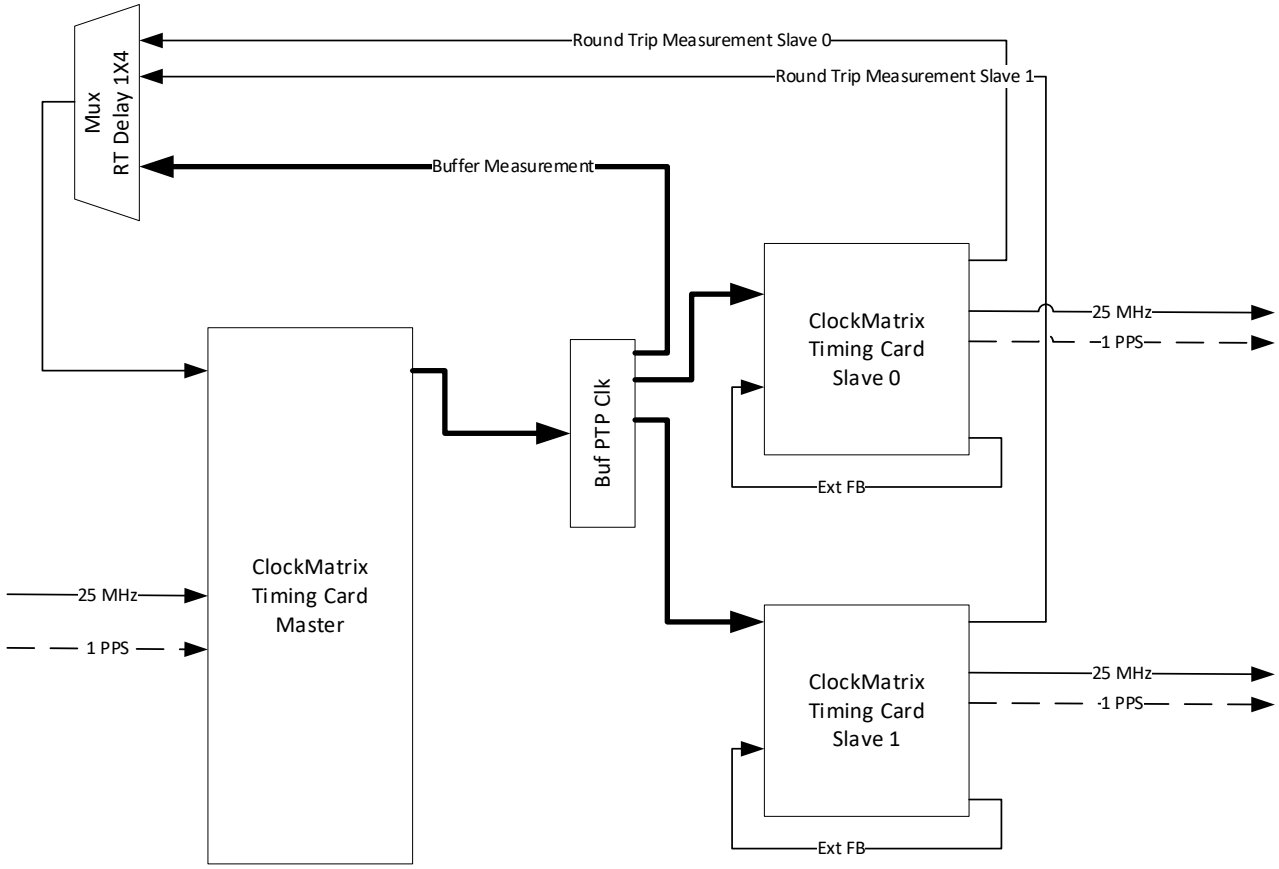

Figure 2. Example System using PWM

In Figure 2, the lines are as follows:

- Lightweight solid lines are high-speed clock signals;
- Dotted lines are 1PPS (1Hz) signals; and
- Heavyweight solid lines are high-speed clock signals with embedded 1PPS signals.

In Figure 2, a similar sequence aligns the 1PPS from the line cards to the master as in Figure 1. First, 25MHz and 1PPS external signals are fed into DPLL0 on the master timing card. DPLL0 on the master card locks to the signals as a ref-sync pair encodes the 1PPS phase on the output PWM clock. Next, the PWM output from DPLL0 at 25MHz feeds through a buffer to the DPLL0 on Line Card 1 and the DPLL0 on Line Card 2. A clock output from DPLL0 on each line card feeds back to the master timing card for a round-trip phase measurement. The round-trip measurement is from the input 25MHz on the master to the clock from the line card. (The

measurement assumes that the one-way delay across the backplane is half of the measured phase difference.) This phase adjustment is used to adjust the 1PPS and 25MHz outputs from DPLL0 on each line card individually so that the 1PPS output from each line card is aligned to the 1PPS input to the master with the required accuracy. A delay of 15 cycles of the PWM encoded clock is due to the PWM encoding and decoding process, and half of the round-trip phase measurement accounts for the delay in the cabling and the buffer.

External feedback is used on the slave ClockMatrix devices to provide the lowest input-to-output delay variation in this system. This method requires two clocks on the backplane per line card (one PWM input per line card and one PWM output per line card).

2. Configuring Master with PWM in Timing Commander

In this example, three channels are used in the configuration. Channel 0 is in DPLL mode to align the frequency with the incoming high-speed signal. Channel 1 is in ref-sync alignment mode to lock to the inputs and generate the PWM output through the combo bus with the Channel 0 frequency updates. Channels 0 and 1 have the Global Sync Enable function enabled, and the output time-to-digital converter (TDC) aligns the 25MHz output clocks. Because two 25MHz signals require alignment, the master divider should be set to 20 (500/25MHz). Channel 2 measures the round-trip delay between the high-speed input and the round-trip input.

Note: To use ref-sync mode on Channel 0, several related fast-lock registers must be set to ensure a quick-lock time to the low frequency sync input.

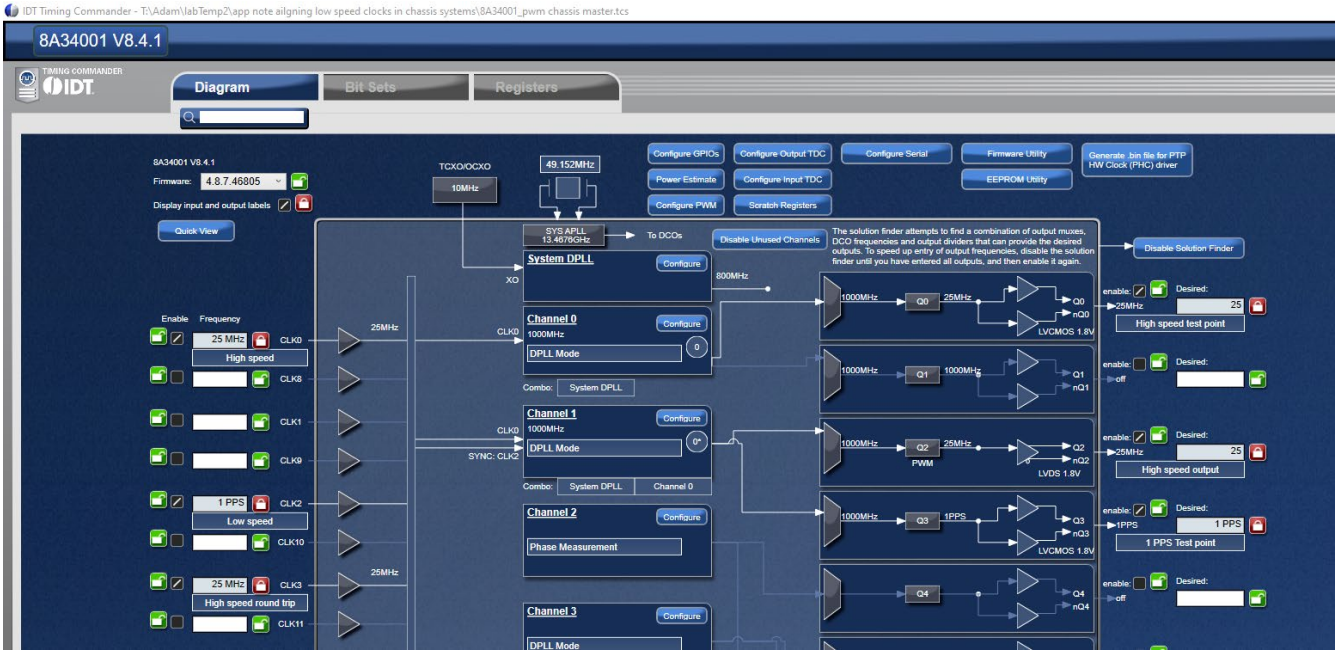

Figure 3. Overview of Configuration for Master

Figure 4. High-Speed Input for Master

Figure 5. Low-Speed Input for Master

Figure 6. High-Speed Round-Trip Input for Master

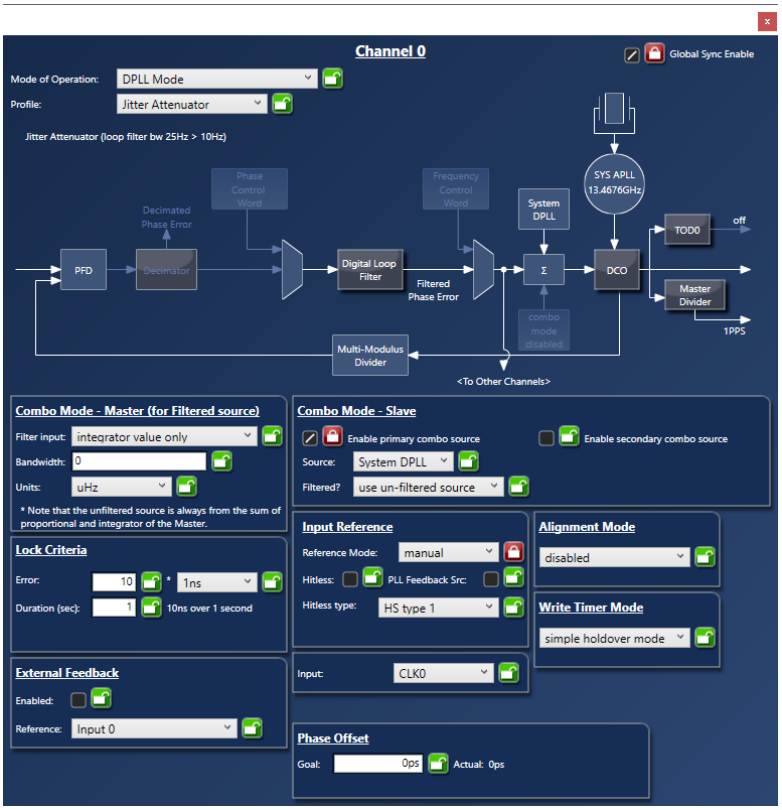

Figure 7. DPLL Channel 0 for Master

Figure 8. DPLL Channel 0 Loop Filter for Master

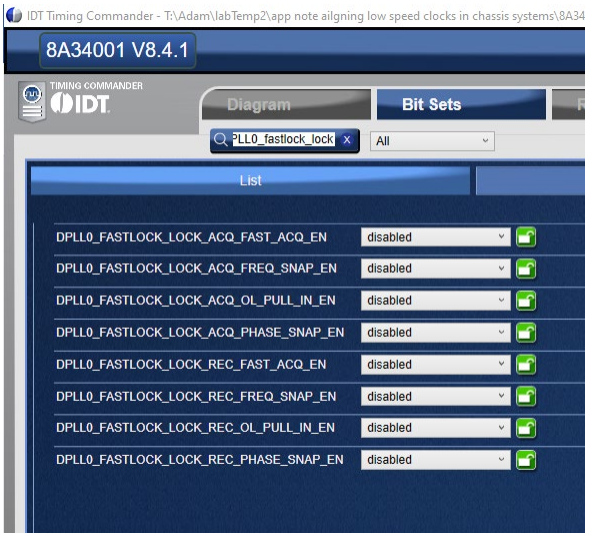

Figure 9. DPLL Channel 0 Fast Lock Settings for Master

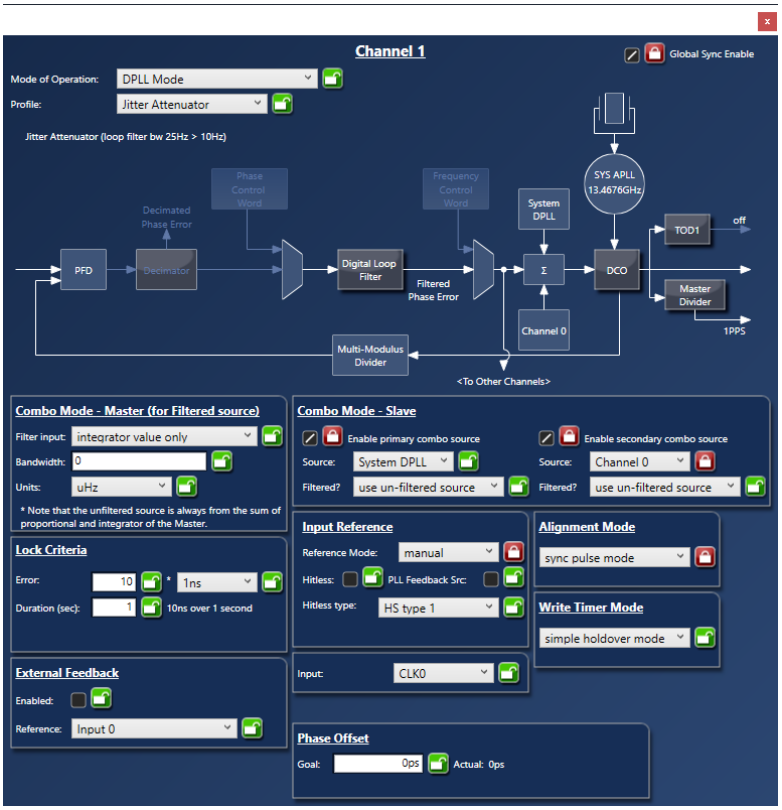

Figure 10. DPLL Channel 1 for Master

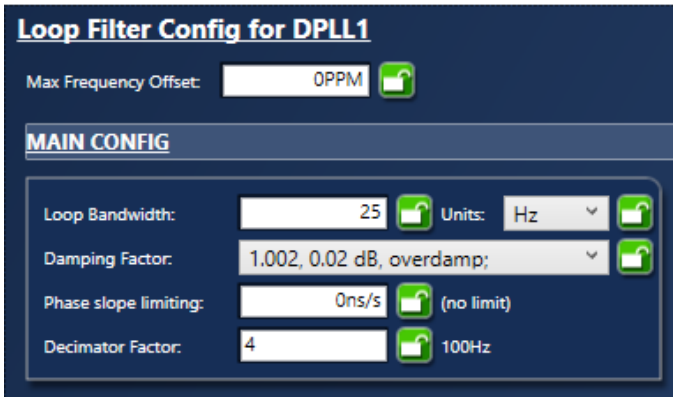

Figure 11. DPLL Channel 1 Loop Filter for Master

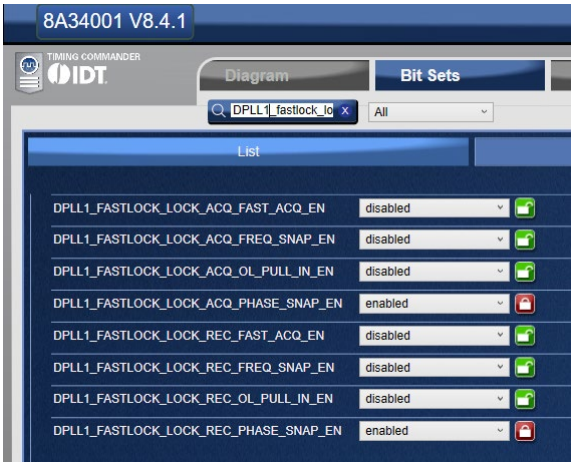

Figure 12. DPLL Channel 1 Fast Lock Settings for Master

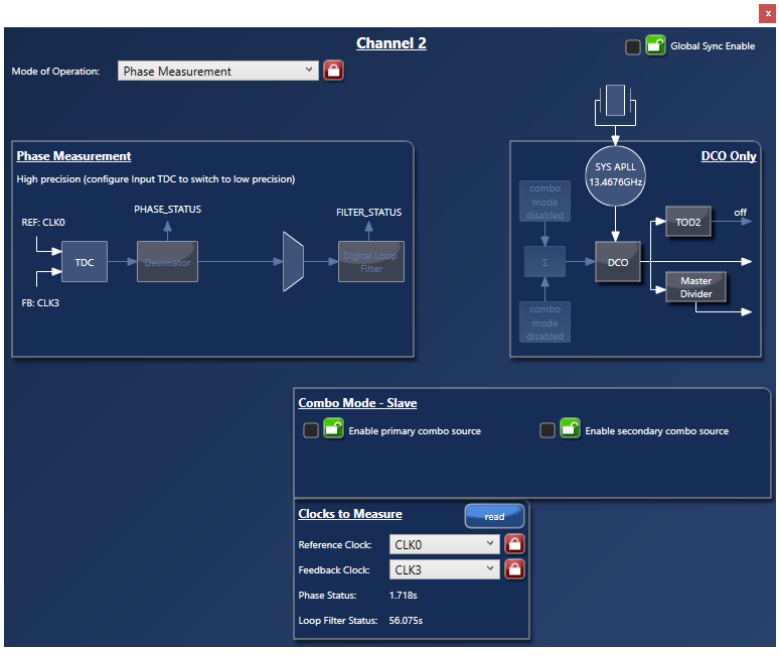

Figure 13. Phase Measurement (Channel 2) for Master

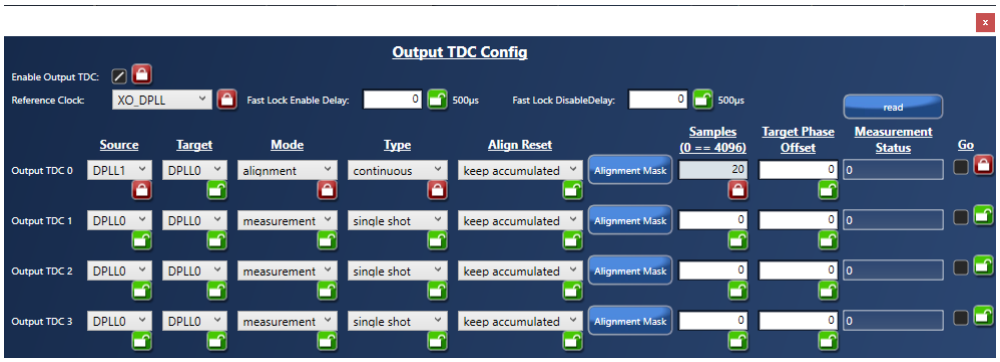

Figure 14. Output TDC for Master

Figure 15. Output TDC0 Alignment Mask for Master

Figure 16. PWM Configuration for Master

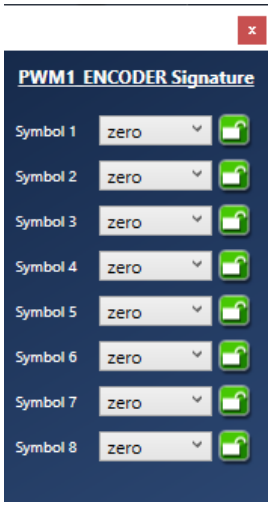

Figure 17. PWM Signature Configuration for Master

Note: For the PWM encode to operate correctly, a 1PPS signal must be configured for Q1; however, it can be set to output type “high-Z” to avoid noise on other signals, or it can be used as a test point.

3. Configuring Line Card with PWM in Timing Commander

In this example, two channels are used in the configuration. Channel 0 is in DPLL mode with external feedback and locks to the frequency and PWM encoded phase of the input signal. Channel 1 is a satellite channel that works with Channel 0 to generate additional clocks locked to the inputs. Channels 0 and 1 have the Global Sync Enable function enabled with a master divider of 20 (500/25 MHz) to align the two 25MHz outputs. The **Phase Offset** value (from the round-trip measurement on the master card) is applied only to Channel 0, and this is provided to Channel 1 through the output TDC. (The combo bus aligns the frequency of the two channels so that the output TDC only requires a small phase adjustment.)

Note: To use ref-sync mode on Channel 0, several related fast-lock registers must be set to ensure a quick-lock time to the low frequency sync input.

Note: A line card does not require a TCXO or OCXO.

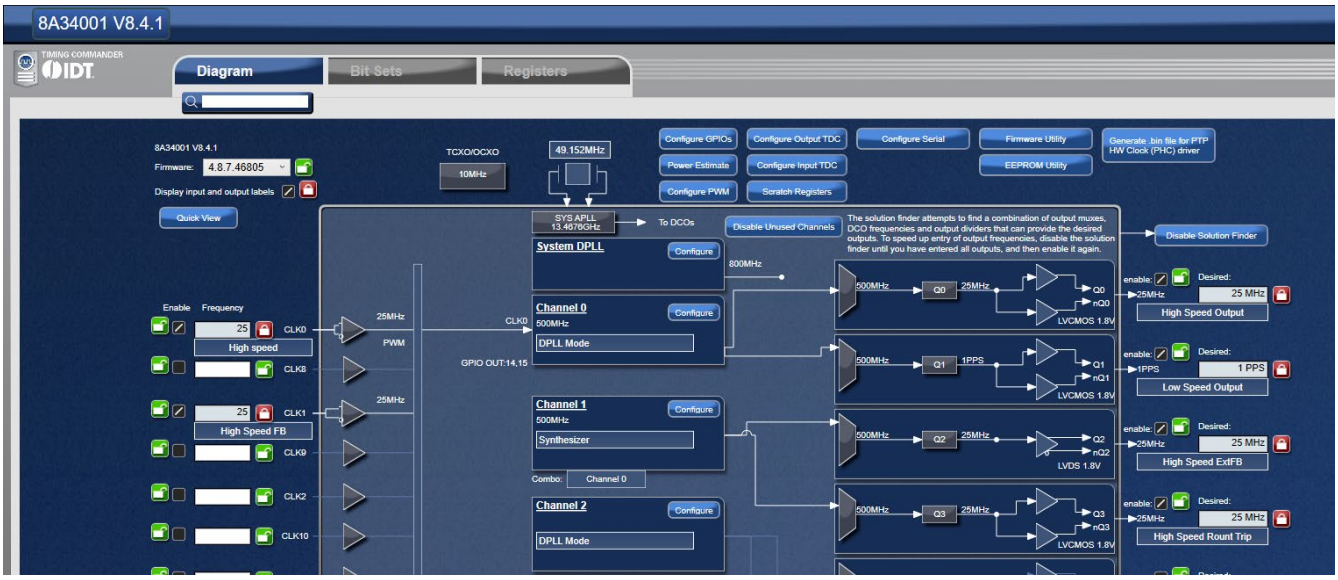

Figure 18. Overview of Configuration for Line Card

Figure 19. High-speed Input for Line Card

Figure 20. Feedback Input for Line Card

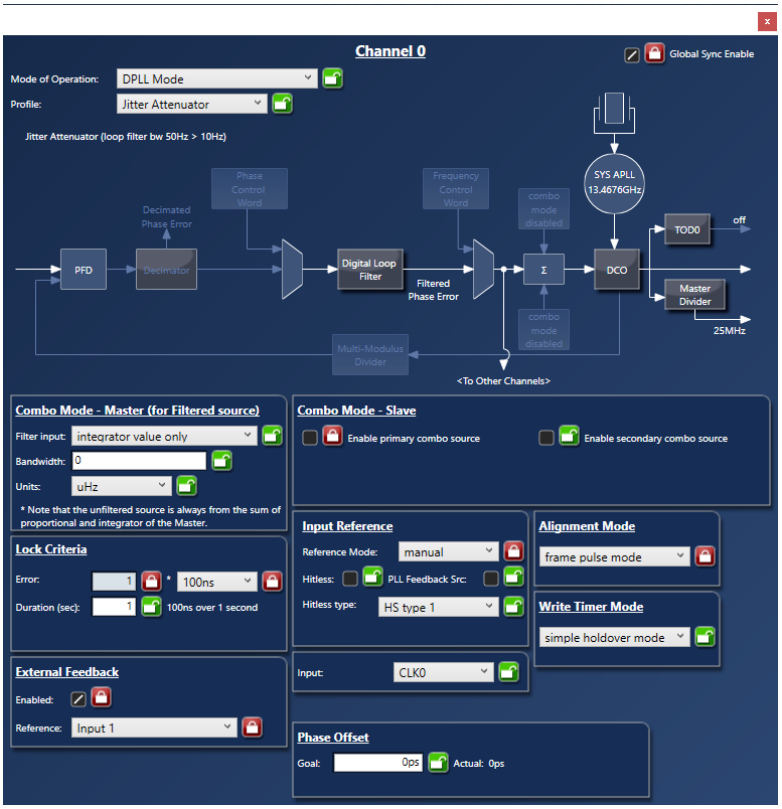

Figure 21. DPLL Channel 0 Configuration for Line Card

Figure 22. DPLL Channel 0 Loop Filter Configuration for Line Card

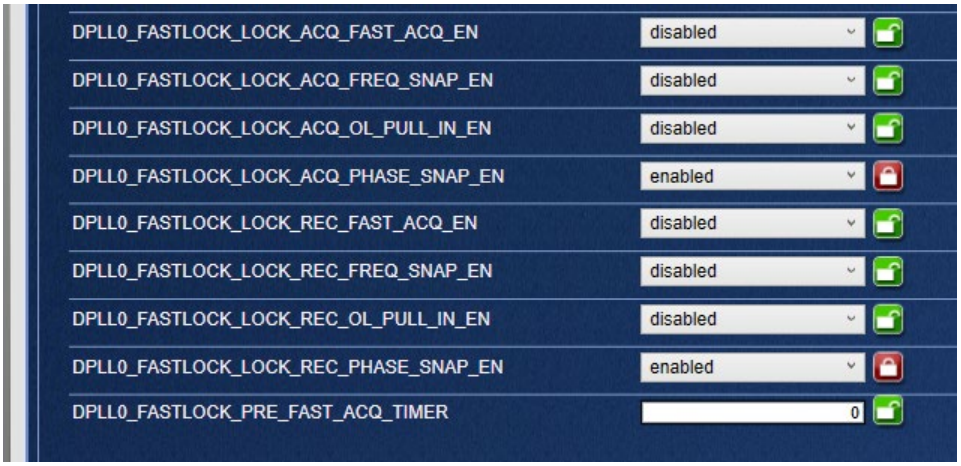

Figure 23. DPLL Channel 0 Fast Lock Register Configuration for Line Card

Figure 24. PWM Configuration for Line Card

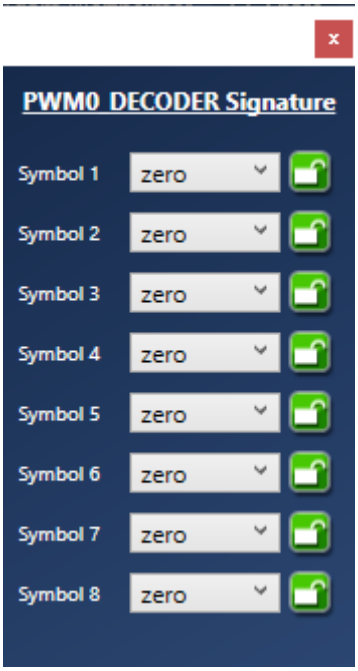

Figure 25. PWM Configuration Signature for Line Card

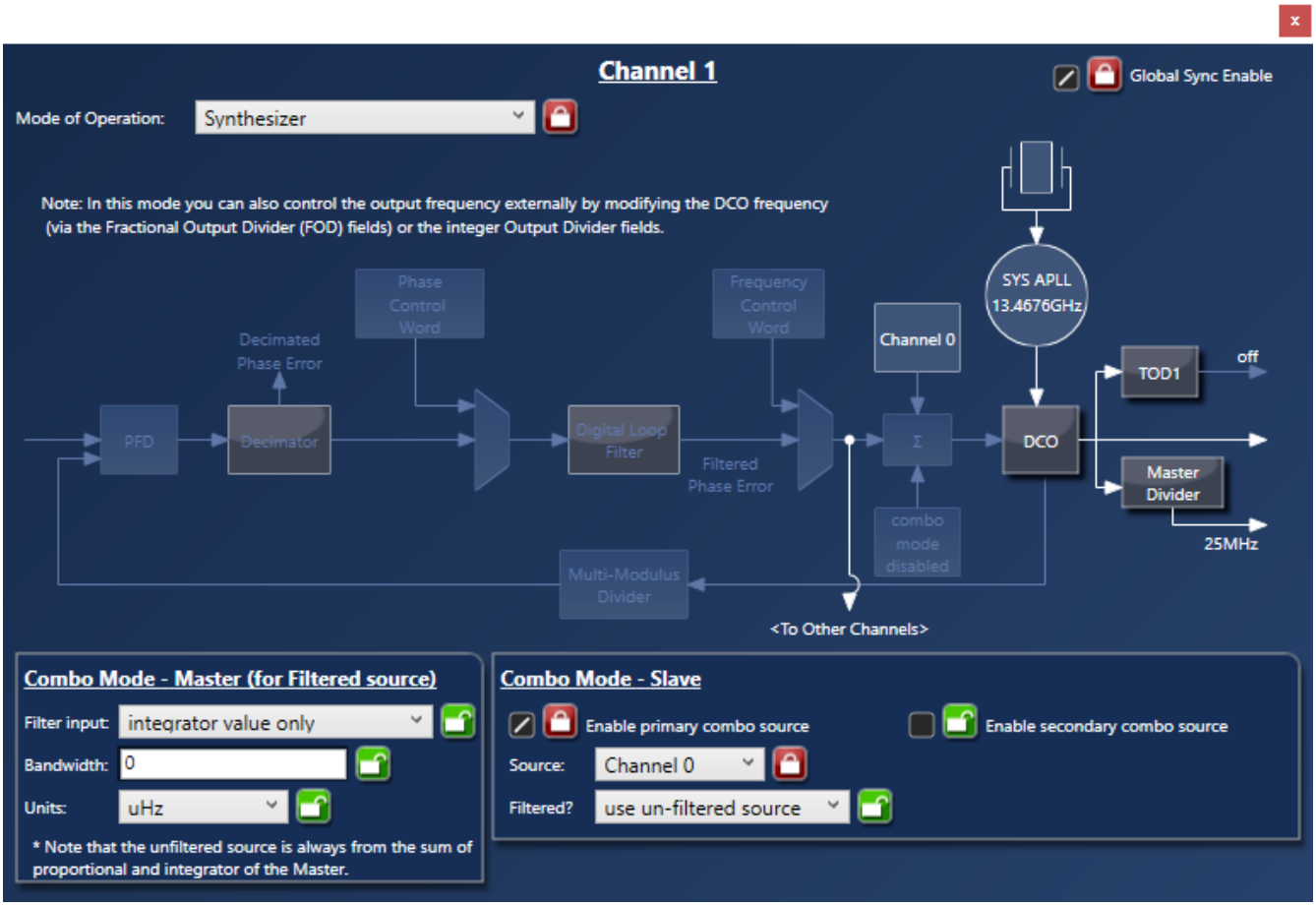

Figure 26. Synthesizer Channel 1 Configuration for Line Card

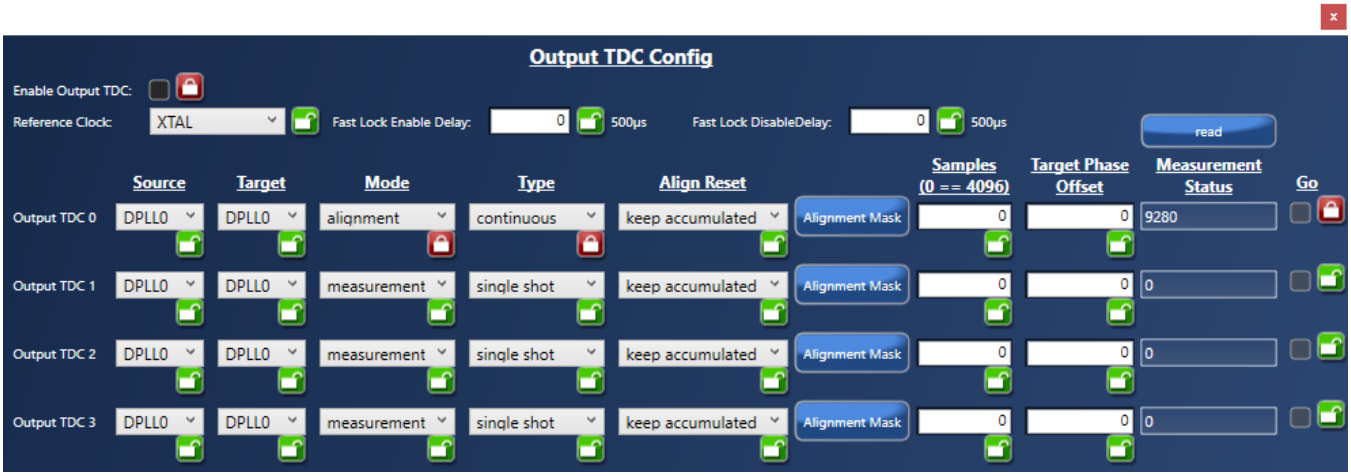

Figure 27. Output TDC for Line Card

Figure 28. Output TDC0 Alignment Mask for Line Card

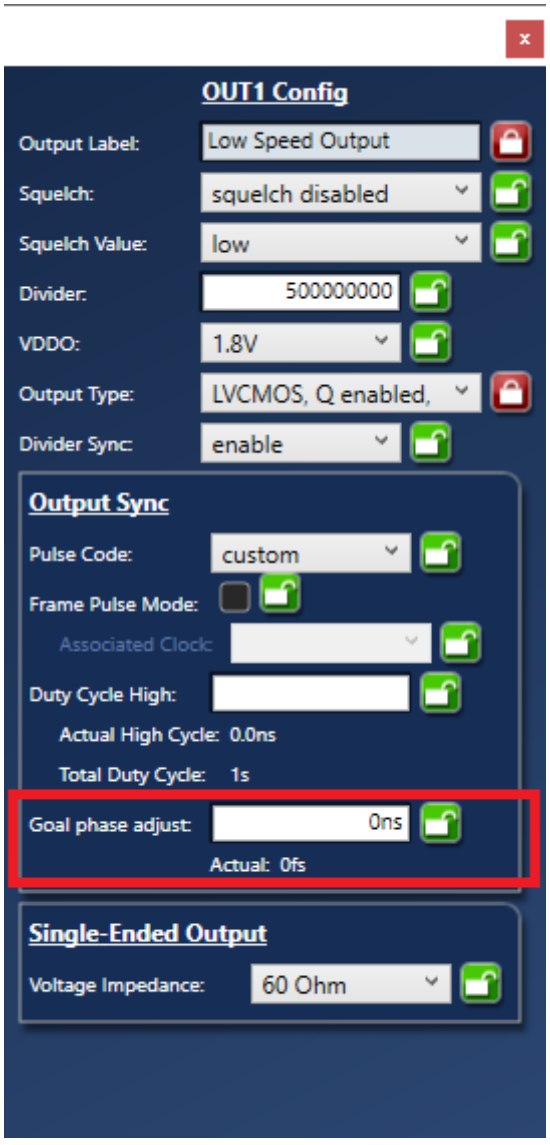

Figure 29. Output 1PPS (Q1) for Line Card

The **Goal phase adjust** for the low speed clock is where the adjustment (that is based on the individual phase measurement) is set on each line card. This value should be set to 15 periods of the PWM clock, and it should be half of the round-trip phase measurement.

4. Revision History

Revision	Date	Description
1.0	Nov.17.20	Initial release.

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