Use of HSP50216 QPDC for CDMA Applications (IS-95 and CDMA2000)

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Description

This document will explain how to use Intersil's Quad Programmable Down Converter, HSP50216, for CDMA2000 applications. It will provide details on how to combine channels in order to increase the output rate and achieve better filter performance.

Configuration 1

Input Rate: 61.44MSPS (50x)

Output Rate: 2.4576MSPS (2x)

Blocker rejection: > 48dB from 750kHz to 900kHz, > 85dB from 900kHz on

This configuration implements a 1.2288MSPS receiver in the HSP50216 using only one of the four available channels, providing up to four receivers per device. The block diagram of the implementation is shown in Figure 1. It consists of a 5th order CIC decimating by 10 followed by the filter compute engine (FCE) running both a two phase polyphase decimator and a 28-tap FIR.

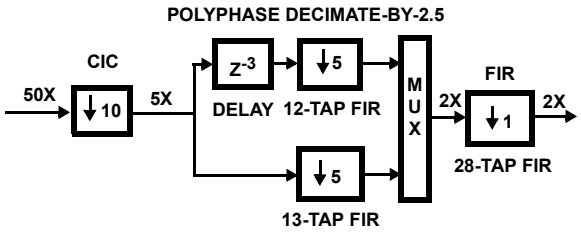

FIGURE 1. FILTER CONFIGURATION BLOCK DIAGRAM

In general, it is best to perform as much of the decimation as possible in the CIC since this avoids having to use clock cycles to write data to the FCE RAM, but this is limited by the tolerable alias level. The chosen decimation of 10 yields a first alias level of -96.135dB (see HSP50216 data sheet, Table 45 with fS/R = 0.5 / 5 = 0.10). For comparison, a CIC decimation of 25 would give an unacceptable first alias level of -52.269dB (for fS/R = 0.5 / 2 = 0.25).

The flexibility of the HSP50216's FCE is seen in the polyphase and FIR structures of Figure 1. A five-step filter sequence is used to implement it. Step 0 is a wait instruction, which waits for 5 new samples to be transferred from the CIC to the FCE's RAM. When these new samples are available steps 1 and 2 (the 12 and 13-tap FIRs, respectively) are run. The 12-tap FIR is preceded by a 3 sample delay (a read pointer offset) giving its output a total group delay of 3 + (12-1)/2 = 8.5 samples. The 13-tap FIR's group delay, (13-1)/2 = 6, differs by 2.5 samples. Together, these polyphase FIRs generate two equally-spaced output samples for each five new input samples. When multiplexed together, the result is a decimation of 2.5. These outputs are sent to filter sequence step number 3, a 28-tap FIR. Step 4, the final step, is a loop back to step 0's wait for five new input samples. This FCE program, along with the filter coefficient data, is provided in the import filter file.

Frequency responses of the polyphase decimator and 28-tap FIR are provided in Figures 2 and 3. From Figure 2, the first alias level for decimation by 5 is about -94dB. The loss at high frequencies in the polyphase is compensated for by the gain in the 28-tap FIR (Figure 3).

Figures 4, 5, and 6 provide show a complete frequency response of the configuration by doing an actual sweep of the part. The plots used a frequency step of 1kHz and are normalized to a 0dB maximum.

The overall decimation of 50X / 2X = 25 allows 24 bit I and Q data to be available at the serial outputs.

Analysis of computation clock usage:

Available clocks per output = 50 / 2 = 25.

TABLE 1.

CLOCKS	FUNCTION
2	Overhead (Wait, Loop).
5	Input Writes from CIC to FCE.
6	12-Tap FIR Computation.
7	13-Tap FIR Computation.
2	2 Input Writes to 28-tap FIR.
28	2 Runs of 28-Tap FIR (One for Each Polyphase Output) X 14 Clocks Per Run.
50	Total Clocks to Compute 2 Outputs

All available clocks are used to implement this configuration.

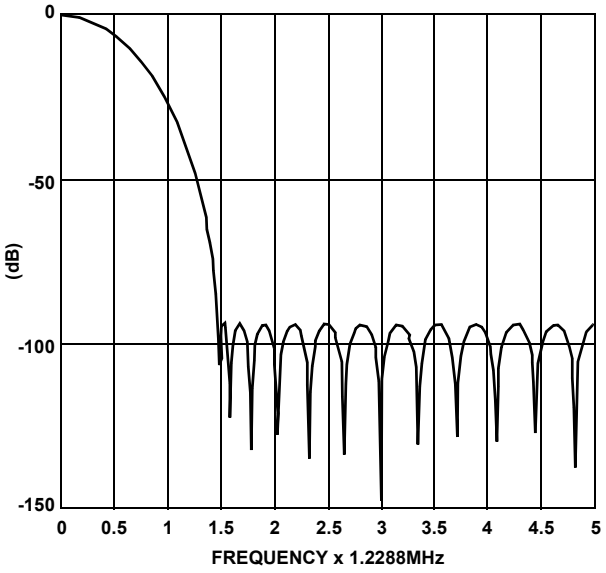

FIGURE 2. POLYPHASE DECIMATOR FREQUENCY RESPONSE, 25-TAP IMPULSE

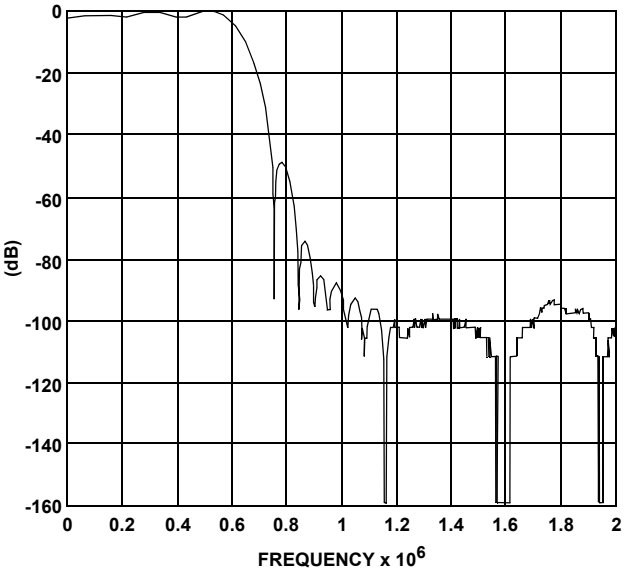

FIGURE 4. FREQUENCY SWEEP OF THE FILTER AS IMPLEMENTED ON THE HSP50216

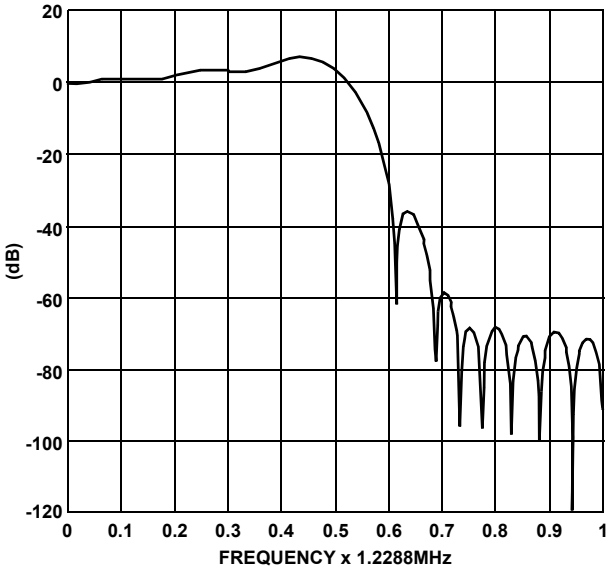

FIGURE 3. 28-TAP FIR FREQUENCY RESPONSE

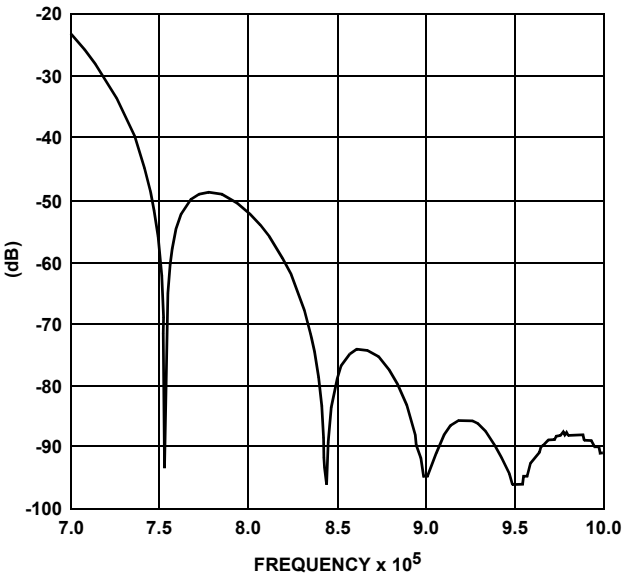

FIGURE 5. FREQUENCY SWEEP ZOOMED IN AROUND 750kHz AND 900kHz BLOCKER FREQUENCIES

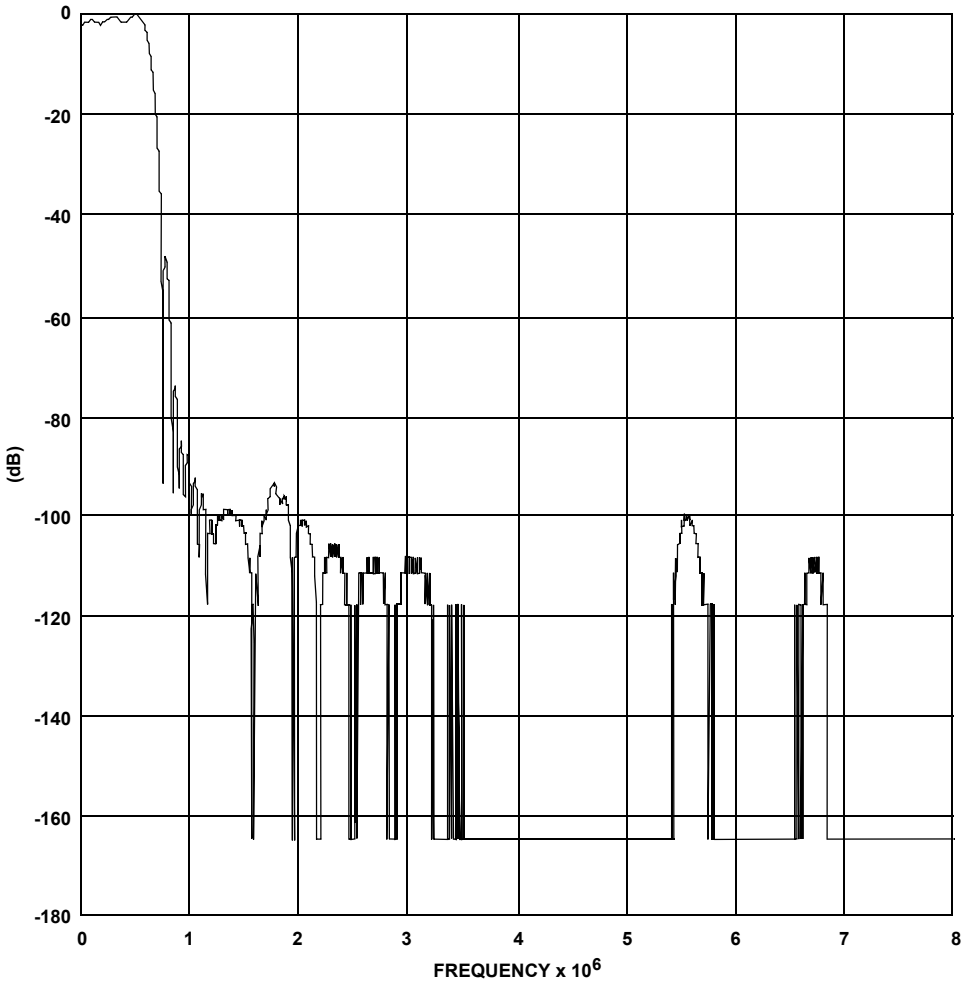

FIGURE 6. FREQUENCY SWEEP FROM DC TO 8MHz

Configuration 2

Input Rate: 61.44MSPS (50x)

Output Rate: 2.4576MSPS (2x)

Blocker Rejection: > 65dB from 750kHz to 900kHz, > 103dB from 900kHz On

This configuration implements a 1.2288MSPS receiver in the HSP50216 using two of the four available channels, providing up to two receivers per device. The block diagram of the implementation of two receivers is shown in Figure 7 below. It consists of, in the first channel, a 5th order CIC decimating by 10 followed by the filter compute engine (FCE) running a two-phase polyphase decimator and, in the second channel, a 44-tap FIR.

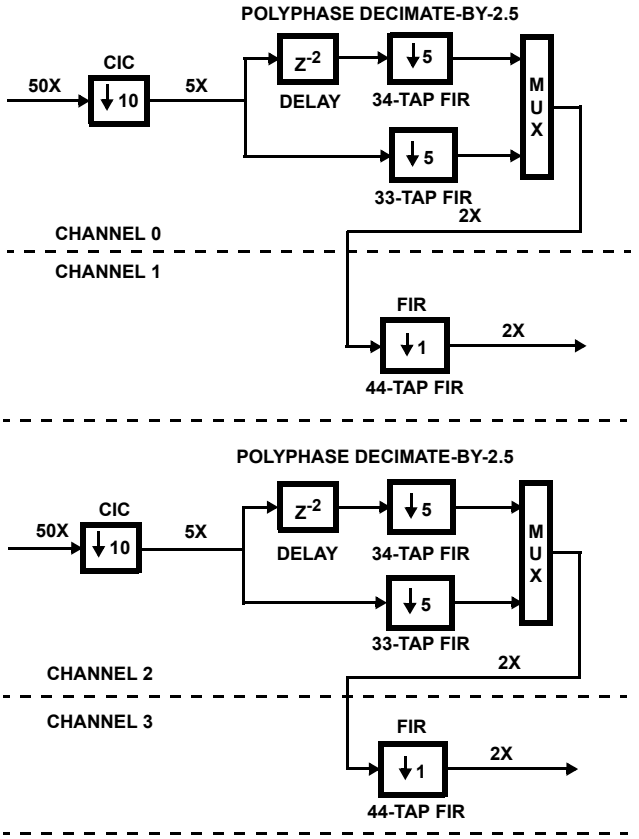

FIGURE 7. FILTER CONFIGURATION BLOCK DIAGRAM FOR TWO RECEIVERS

As shown in the first configuration, the chosen decimation of 10 in this configuration with a 50X input yields a first alias level of -96.135dB.

The decimate-by-2.5 filter is implemented in the FCE as a 4-step sequence. Step 0 is a wait instruction, which waits for 5 new samples to be transferred from the CIC to the FCE's RAM. When these new samples are available steps 1 and 2 (the 34 and 33-tap FIRs, respectively) are run. The 34-tap FIR is proceeded by a 2 sample delay (a read pointer offset) giving its output a total group delay of 2 + (34-1)/2 = 18.5 samples. The 33-tap FIR's group delay, (33-1)/2 = 16, differs by 2.5 samples. Together, these polyphase FIRs generate two equally-spaced output samples for each five new input samples. When multiplexed together, the result is a decimation of 2.5. These outputs are sent to the FCE of the next channel, which runs a 44-tap FIR. Step 3, the final step of the polyphase sequence, is a loop back to step 0's wait for five new input samples. This FCE program, along with the polyphase filter coefficient data, is provided in the import filter file.

Frequency responses of the polyphase decimator and 44-tap FIR are provided in Figures 8 and 9. From Figure 8, the first alias level in the signal bandwidth for decimation by 5 is about -120dB.

Figures 10, 11, and 12 provide show a complete frequency response of the configuration by doing an actual sweep of the part. The plots used a frequency step of 1kHz and are normalized to a 0dB maximum.

The overall decimation of 50X / 2X = 25 allows 24 bit I and Q data to be available at the serial outputs.

Analysis of Computation Clock Usage

Channel 0

Available clocks per output = 50 / 2 = 25

CLOCKS	FUNCTION
2	Overhead (Wait, Loop)
5	Input Writes from CIC to FCE
17	34-Tap FIR Computation
17	33-Tap FIR Computation
41	Total Clocks to Compute 2 Outputs

Channel 0 has 50 clocks available to produce 2 outputs (25 clocks per output), but its configuration uses only 41. These available 9 clock cycles permit up to an additional 18 taps to be added to channel 0's filtering if desired.

Channel 1

Available clocks per output = 25 (same as channel 0)

CLOCKS	FUNCTION
2	Overhead (Wait, Loop)
2	Input Writes from Channel 0's FCE to Channel 1's FCE
44	2 Runs of the 44-Tap Filter x 22 Clocks Per Run
48	Total Clocks to Compute 2 Outputs

Channel 1's configuration uses 48 of its available 50 clocks in computing two output samples. An additional 4 taps could be added to this filter if desired.

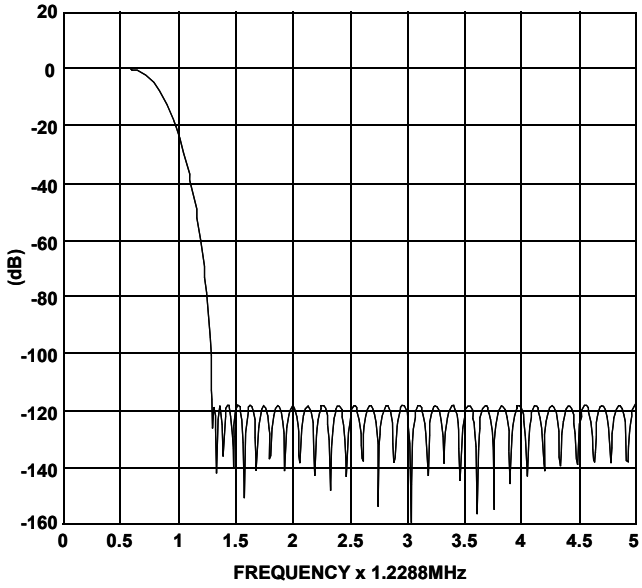

FIGURE 8. POLYPHASE DECIMATOR FREQUENCY RESPONSE, 67-TAP IMPULSE

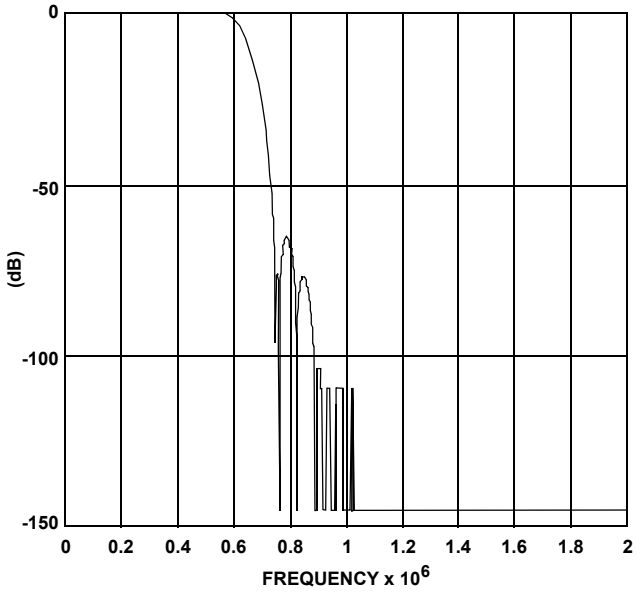

FIGURE 10. FREQUENCY SWEEP OF THE FILTER AS IMPLEMENTED ON THE HSP50216

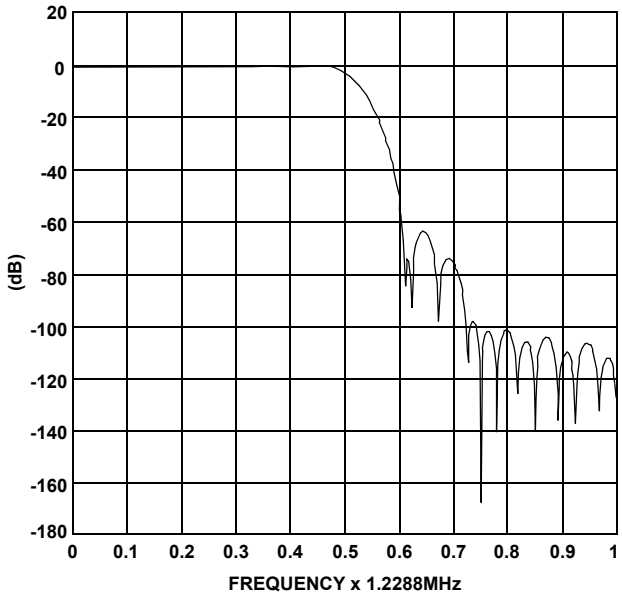

FIGURE 9. 44-TAP FIR FREQUENCY RESPONSE

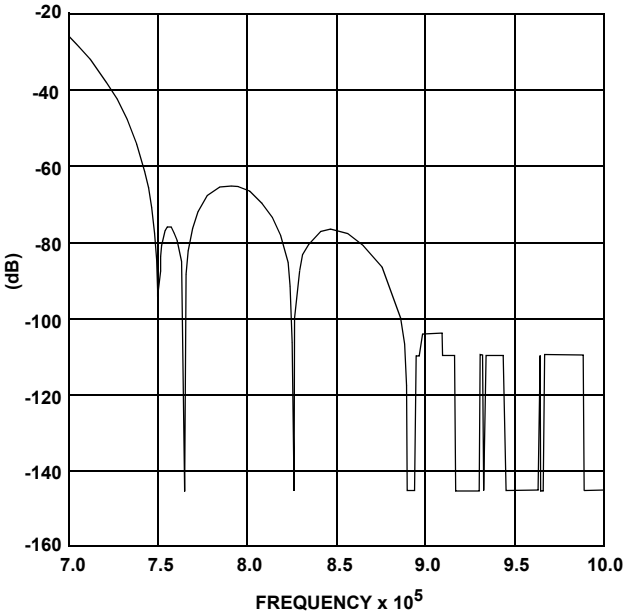

FIGURE 11. FREQUENCY SWEEP ZOOMED IN AROUND 750kHz AND 900kHz BLOCKER FREQUENCIES

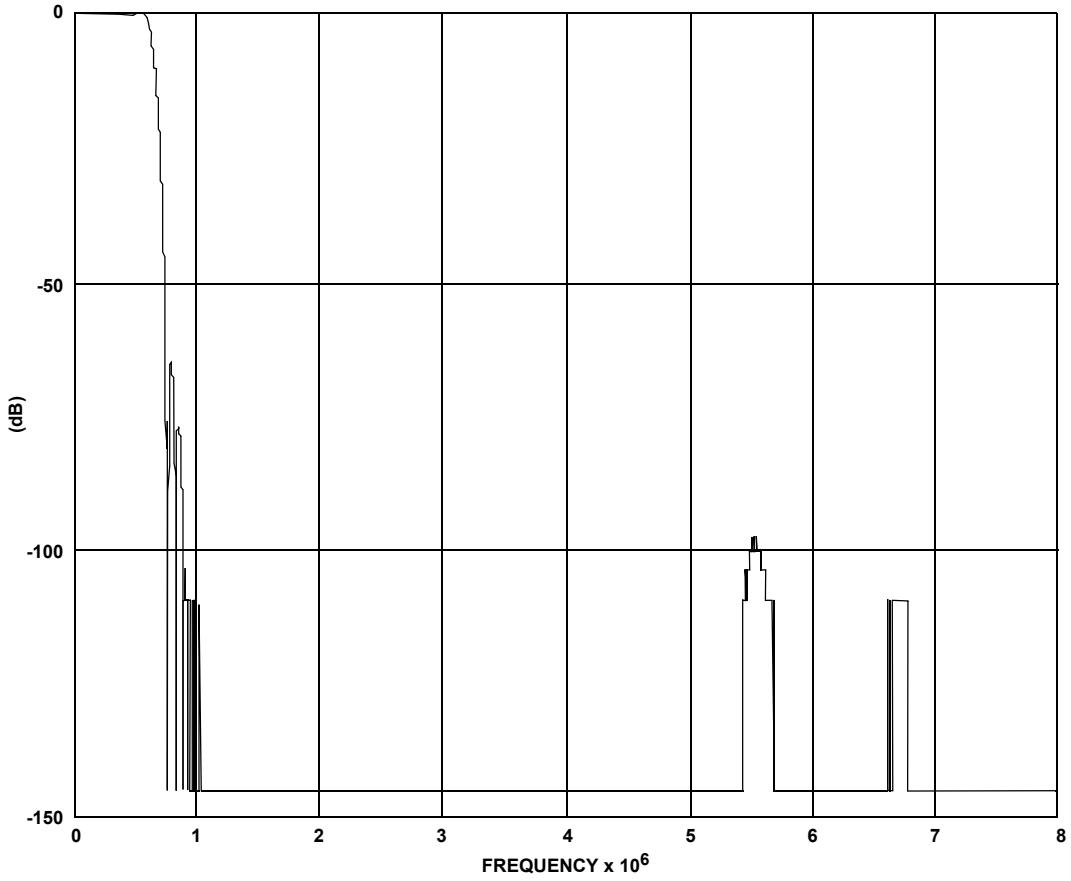

FIGURE 12. FREQUENCY SWEEP TO 8MHz

Use of HSP50216 EVAL Software for this Application

The eval board software is the perfect tool to evaluate performance of the part, configure registers, verify filter designs, and display the I/Q constellation and spectrum of the output. Connectivity to the eval board is supported only by Windows 95 and 98, however Windows NT and 2000 may be used for generating the register value files which may be downloaded to the chip with the user's own hardware.

NOTE: The software can configure the register value files even if the HSP50216/ ISL5216 Evaluation Board is not connected.

The configuration file is loaded by selecting option 8 in the main menu of the software. Enter only the root name of the configuration, where the root name is the file name preceding the .0, .1, .2, .3 and .top file extensions.

Figure 14 shows the channel 0 data path settings for Configuration 1 (in the configuration files for this example, channels 1, 2 and 3 are configured the same as channel 0). It shows the 61.44MSPS input rate, 5th order CIC decimation of 10, and an NCO center frequency as well as the source input bus. The imported filter program specified in options 13, 27 and 28 contains both the FCE program and 12, 13 and 28-tap FIR coefficients (see Figure 1). Imported filters are hand-coded filter programs which bypass the software's automatic register value generation.

When loading of the configuration is completed (main menu option 8), initialize the eval board using option 17, compute the register value files using option 10, and download the register values to the '216 using option 12. Finally, select run and display (option 13) to see the '216 output in real time.

As noted previously, if only register values are needed, option 10 in the Main Menu will compute register values for each of the channels, and store them in the files file_name.r0, file_name.r1, file_name.r2, file_name.r3 and file_name.rtp where file_name is name entered into the load or save configuration options (8 and 9) from the main menu. These files are human readable text files containing register numbers and values in hex.

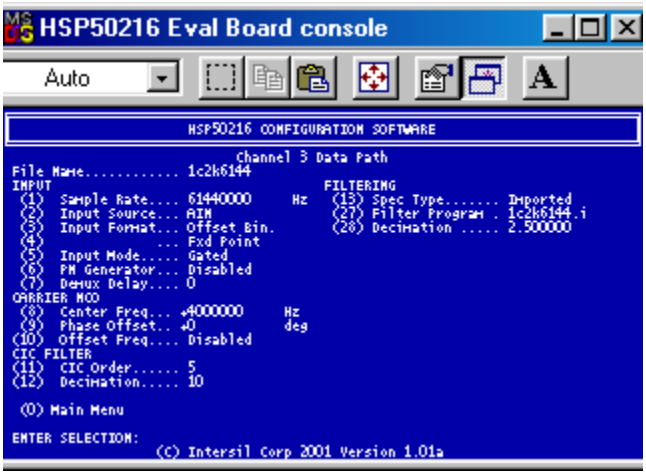

FIGURE 13. EVAL BOARD SOFTWARE MAIN MENU

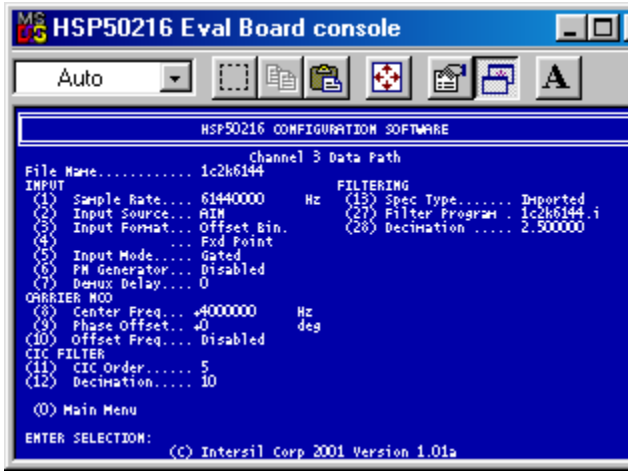

FIGURE 14. EVAL BOARD SOFTWARE DATA PATH MENU

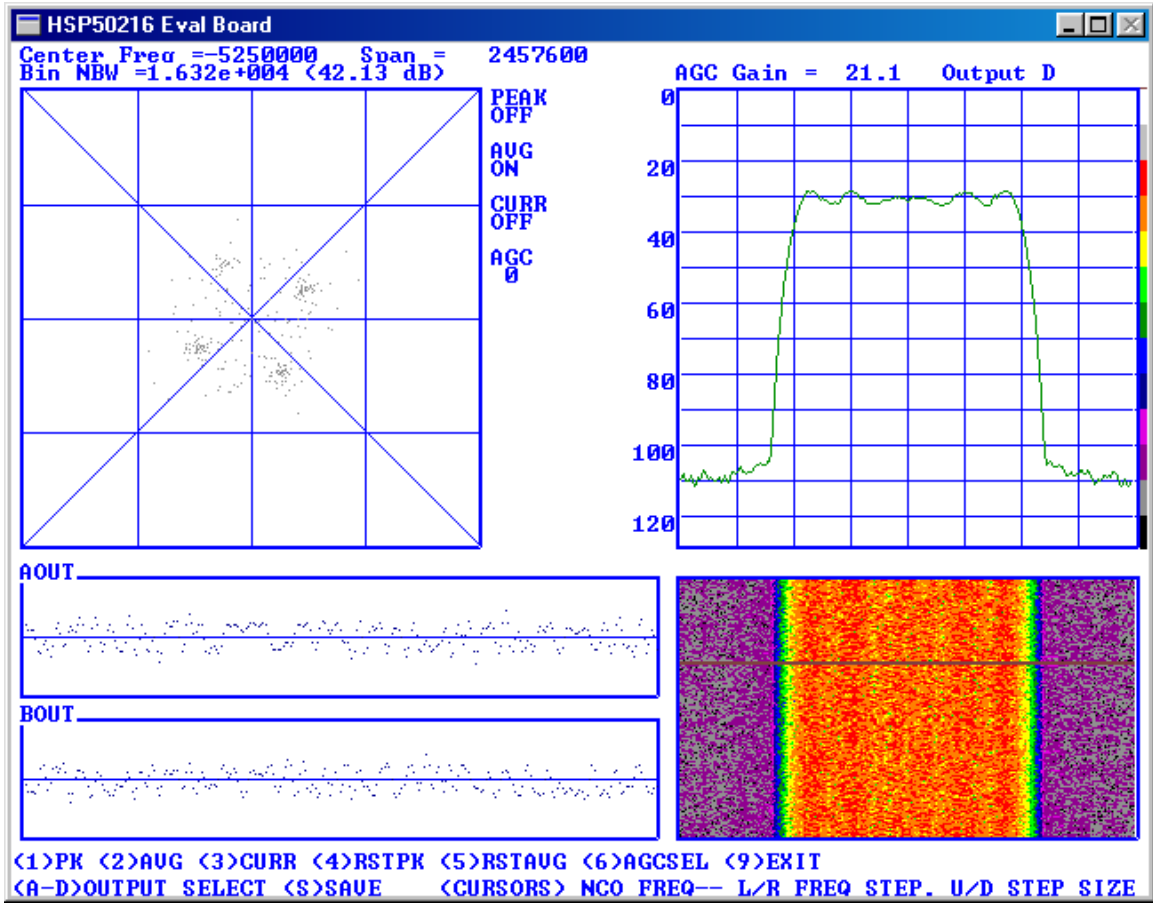

FIGURE 15. SCREEN SHOT FROM HSP50216 EVALUATION BOARD SOFTWARE

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