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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Super Low Power Series

Averaging the Results of Measurement by ΔΣA/D Converter

Introduction

The ΔΣA/D converter is used to measure the voltage input to the Ain1 pin. The external input voltage provides the reference voltage for the ΔΣA/D converter. The data created after 64 rounds of conversion are averaged and the results are saved in the internal RAM as 14-bit data.

Target Device

H8/38086R

Contents

1. Specifications

- As is shown in figure 1, the ΔΣA/D converter of the H8/38086R is used to measure the voltage input to the Ain1 pin.
- The external input voltage provides the reference voltage for the ΔΣA/D converter.
- The voltage to be measured is applied to the Ain1 pin. It is then A/D converted, and the data thus created are averaged and saved to the internal RAM. 65 rounds of A/D conversion are executed. The data created in the first round of conversion are discarded, and those from the second and later rounds are used. Also, the A/D-converted data read from the A/D Data Register (ADDR) are shifted 2 bits right and handled as 14-bit data. The 14-bit data created in the 64 rounds of A/D conversion are added together, and the result of addition is shifted 6 bits right and saved in the internal RAM.
- The mode of operation is the wait mode. The oversampling frequency is ϕ. The A/D conversion is executed with the programmable-gain amplifier (PGA) bypassed.
- The operating mode is switched to sleep (high-speed) mode during A/D conversion since this minimizes the noise generated by the CPU. The A/D conversion end interrupt takes the chip out of sleep (high-speed) mode and places it in the active (high-speed) mode. The data generated by A/D conversion are then stored in the internal RAM. The module standby function is used to place internal peripheral functions other than the ΔΣA/D converter, such as SCI3, timer F, IIC2, the A/D converter, RTC, TPU, PWM, watchdog timer, and LCD internal peripheral module, on module standby.

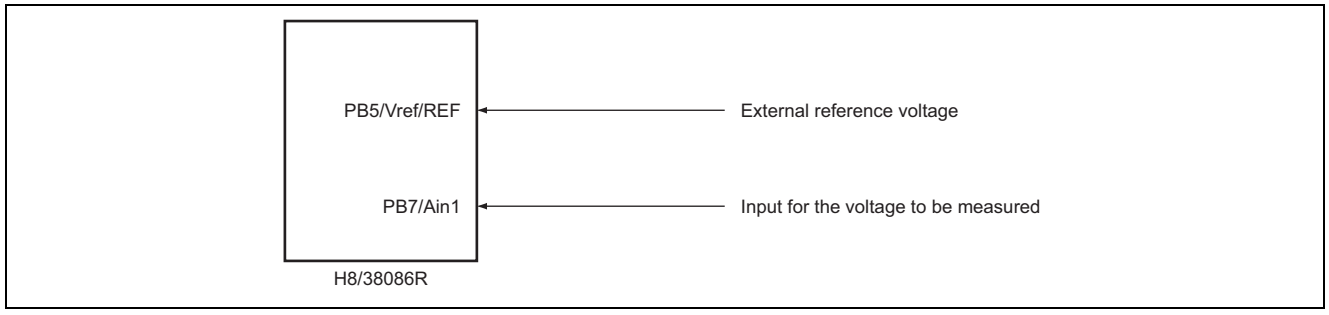


Figure 1 Setup of the ΔΣA/D Converter for Measurement Results to be Averaged

2. Measurement conditions

Figure 2 shows the measuring circuit in this sample task.

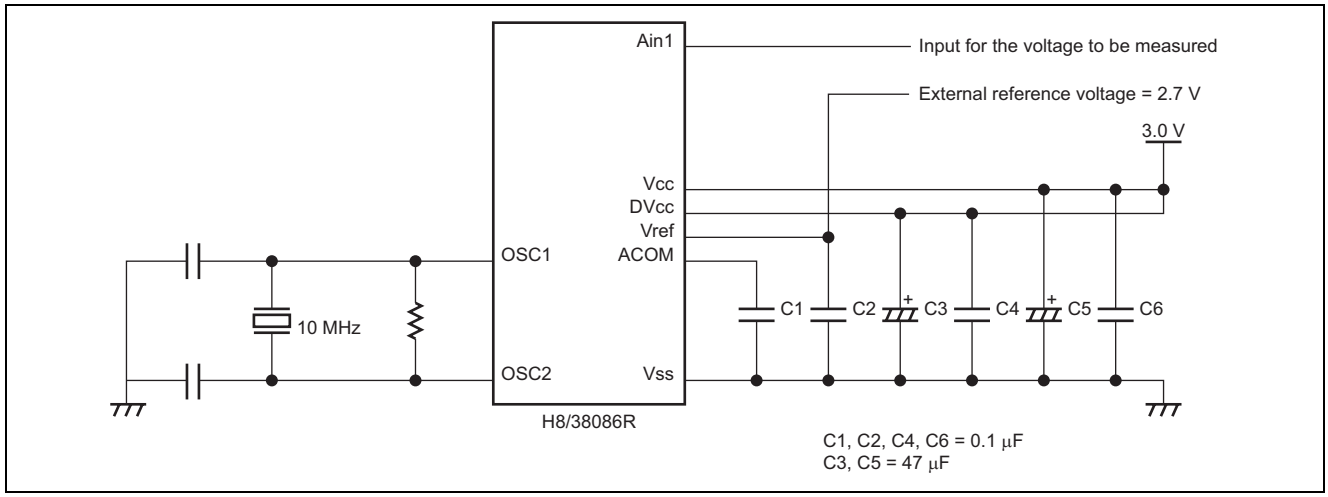


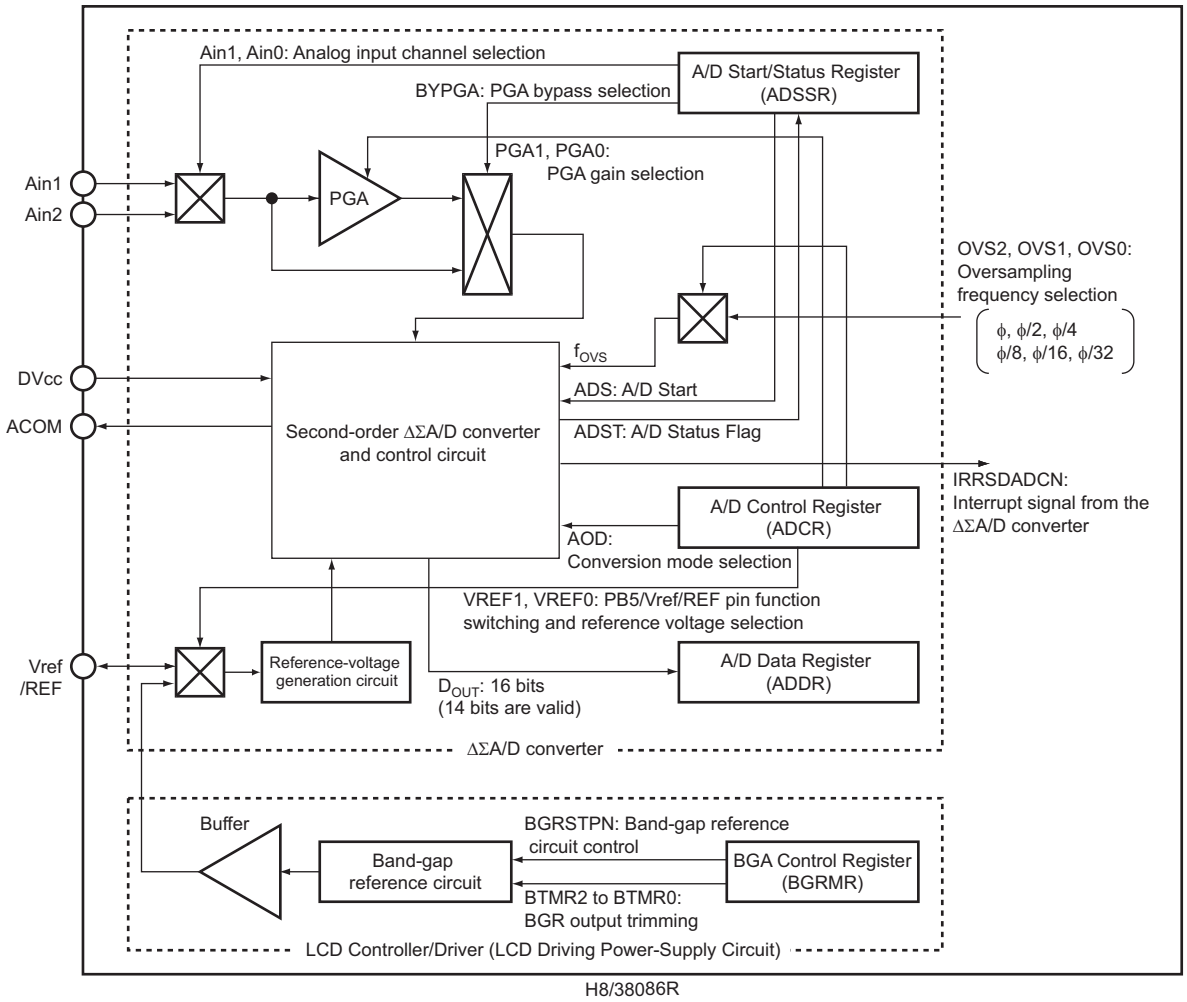
Figure 2 ΔΣA/D Converter Measuring Circuit (When Using an External Reference Voltage)

Conditions for voltage measurement with the ΔΣA/D converter using an external reference voltage are as follows.

- Vcc = 3.0 V
- DVcc = 3.0 V
- Vref = Externally input 2.7 V
- System clock frequency (ϕ) = 10 MHz
- Oversampling frequency (fovs) = ϕ
- PGA = bypass
- Conversion mode = wait mode
- Range of input voltage = 0.2 to 2.7 V (Vref)

3. Description of functions used

Figure 3 is a block diagram of the ΔΣA/D converter.



[Legend]
DVcc: ΔΣA/D Converter Analog Power-Supply Pin
Ain1: Analog Input Pin 1
Ain2: Analog Input Pin 2
Vref: Reference Voltage Pin
REF: Internal Reference Voltage Output Pin
ACOM: Analog Voltage Stabilization Pin

Figure 3 Block Diagram of the ΔΣA/D Converter

Functions of the ΔΣA/D converter are described below.

3.1 Assignment of pin functions

Table 1 shows the assignment of pin functions used for the ΔΣA/D converter.

Table 1 Assignment of Pin Functions

Pin	Function
Vref/REF	As the Vref input pin, input for the external reference voltage (2.7 V dc)
DVcc	As the power-supply pin for the ΔΣA/D converter, input for 3.0 V dc
Ain1	As the analog input pin, input for the voltage to be measured
Ain2	Not used
ACOM	As the analog voltage stabilization pin, for connection to a 0.1-µF capacitor

4. Principle of averaging the results of measurement by the ΔΣA/D converter

Figure 4 illustrates averaging of the results of measurement by the ΔΣA/D converter

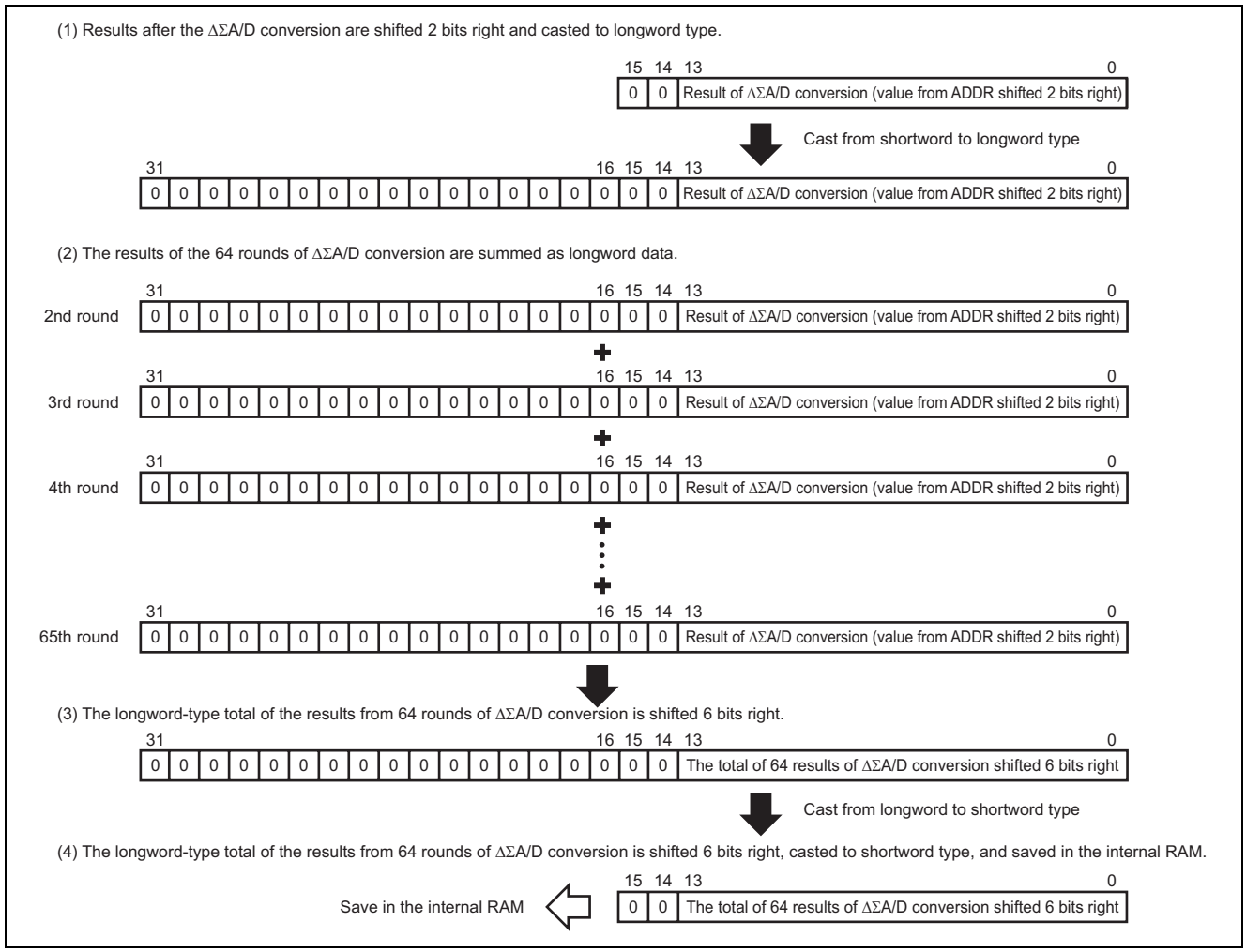


Figure 4 Averaging of the Results of Measurement by the ΔΣA/D Converter

5. Description of software

5.1 Description of internal I/O register usage

Internal I/O registers used in this sample task are described below.

- A/D Data Register (ADDR) Address: H'F062

Bit	Bit Name	Initial value	R/W	Description
15	ADD13	—	R	16-bit read-only register that holds the results of A/D conversion. The 14 bits of A/D-converted data are stored in the higher-order 14 bits. The ADDR value during A/D conversion is undefined.
14	ADD12	—	R	
13	ADD11	—	R	
12	ADD10	—	R	
11	ADD9	—	R	
10	ADD8	—	R	
9	ADD7	—	R	
8	ADD6	—	R	
7	ADD5	—	R	
6	ADD4	—	R	
5	ADD3	—	R	
4	ADD2	—	R	
3	ADD1	—	R	
2	ADD0	—	R	
1	—	—	—	—
0	—	—	—	

- A/D Control Register (ADCR) Address: H'F060

Bit	Bit Name	Initial value	R/W	Description
7	MOD	0	R/W	Conversion Mode Select Sets the conversion mode. While the MOD bit is set to 1, A/D conversion is executed regardless of the value of the ADS bit in ADSSR. 0: Wait mode 1: Continuous mode
6	OVS2	0	R/W	Oversampling Frequency Select
5	OSV1	0	R/W	Select the oversampling frequency.
4	OVS0	0	R/W	000: φ 001: φ/2 010: φ/4 011: φ/8 100: φ/16 101: φ/32 11x: Setting prohibited
3	VREF1	0	R/W	PB5/Vref/REF Pin Function Switch and Reference Voltage
2	VREF0	1	R/W	Select Specify whether the PB5/Vref/REF pin functions as a PB5 pin, Vref pin, or REF pin. In addition, these bits select the external reference voltage (Vref) or internal reference voltage (REF) as the reference voltage for the ΔΣA/D converter. If REF is to be selected, set these bits after setting the BGRSTPN bit in BGRMR to 1 so that the BGR operates. 00: Functions as a PB5 input pin 01: Functions as a Vref input pin, and the external reference voltage (Vref) is input to the reference generator 10: Functions as a REF output pin 11: Functions as a REF output pin, and the internal reference voltage (REF) is input to the reference generator When these bits are set to B'11, the REF voltage is input to the reference voltage generator in the ΔΣA/D converter at the same timing as the internal reference voltage (REF) is output from the REF pin. To operate the ΔΣA/D converter with the internal reference voltage (REF), set these bits to B'11.
1	PGA1	0	R/W	PGA Gain Select
0	PGA0	0	R/W	Set the analog input voltage multiplication ratio to a value from 1/3 to 4. 00: 1 01: 2 10: 4 11: 1/3

Note: x: Don't care

- A/D Start/Status Register (ADSSR) Address: H'F061

Bit	Bit Name	Initial value	R/W	Description
7	ADS	1	R/W	A/D Start When this bit is set to 1 in wait mode (the MOD bit in ADCR is cleared to 0), A/D conversion is started.
6	ADST	—	R	A/D Status Flag When this bit is read in wait mode (the MOD bit in ADCR is cleared to 0), A/D conversion status can be identified. 0: In the idle state 1: A/D conversion in progress
5	AIN1	0	R/W	Analog Input Channel Select
4	AIN0	1	R/W	Select the analog input channel. 00: Not selected 01: Ain1 10: Ain2 11: Not selected
3	BYPGA	1	R/W	PGA Bypass Select Selects whether the analog input is to the PGA or second-order ΔΣA/D converter. 0: To the PGA 1: To the second-order ΔΣA/D converter
2	—	—	—	Reserved
1	—	—	—	These bits cannot be modified.
0	—	—	—	

- Interrupt Enable Register 2 (IENR2) Address: H'FFF4

Bit	Bit Name	Initial value	R/W	Description
5	IENSAD	1	R/W	ΔΣA/D Converter Interrupt Request Enable The ΔΣA/D converter interrupt request is enabled when this bit is set to 1. 0: ΔΣA/D converter interrupt request is disabled. 1: ΔΣA/D converter interrupt request is enabled.

- Interrupt Request Register 2 (IRR2) Address: H'FFF7

Bit	Bit Name	Initial value	R/W	Description
5	IRRSAD	0	R/(W)*	ΔΣA/D Converter Interrupt Request Flag [Setting condition] Completion of ΔΣA/D conversion [Clearing condition] Writing of 0 to this bit

Note: * The only effective write value is 0, which clears the flag.

- System Control Register 1 (SYSCR1) Address: H'FFF0

Bit	Bit Name	Initial value	R/W	Description
7	SSBY	0	R/W	Software Standby Selects the mode to be entered after execution of the SLEEP instruction. 0: The transition is to sleep mode or subsleep mode. 1: The transition is to standby mode or watch mode.
3	LSON	0	R/W	Low-Speed On Flag Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock on exit from watch mode. 0: The CPU operates from the system clock (ϕ) 1: The CPU operates from the subclock (ϕ_{SUB})

- System Control Register 2 (SYSCR2) Address: H'FFF1

Bit	Bit Name	Initial value	R/W	Description
3	DTON	0	R/W	Direct Transfer on Flag Along with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2, selects the mode to be entered after execution of the SLEEP instruction.
2	MSON	0	R/W	Medium Speed on Flag After standby, watch, or sleep mode is cleared, this bit selects active (high-speed) or active (medium-speed) mode.

- Clock Halt Register 1 (CKSTPR1) Address: H'FFFA

Bit	Bit Name	Initial value	R/W	Description
7	S4CKSTP	1	R/W*1	SCI4 Module Standby SCI4 enters standby mode when this bit is cleared to 0. 0: SCI4 is placed in module standby mode 1: SCI4 is taken out of module standby mode.
6	S31CKSTP	0	R/W	SCI3_1 Module Standby*2 SCI3_1 enters standby mode when this bit is cleared to 0. 0: SCI3_1 is placed in module standby mode. 1: SCI3_1 is taken out of module standby mode.
5	S32CKSTP	0	R/W	SCI3_2 Module Standby*2 SCI3_2 enters standby mode when this bit is cleared to 0. 0: SCI3_2 is placed in module standby mode 1: SCI3_2 is taken out of module standby mode.
4	ADCKSTP	0	R/W	A/D Converter Module Standby The A/D converter enters standby mode when this bit is cleared to 0. 0: The A/D converter is placed in module standby mode. 1: The A/D converter is taken out of module standby mode.
3	DADCKSTP	1	R/W	ΔΣA/D Converter Module Standby The ΔΣA/D converter enters standby mode when this bit is cleared to 0. 0: The ΔΣA/D converter is placed in module standby mode. 1: The ΔΣA/D converter is taken out of module standby mode.
2	TFCKSTP	0	R/W	Timer F Module Standby Timer F enters standby mode when this bit is cleared to 0. 0: Timer F is placed in module standby mode. 1: Timer F is taken out of module standby mode.
1	FROMCKSTP	1	R/W	Flash Memory Module Standby The flash memory enters standby mode when this bit is cleared to 0. 0: The flash memory is placed in module standby mode. 1: The flash memory is taken out of module standby mode.
0	RTCCKTP	0	R/W	RTC Module Standby The RTC enters standby mode when this bit is cleared to 0. 0: The RTC is placed in module standby mode. 1: The RTC is taken out of module standby mode.

Note: *1. In the mask-programmed ROM version, this is a reserved bit which is not readable or writable.
*2. When SCI3 is put on module standby, all registers of SCI3 enter the reset state.

- Clock Halt Register 2 (CKSTPR2) Address: H'FFFB

Bit	Bit Name	Initial value	R/W	Description
7	ADBCKSTP	1	R/W	Address Break Module Standby The address break module enters standby mode when this bit is cleared to 0. 0: The address break module is placed in module standby mode. 1: The address break module is taken out of module standby mode.
6	TPUCKSTP	0	R/W	TPU Module Standby The TPU enters standby mode when this bit is cleared to 0. 0: The TPU is placed in module standby mode 1: The TPU is taken out of module standby mode.
5	IICCKSTP	0	R/W	IIC2 Module Standby The IIC2 module enters standby mode when this bit is cleared to 0. 0: The IIC2 module is placed in module standby mode. 1: The IIC2 module is taken out of module standby mode.
4	PW2CKSTP	0	R/W	PWM2 Module Standby The PWM2 module enters standby mode when this bit is cleared to 0. 0: The PWM2 module is placed in module standby mode. 1: The PWM2 module is taken out of module standby mode.
3	AECCKSTP	0	R/W	Asynchronous Event Counter Module Standby The asynchronous event counter enters standby mode when this bit is cleared to 0. 0: The asynchronous event counter is placed in module standby mode. 1: The asynchronous event counter is taken out of module standby mode.
2	WDCKSTP	0	R/W*	Watchdog Timer Module Standby The watchdog timer enters standby mode when this bit is cleared to 0. 0: The watchdog timer is placed in module standby mode 1: The watchdog timer counter is taken out of module standby mode.
1	PW1CKSTP	0	R/W	PWM1 Module Standby The PWM1 module enters standby mode when this bit is cleared to 0. 0: The PWM1 module is placed in module standby mode. 1: The PWM1 module is taken out of module standby mode.

Bit	Bit Name	Initial value	R/W	Description
0	LDCKSTP	0	R/W	LCD Module Standby The LCD controller/driver enters standby mode when this bit is cleared to 0. 0: The LCD controller/driver is placed in module standby mode. 1: The LCD controller/driver is taken out of module standby mode.

Note: * This bit is valid when the WDON bit in TCSRWD1 is 0. If this bit is cleared to 0 while the WDON bit is set to 1 (i.e. while the watchdog timer is operating), the bit is cleared but the watchdog timer does not enter module standby mode; instead, it continues to operate. When the watchdog timer stops operating and the WDON bit is cleared to 0 by software, this bit is fully effective and the watchdog timer enters module standby mode.

5.2 Description of modules

Table 2 gives descriptions of the modules used in this sample task.

Table 2 Description of Modules

Module Name	Function
main ( )	Main Routine Initial settings of the ΔΣA/D converter. Waits for the end of the first round of ΔΣA/D conversion, enables the ΔΣA/D conversion end interrupt request, starts the second and later rounds of ΔΣA/D conversion, and places the chip in the sleep (high-speed) mode. On completion of the 65th round of ΔΣA/D conversion, obtains the average of the results, and saves the averaged result in the internal RAM.
int_dsadc ( )	ΔΣA/D converter interrupt processing routine Clears the ΔΣA/D converter interrupt request flag, obtains a running total of the results of A/D conversion in the second and later rounds, and increments the counter that controls the number of rounds of conversion by the ΔΣA/D converter.

5.3 Description of RAM usage

Table 3 shows the RAM usage in this sample task.

Table 3 Description of RAM usage

Label Name	Function	Data Size	Address	Module Name
ad_result	Location for the average value of the results of measurement, i.e. the total over the 64 rounds of conversion shifted 6 bits right	unsigned short (2 bytes)	H'F780	main ( )
ad_work	Working area where the running total of results from the 64 rounds of ΔΣA/D conversion is kept.	unsigned long (4 bytes)	H'F782	main ( ) int_dsadc ( )
ad_cnt	Counter that controls the number of rounds of conversion by the ΔΣA/D converter	unsigned char (1 byte)	H'F786	main ( )

5.4 Link address settings

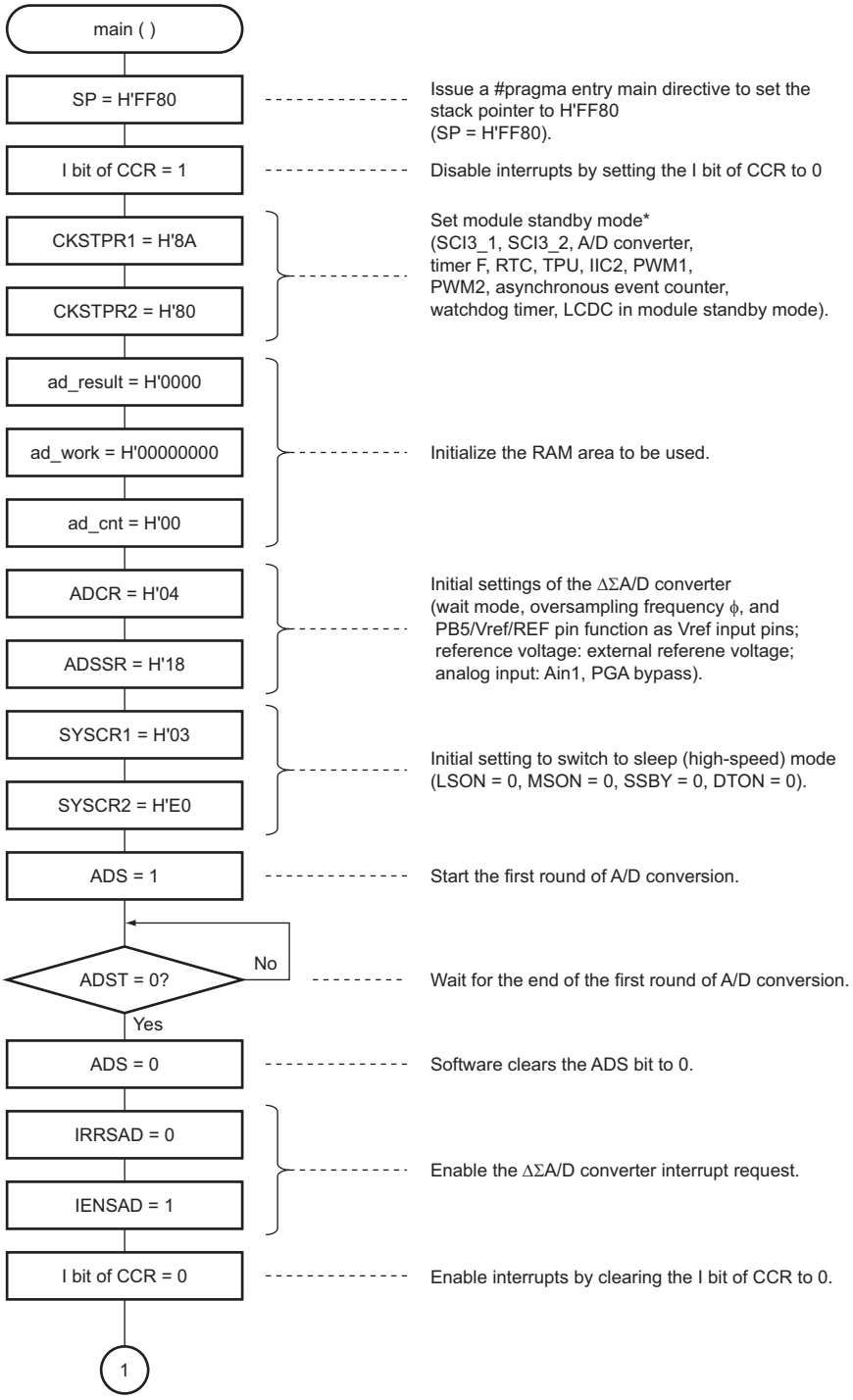
Table 4 shows the link addresses used in this sample task.

Table 4 Link Address Settings

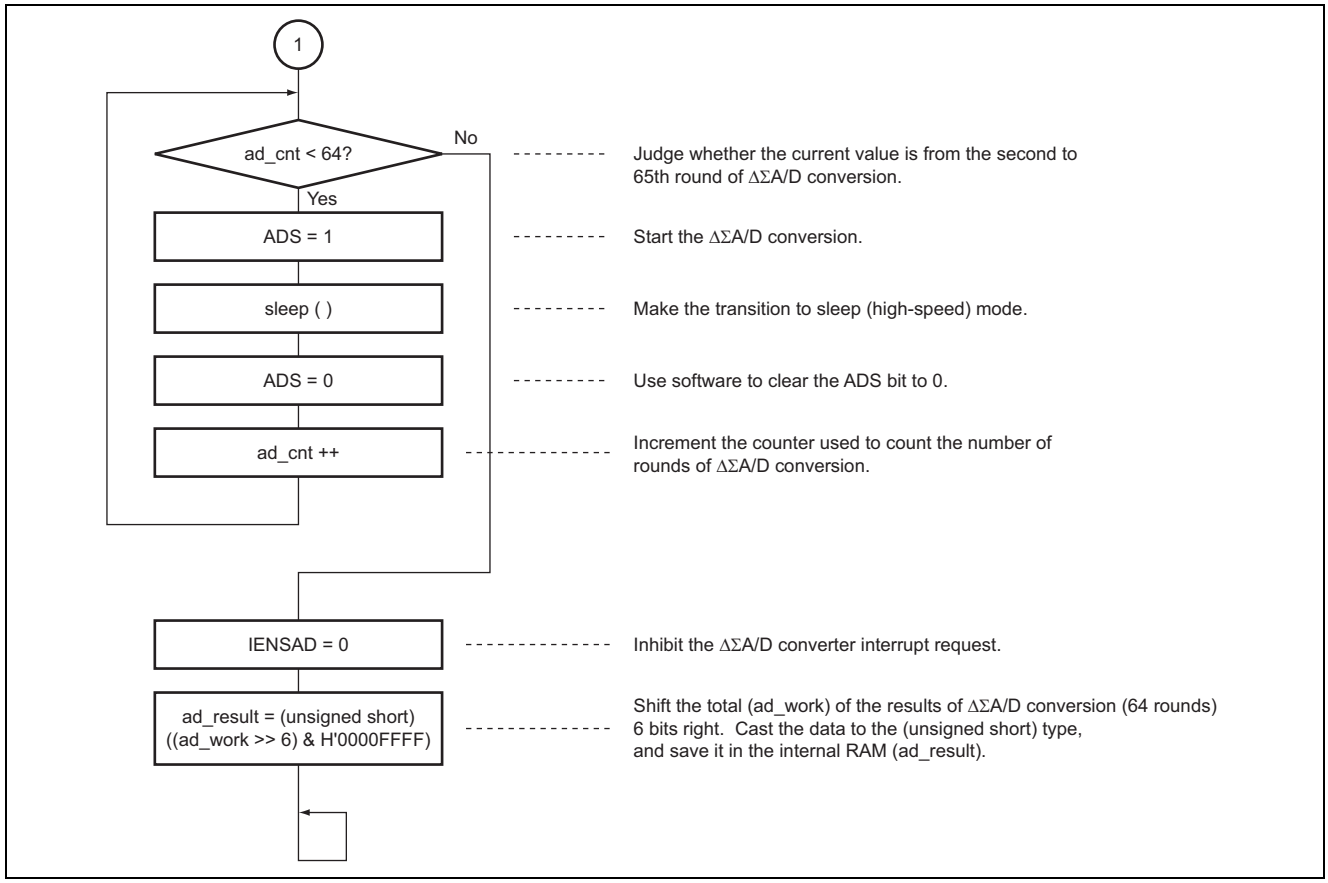
Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

6. Flowcharts

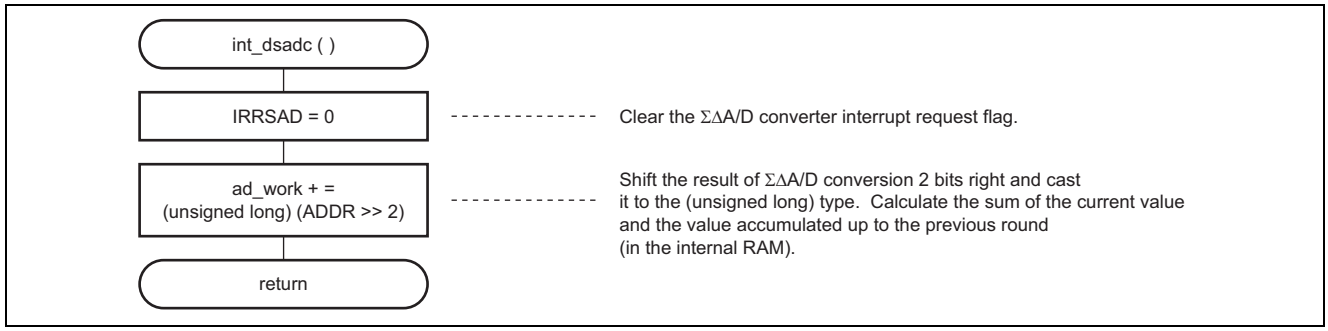
6.1 Main routine



Note: * In this sample task, all internal peripheral modules other than SCI4, the flash memory, address break, and ΔΣA/D converter are placed in module standby mode. Write 1 rather than 0 to any bits of the clock stop register that correspond to other peripheral modules you might require.



6.2 ΔΣA/D converter interrupt processing routine



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