Application Note

Universal Class D (UcD) Power Amplifier Using HVPAK

AN-CM-322

Abstract

This application note describes how to design and build a stereo full-bridge Universal Class D (UcD) audio power amplifier using the SLG47105 IC.

The application note comes complete with a design file that can be found in the Reference section.

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1 Terms and Definitions

ACMP	Analog Comparator
GPO	General Purpose Output
HV	High Voltage
IC	Integrated Circuit
I/O	Input / Output
LDO	Low Drop-out
MOSFET	Metal–oxide–semiconductor Field-effect Transistor
PWM	Pulse Width Modulation
THD + N	Total Harmonic Distortion Plus Noise
UcD	Universal Class D

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[3] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[4] AN-CM-322 Universal Class D (UcD) Power Amplifier Using HVPAK.hvp, Design file
[5] SLG47105 Datasheet
[6] AN-CM-321 Class D Power Amplifier Using HV PAK
[7] Simple Self-Oscillating Class D Amplifier with Full Output Filter Control by Bruno Putzeys, May 2010
[8] A Universal Grammar of Class D Amplification by Bruno Putzeys, Hypex Electronics, The Netherlands, May 2007
[9] UM10155, Discrete Class D High Power Audio Amplifier, Rev. 02 — 5 September 2006
[10] WO 2003/090343 A3, Rev. 02 — 5 September. International application published under the patent cooperation treaty (PCT)

2 Introduction

This application note describes how to design and build a stereo full-bridge Universal Class D (UcD) audio power amplifier using the SLG47105 IC.

A class D amplifier operates by deriving a two-state signal from a continuous control signal and amplifying it using power switches. At the core of every class D amplifier is at least one comparator and one switching power stage. In all but the low-cost power amplifiers, a passive LC filter is added.

Here's a summary of the benefits and disadvantages of the Class-D amplifier versus the traditional Class-AB amplifier.

- Class AB

Benefit: Lowest distortion—total harmonic distortion plus noise (THD + N) is less than 0.1% for high fidelity.

Disadvantages: Inefficient—maximum possible efficiency is about 60%. High power consumption and significant heat generation. It's also larger in size.

- Class D

Benefits: High efficiency—greater than 90%. Less power consumption and lower heat generation. Smaller size. Very high-power potential (400 to 500 W) in a small package.

Disadvantages: High-frequency noise generation.

2.1 Basic Class D Topology

The most basic topology utilizes pulse-width modulation (PWM) with a triangle-wave (or sawtooth) oscillator. Figure 1 shows a simplified block diagram of a PWM-based, half-bridge Class D amplifier. It consists of a pulse-width modulator, two output MOSFETs, and an external lowpass filter (L_F and C_F) to recover the amplified audio signal. As shown in the figure, both MOSFETs operate as current-steering switches by alternately connecting the output node to V_{DD} and ground, thus the resulting output of a Class D amplifier is a high-frequency square wave. The output square wave is pulse-width modulated by the input audio signal. PWM is accomplished by comparing the input audio signal to an internally generated triangle-wave (or sawtooth) oscillator. The resulting duty cycle of the square wave is proportional to the level of the input signal. When no input signal is present, the duty cycle of the output waveform is equal to 50%. Figure 2 illustrates the resulting PWM output waveform due to the varying input-signal level.

This basic topology has a few downsides. Very low power supply rejection ratio. High THD. The quality of the output signal is highly dependent on the linearity and stability of the triangle wave, which significantly complicates the circuit.

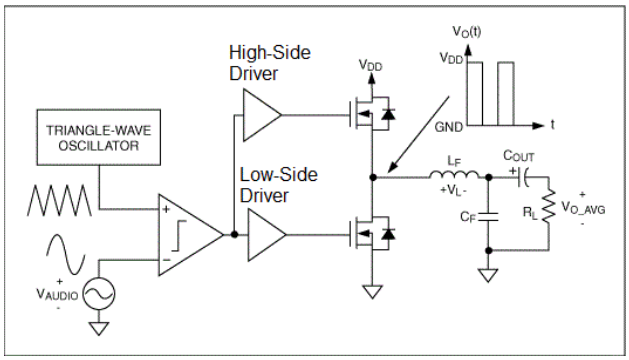


Figure 1: Half-Bridge Class D Amplifier, Basic Topology

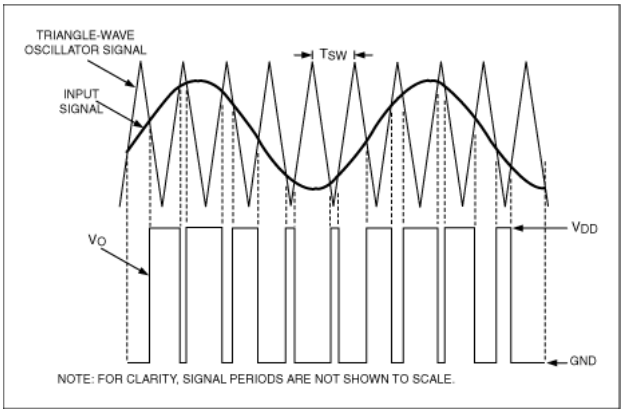


Figure 2: The Output-Signal Pulse Widths Vary Proportionally With the Input-Signal

One of the most commonly used topologies of class D audio amplifiers is known as self-oscillation. Self-oscillating class D audio amplifiers are characterized by having an open-loop bandwidth equal to the switching frequency as opposed to traditional PWM amplifiers, where the loop bandwidth typically will be limited to one-tenth of the switching frequency. This increased loop bandwidth provides valuable loop gain at low frequency, which is beneficial with respect to the reduction of Total Harmonic Distortion (THD).

There are several ways of designing a self-oscillating class D power amp, but in this document, only **Phase-shift control using the reconstruction filter** topology (UcD) will be considered, as this topology provides the best audio performance and ensures the highest sound quality.

2.2 Phase-shift Control Using the Reconstruction Filter Topology

The phase shift of the reconstruction filter is usually seen as a burden, rarely as an advantage. Second-order filters turn out to be very interesting for building phaseshift controlled amplifiers. One is reminded that the switching frequency is set well beyond the corner frequency of the filter. At any sufficiently high frequency, a second-order low pass filter produces a phase shift close to 180 degrees. Varying load conditions only affect this to the order of a few degrees.

Closing a negative feedback loop around such a filter is not enough though. The oscillation occurs at a phase shift of exactly 180 degrees (the other 180 degrees are furnished by the polarity inversion), which only happens at infinity. An additional network is in order that holds the phase shift well away from 180 degrees below the desired switching frequency, and another one that pushes it well beyond it above this frequency. Any practical circuit will already have the latter for free. The combined propagation delays of the comparator and the power stage constitute a phase shift directly proportional to frequency. The former can be as simple as a phase lead network in the feedback path. See Figure 3.

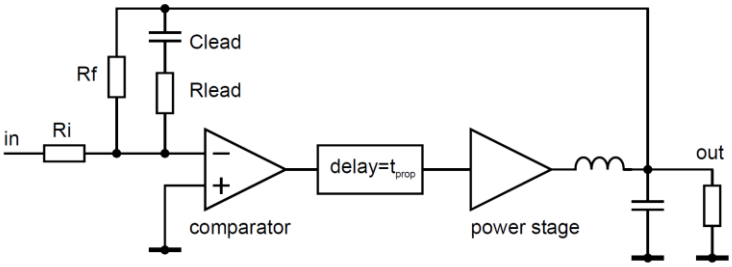
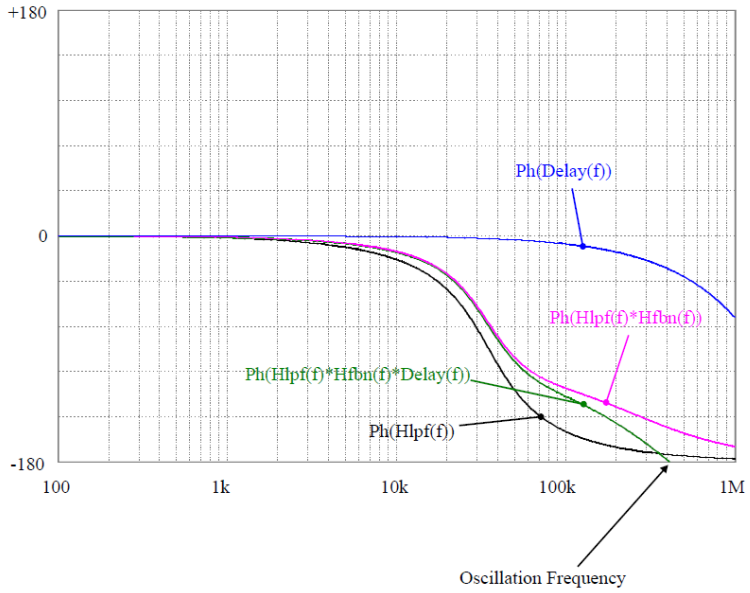


Figure 3: Phase-Shift Control Using the Reconstruction Filter Topology

Since at any useful oscillation frequency the phase shift of the output filter is 180 degrees, oscillation will occur at the frequency where the propagation delay and the phase lead cancel out. Care should be taken to ensure that under any realistic load condition there is not a second point with 180 degrees phase shift, because this point will be most certainly be the physical resonance frequency filter. Failing this usually leads to the undoing of the amplifier the first time it is overdriven with no load attached. See Figure 4.



Where H_{lpf} is the transfer function of the LC filter and H_{fbn} that of the feedback network Delay(s) is a linear phase shift function representing the propagation delay.

Figure 4: Phase-Shift

The phase-shift control using the reconstruction filter topology has a big advantage over other topologies. The negative feedback loop is encompassing the reconstruction filter, this allows to completely compensate for any non-linearity. The amplifier designed using this topology is capable of producing extremely low THD+N and can compete with class AB while having all advantages of class D.

3 Design Operation

3.1 Schematic Design

Designing a class D power amp using the SLG47105 IC has its advantages. The chip has two full-bridge high-speed power outputs which allow building a stereo full-bridge UcD audio power amplifier using a minimum of internal and external components. See Figure 5 for a complete schematic diagram in the GreenPAK Designer project. The amplifier operates exactly as described in Section 2.2. The only difference is a full-bridge output. Also, the output (reconstruction) filter is designed to use a single ferrite core (or iron powder ring) for both L1 and L2 (L3 and L4). It should be noted that the windings of the coils should be connected in accordance with the schematics. The beginning of each winding is marked with a dot near the coil symbol, see Figure 5.

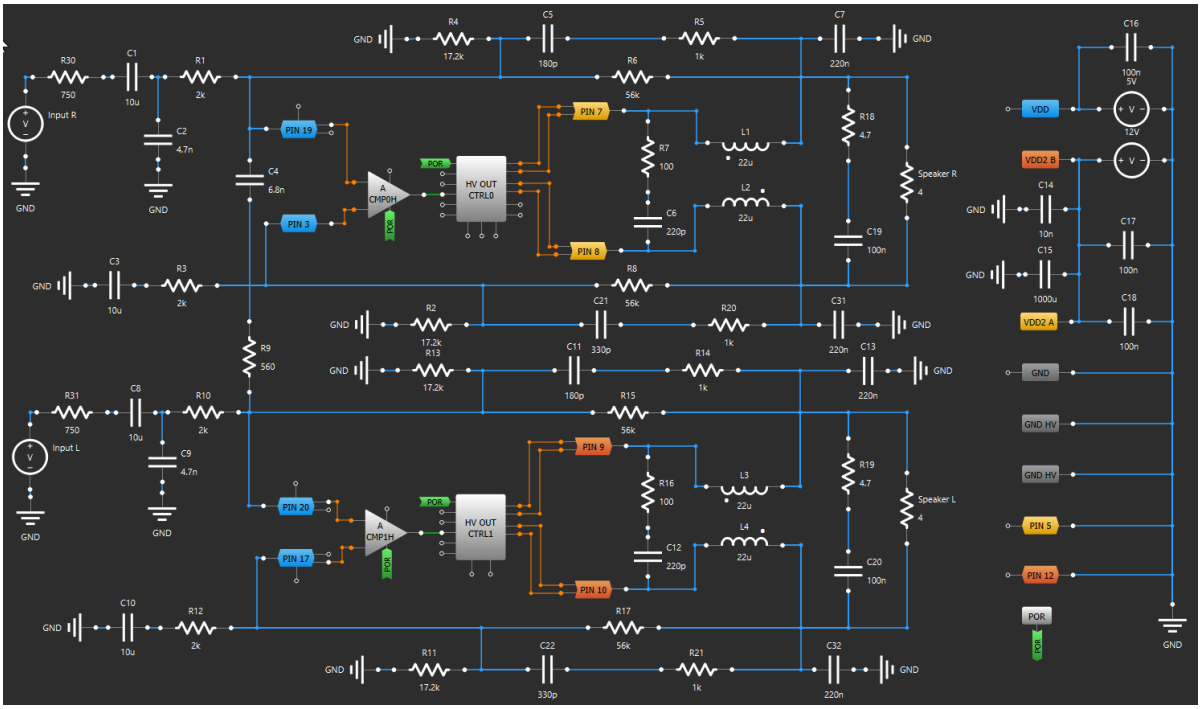


Figure 5: Stereo Full-bridge UcD Audio Power Amplifier Project

It is also possible to use a separate LC filter for each output, four in total in this design. But this will only increase the quantity of the external components leading to a larger PCB size and higher overall cost.

Since this design is a stereo amp, it means both channels will oscillate with very close frequencies. That may cause an extra high-frequency interference. To overcome this issue both channels must be synchronized, it is done by C4 and R9. These components must be selected so the phase shift between oscillations is as minimal as possible, down to nanoseconds.

The oscillating frequency doesn't depend much on factors such as parasitic RCL parameters of the PCB and the IC itself. The main components that set up the frequency are the output filter and R5 C5 chain (R15 C11 for another channel). Using the values shown on the schematic diagram the frequency is close to 300kHz.

Both ACMPs within the IC have a first-order low-pass filter builtin on the inverting input. This results in the non-linearity of the bandwidth characteristics. To reduce this effect, one more RC chain was added R20 C21 (R21 C22 for another channel).

The amp is powered by a 12 V power supply for VDD2A and VDD2B, also a 5 V LDO IC is used to power VDD. Since the ACMPs inside the HV PAK are powered from 5 V and the output stages are powered from 12 V, the additional voltage divider is required to prevent damaging ACMPs via the feedback loop. Figure 6 shows a simplified circuit where the additional voltage dividing resistors are marked red. Also marked R2, R4, R11, and R13 in Figure 5.

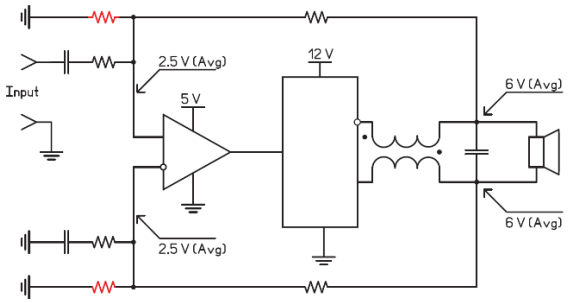


Figure 6: Simplified Circuit of the Amplifier. One Channel

3.2 Typical Operating Characteristics

Note that connecting speakers of less than 8 Ohm is not recommended unless an additional heat dissipation is considered. In this case, it is possible to get up to 15 W of output power per channel.

The amplifier has the following characteristics:

- Power supply voltage – 7.5 V to 12 V
- Current consumption (no input signal) – 35 mA
- Output power per channel (supply – 12V, load – 8 Ohm) – 9 W (max)
- Gain – 42 dB
- Input resistance – 2.7 kOhm
- THD (1 W, 1 kHz) – 0.02%
- THD (9 W, 1 kHz) – 0.5%
- Frequency response – 10 Hz to 17 kHz (-3 dB)

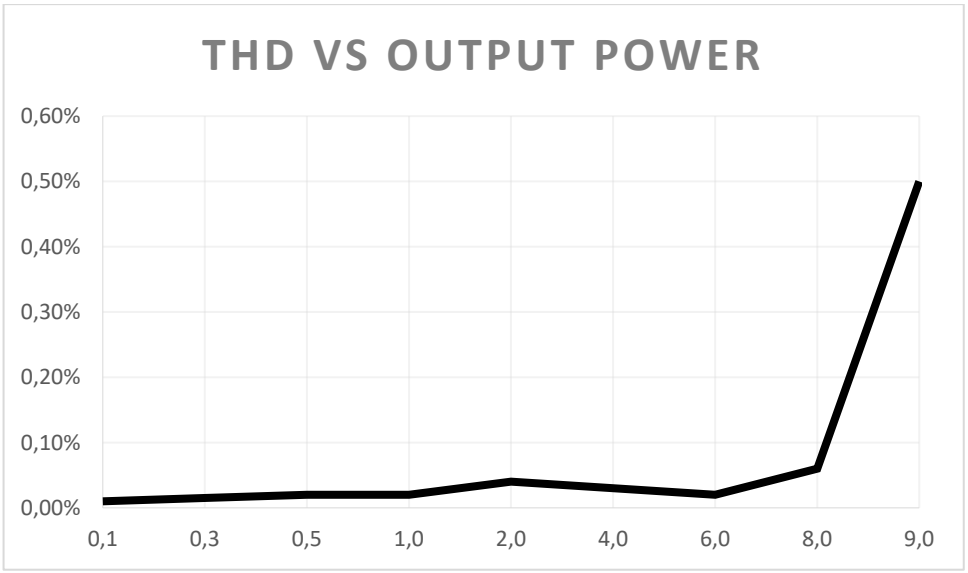


Figure 7: THD vs Output Power, Rl = 8 Ohm, f = 1kHz

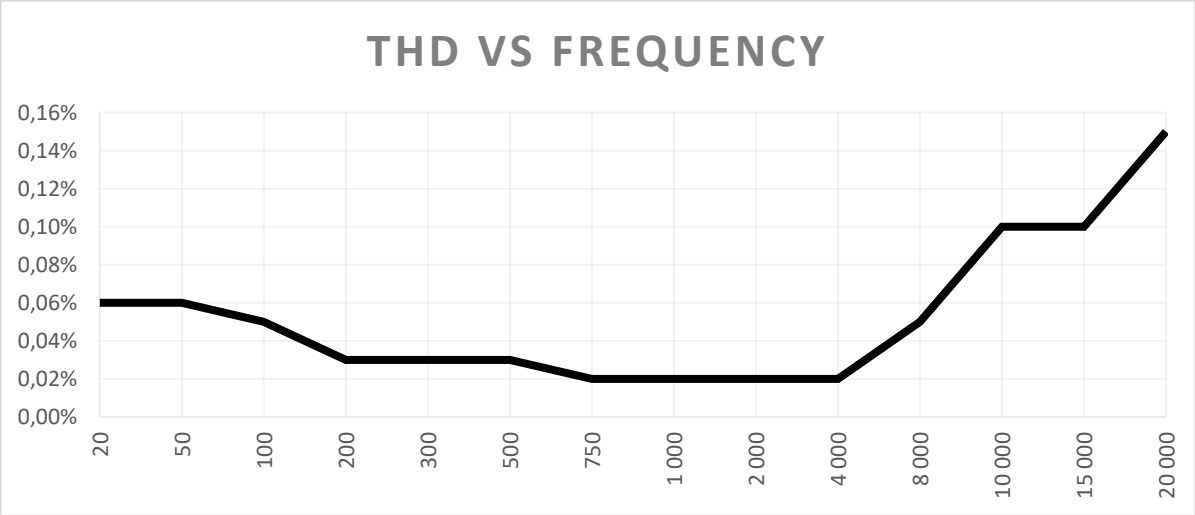


Figure 8: THD vs Frequency, Rl = 8 Ohm, Pout = 1 W

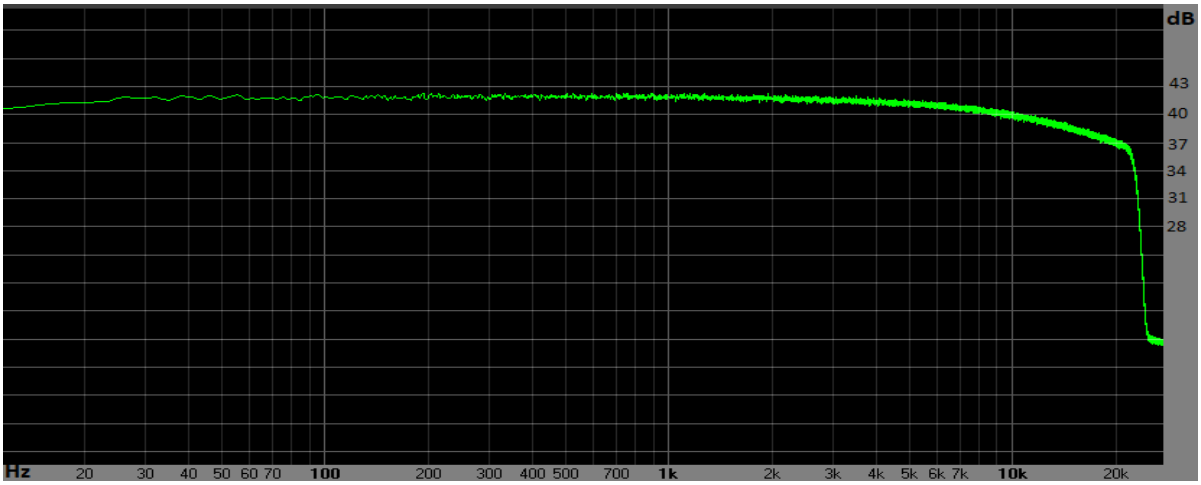


Figure 9: Frequency response, V_{DD} = 12V, Rl = 8

3.3 Macrocell Configuration

Table 1: PIN Settings

Properties	PIN 7, 8, 9, and 10	PIN 3, 17, 19, and 20
I/O selection	Digital output	Analog input/output
Input mode OE=0	None	Analog input/output
Output mode OE=1	HIGH and LOW side	Analog input/output

Resistor	--	Floating
Resistor value	--	Floating

Table 2: ACMP Settings

Properties	ACMP0H	ACMP1H
Hysteresis	Disable	Disable
IN+ gain	Disable	Disable
Connections		
IN+ source	PIN 19 (GPIO5)	PIN 20 (GPIO6)
IN- source	Ext. Vref (PIN 3 (GPI))	Ext. Vref (PIN 17 (GPIO4))

Table 3: HV Output Settings

Properties	HV OUT CTRL0	HV OUT CTRL1
Slew rate	Fast for pre-driver mode	Fast for pre-driver mode
HV OUT mode	Full bridge	Full bridge
Mode control	PH-EN	PH-EN
Thermal shutdown	Enable	None
OCP deglitch time enable	With deglitch time	With deglitch time
Control delay of OCP0 retry	Delay 492 us	Delay 492 us
Control delay of OCP1 retry	Delay 492 us	Delay 492 us
VDD2A UVLO	Desable	Desable

3.4 PCB Layout Consideration

PCB should have enough ground plane to dissipate heat. SLG47105 has two additional pads which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from the chip to other layers of the PCB. When using loading less than 8 Ohm please attach an additional radiator to dissipate heat generated by the chip.

The power capacitors should be placed as close as possible to the chip for reducing parasitic parameters. Also, both the input signal ground and the power ground should be separated and connected together on the large capacitor, C15 in this project. See test PCB designed for this application in Figure 10 and Figure 11. The size of the board is 33 x 34 mm.

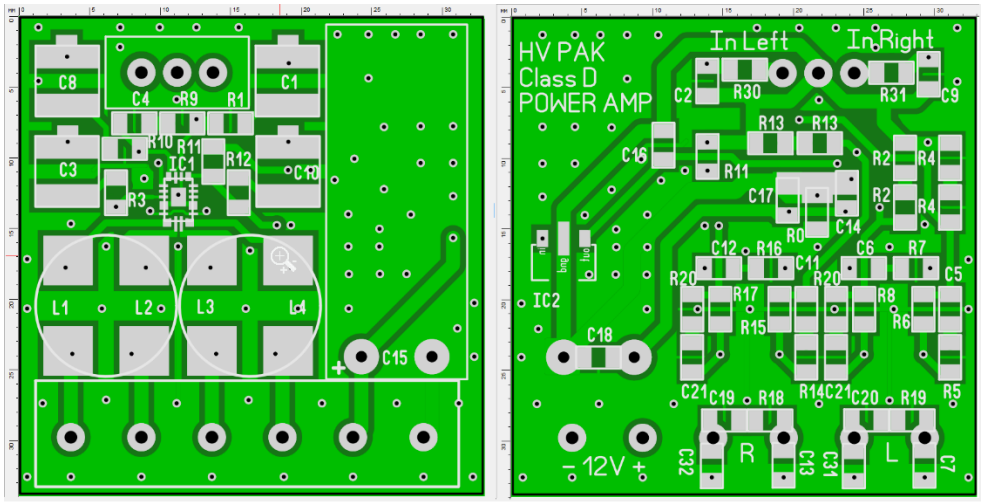


Figure 10: Test PCB Design

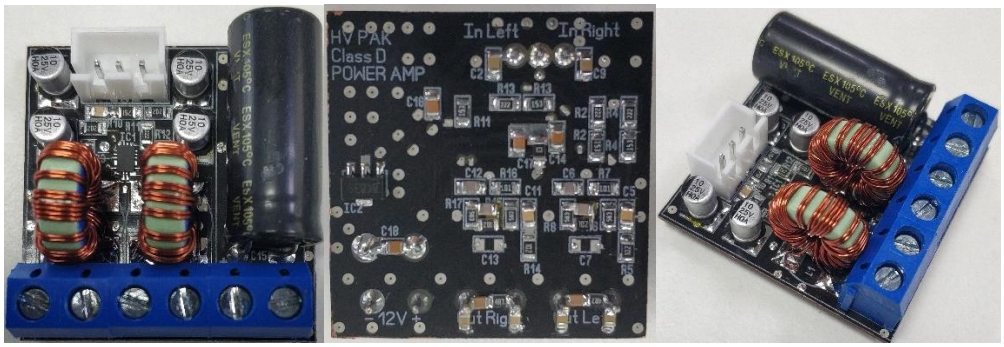


Figure 11: Test PCB Photo

4 Conclusions

As can be seen, designing and building a stereo full-bridge Universal Class D (UcD) audio power amplifier using the HV PAK is very easy. The design shown in this document is the simplest version of the device that can be built based on the SLG47105. There are plenty of unused macrocells that can be used to design additional functions such as Mute, Enable, Stand By, Overcurrent, and Overtemperature protection with indication, etc.

Revision History

Revision	Date	Description
1.0		Initial Version
2.0	12.22.2021	Updated section **3 Design Operation**

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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