Using Renesas SLG59H1405V in PowerMUX applications
SLG59H1405V

This application note describes how to use Renesas SLG59H1405V in PowerMUX applications. Corresponding oscilloscope captures of operational behavior are included.

Contents

1. References

For related documents please visit:

Load Switches | Renesas

[1] SLG59H1405V Datasheet, Renesas Electronics

2. Terms and Definitions

OVP	Over Voltage Protections
UVLO	Under Voltage Lockout
OCP	Over Current Protection
SCP	Short Circuit Protections
OTP	Over-temperature Protection
ACL	Active Current Limit
FET	Field-Effect Transistor
IC	Integrated Circuit
PowerMux	Power multiplexer

3. Introduction

Many applications require two or more power sources and there can be issues when switching between them. For example, almost all portable electronic devices have integrated rechargeable batterie and USB port to charge it. As a result, a solution for seamlessly transitioning between the internal battery and external power sources is required. Connecting multiple power supplies to a single input without any protection can take to power failures, short circuits, and loss of power. In such cases, PowerMUX devices are commonly used as a reliable solution. This document shows the application solution of manual switching between two power sources using the Renesas SLG59H1405V device.

4. Power MUX General Concept

Power multiplexors or PowerMux are devices that provide a seamless transition between two or more power inputs. They are typically used in applications like computers, digital cameras, modems, cellphones, etc. It may also be used in battery management systems and peripheral power interface systems.

In general, the PowerMux device switches between 2 input power supplies to 1 common output supply rail and thus provides a continuous supply for the overall device. A simplified block diagram of PowerMUX is illustrated in Figure 1.

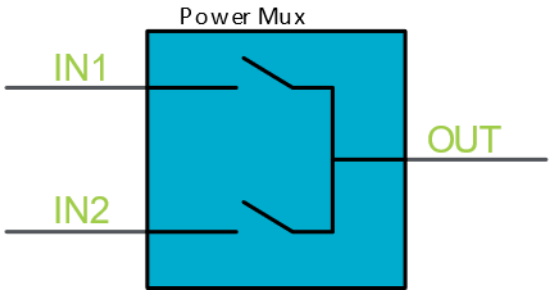

Figure 1: Power Mux simplified block diagram

From a technical standpoint, PowerMUX is typically implemented by controlling MOSFETs RDS_{ON} resistance because MOSFETs have high off isolation, which is important to prevent back-feeding power between two inputs.

From a controlling standpoint, the output power rail can be chosen manually.

A manual PowerMUX is one in which each path is individually controlled by an external signal (logic or microcontroller). An example of Manual PowerMUX with two enable inputs is shown in Figure 2. Such a method is generally used when there is a microcontroller that can decide under what conditions to enable each input. Renesas SLG59H1405V device can be easily used in PowerMux applications and its detailed operation is described below.

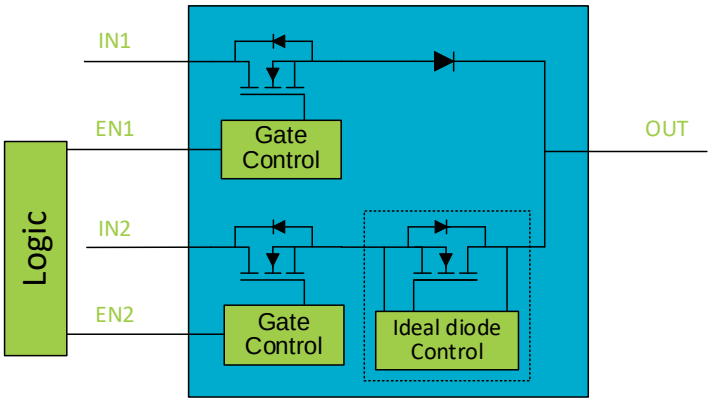

Figure 2: Manual Power Mux

4.1 SLG59H1405 Resume

The SLG59H1405V comes with one 5 V, 3 A and one 12 V, 1.25 A rated load switch with common output. The part allows manual selection and seamless transition between available inputs as well as to provide different kinds of protection features. The part is designed for typical 5V/12V manual switchover Power MUX applications, that are well suited for many systems, that have multiple power sources. The SLG59H1405V pin configurations is shown in Figure 3.

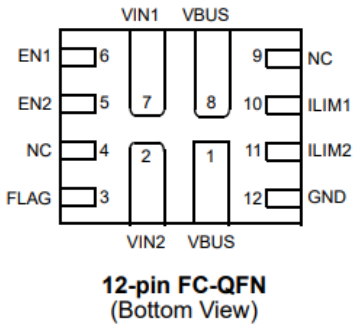

Figure 3: Pin Configuration for SLG59H1405V

The following list provides more details on the functions of each pin:

- **GND** pin: Is a Ground connection. Connect this pin to the system's analog or power ground plane.
- **VIN1** pins: Input terminal of 5.5 V rated Channel 1.
- **VIN2** pins: Input terminal of 13.2 V rated Channel 2.
- **VBUS** pins: Output terminal of the SLG59H1405V Power MUX.
- **FLAG** pin: An open-drain output, FLAG is asserted LOW when a $V_{IN[1,2]}$ overvoltage, undervoltage, current-limit, or an over-temperature condition is detected. Connect a 100 kΩ external resistor from the FLAG pin to a local system logic supply. Connect to GND if not use.
- **NC** pins: No Connect.

- **EN1** pin: EN1 turns on Channel 1 and is a low logic-level CMOS input with EN1_V_{IL} < 0.5 V and EN1_V_{IH} > 1.5 V. While there is an internal pull-down circuit to GND (~1 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
- **EN2** pin: EN2 turns on Channel 2 and is a low logic-level CMOS input with EN2_V_{IL} < 0.5 V and EN2_V_{IH} > 1.5 V. While there is an internal pull-down circuit to GND (~1 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
- **ILIM1** pin: A 1%-tolerance, metal-film resistor sets the active current limit for Channel 1. A 20 kΩ resistor sets the active current limit to 4.01 A.
- **ILIM2** pin: A 1%-tolerance, metal-film resistor sets the active current limit for Channel 2. A 20 kΩ resistor sets the active current limit to 1.94 A

4.2 Using SLG59H1405V in PowerMUX applications

For using SLG59H1405V in manual power rail selection applications, an external voltage $V_{EN[1,2]}$ > EN[1,2]_V_{IH} should be applied to the EN[1,2] pins. Typically, EN1 and EN2 pins are connected to the MCU or other logic level source.

To turn on one of two Channels both V_{IN1} and V_{IN2} voltages should be within the operating voltage range ($V_{IN[1,2]}$ > $V_{IN[1,2]\_UVLO}$ and $V_{IN[1,2]}$ < $V_{IN[1,2]\_OVP}$), otherwise the part will be latched-off and EN1 and EN2 signals will be ignored. When a logic high ($V_{EN[1,2]}$ > EN[1,2]_V_{IH}) is applied to the EN[1,2] pin, the Channel 1 or Channel 2 will be on output respectively.

Please note that to turn on Channel 2 in SLG59H1405V, EN2 > EN2_V_{IH} can be applied not sooner than 100 ms after EN1 > EN1_V_{IH}, otherwise, the EN2 signal will be ignored and the switchover to Channel 2 will not be possible until EN1 < EN1_V_{IL} and then EN1 > EN1_V_{IH} again. In conclusion, to turn on Channel 2, Channel 1 should always be turned on first.

The FLAG pin can be pulled high with a resistor to provide feedback on the status of the system. FLAG is asserted LOW when a $V_{IN[1,2]}$ overvoltage, undervoltage, current-limit, or over-temperature condition is detected. Connect to GND if not used.

The following application scope-shots below demonstrate the turn-on, turn-off and switchover behavior of the SLG59H1405V device for V_{IN1} = 5 V, V_{IN2} = 12 V. Current limit is set to 4 A for Channel 1 and 1.9 A for Channel 2. A typical connection diagram for these conditions is illustrated in Figure 4.

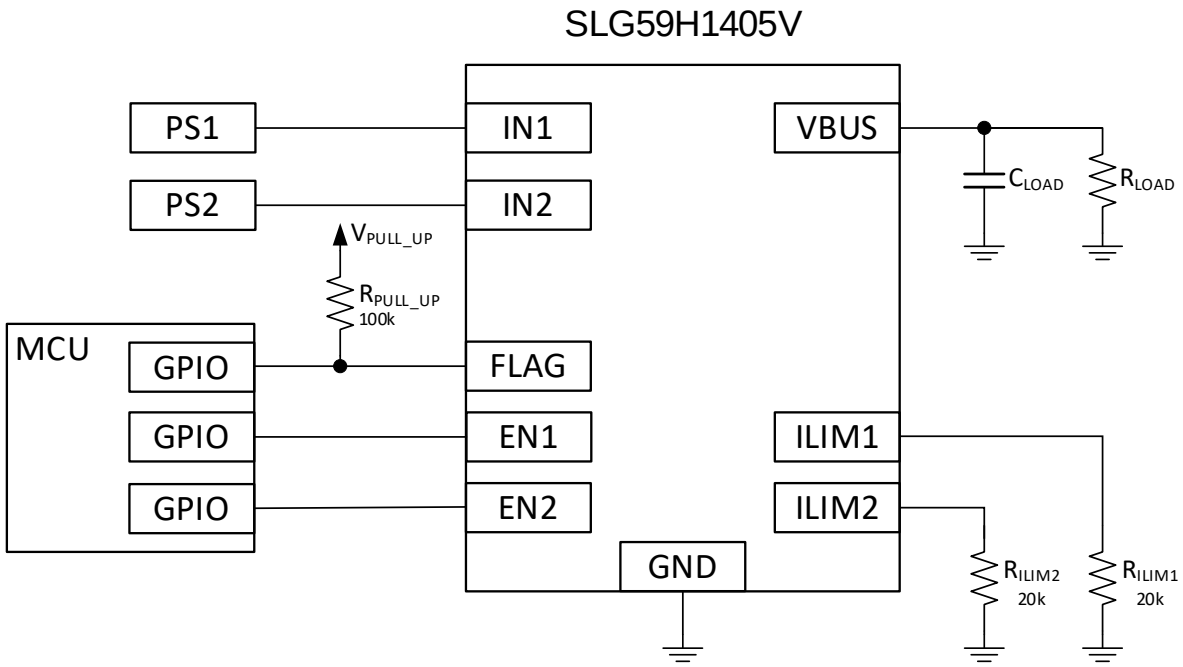

Figure 4: Connection diagram of using SLG59H1405V in PowerMUX applications for V_{IN1} = 5 V, V_{IN2} = 12 V

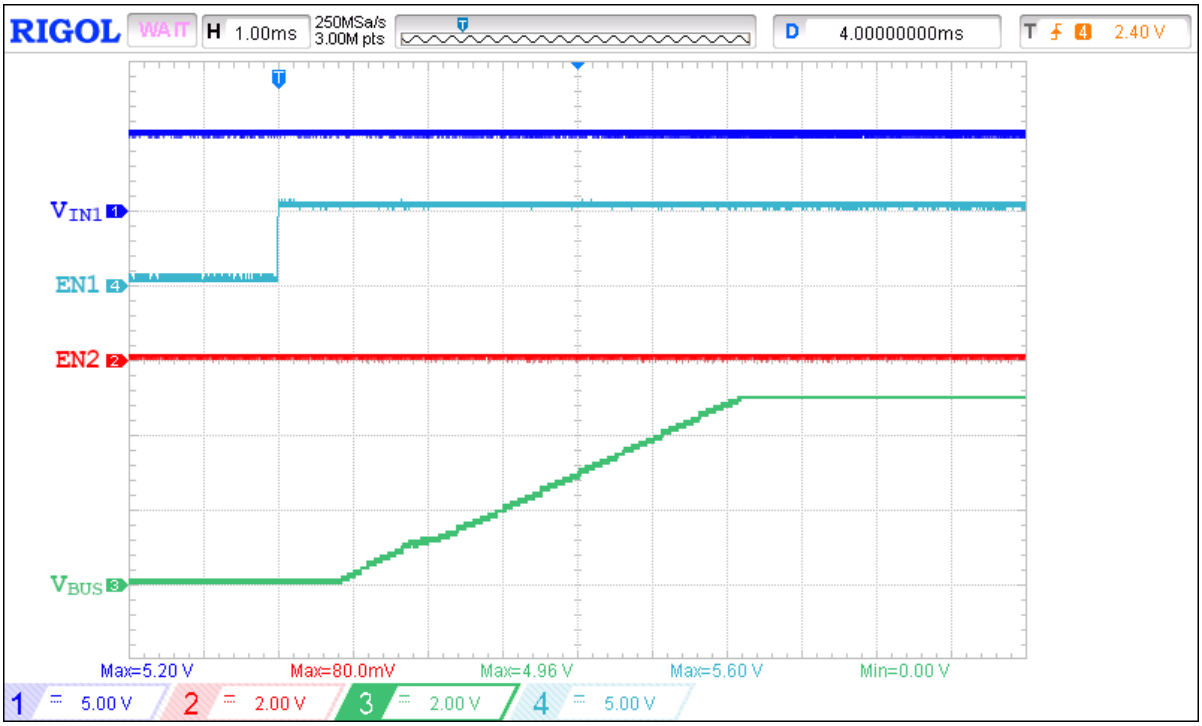

Figure 5: Turn ON operation waveform of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = Low → High, EN2 = Low, R_{LOAD} = 5 Ω, C_{LOAD} = 20 µF

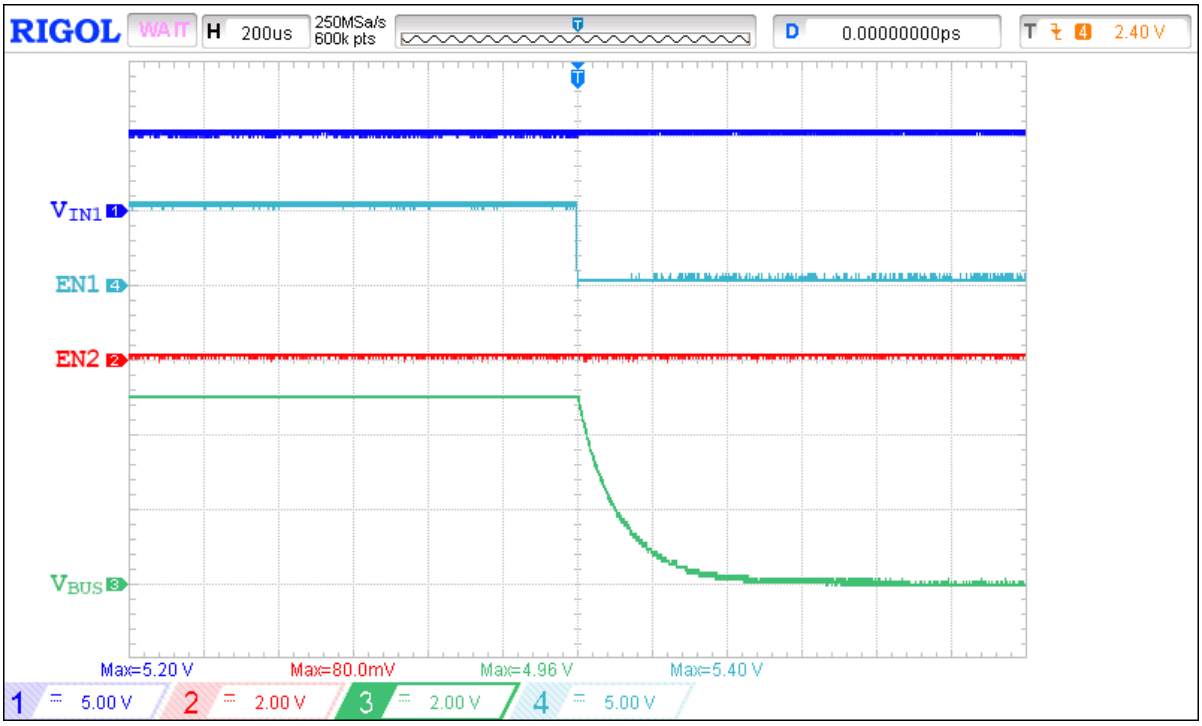

Figure 6: Turn OFF operation waveform of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = High → Low, EN2 = Low, R_{LOAD} = 5 Ω, C_{LOAD} = 20 µF

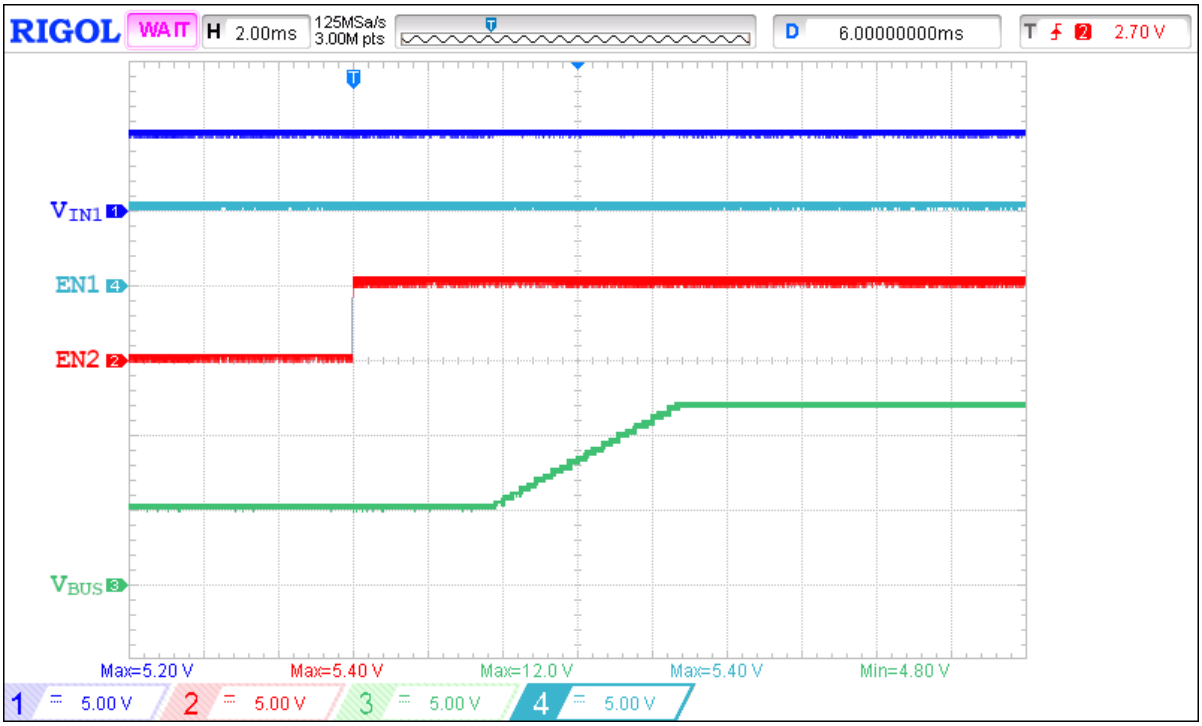

Figure 7: Switchover operation waveform of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = High, EN2 = Low → High, R_{LOAD} = 12 Ω, C_{LOAD} = 20 µF

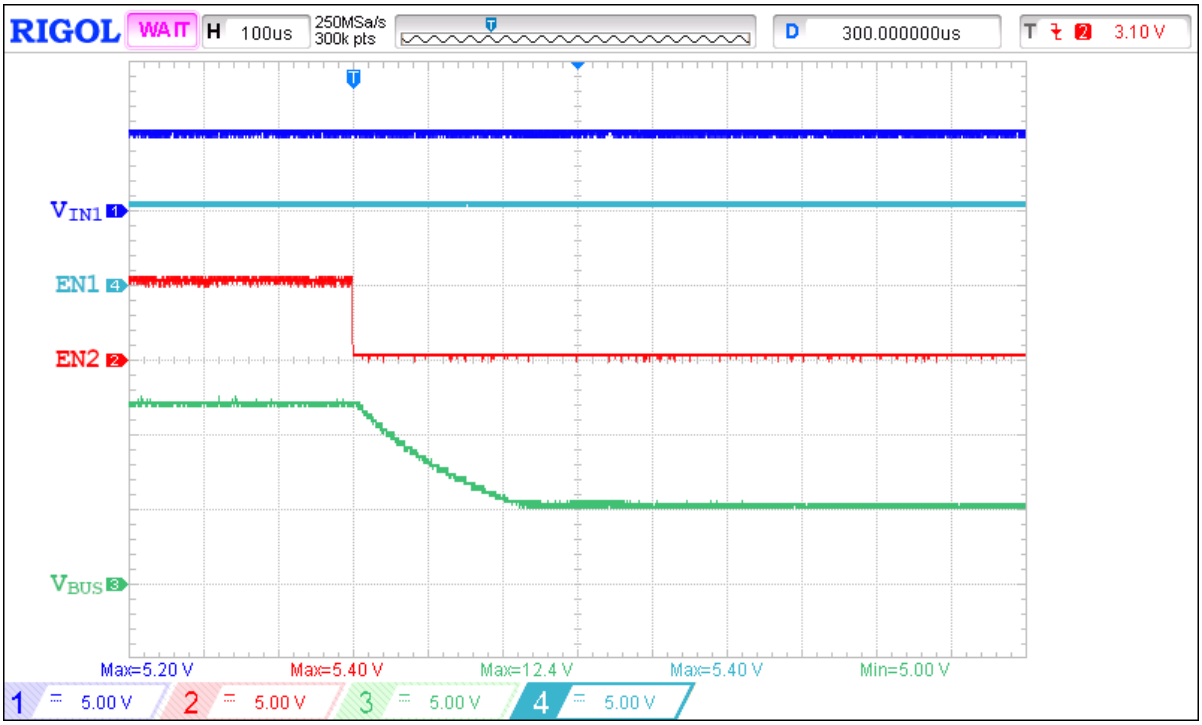

Figure 8: Switchover operation waveform of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = High, EN2 = High → Low, R_{LOAD} = 12 Ω, C_{LOAD} = 20 µF

4.3 SLG59H1405 Protections

The Renesas SLG59H1405 load switch has many protections:

- Over Voltage Protections (OVP)
- Under-Voltage Lockout (UVLO)
- Over Current Protections (OCP)
- Short Circuit Protections (SCP)
- Over-temperature Protection (OTP)

Once one of these protections (except UVLO) has triggered, the SLG59H1405 goes Latch-Off. To release the part from the latch-off condition, both EN1 and EN2 should be set lower than EN[1,2]_V_{IL}.

4.3.1. Over Voltage Protection

The Over Voltage Protection is always monitoring the input voltage regardless of the active channel. Once V_{IN1} > V_{IN1_OVP} or V_{IN2} > V_{IN2_OVP} an SLG59H1405V will latch-off within T_{OVP} response time.

The following application scope-shots below demonstrate the OVP Latch-Off behavior and then proper recovery from Latch-Off of the SLG59H1405V device for V_{IN1} = 5 V step up to 6 V, V_{IN2} = 12 V. Figure 9 and Figure 10 are illustrated when Channel 1 is active, and when Channel 2 is active are shown in Figure 11. A typical connection diagram for these conditions is illustrated in Figure 4.

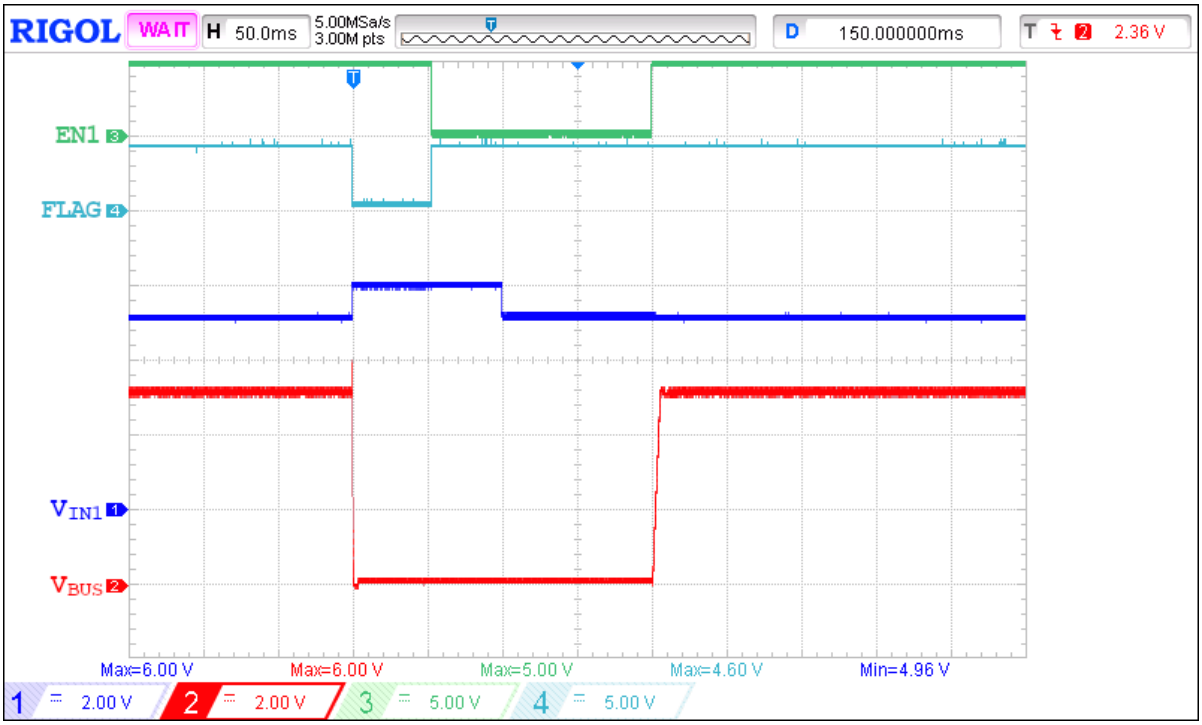

Figure 9: OVP behavior and proper recovery from Latch-Off waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V step up to 6 V, V_{IN2} = 12 V, EN1 = High, EN2 = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF

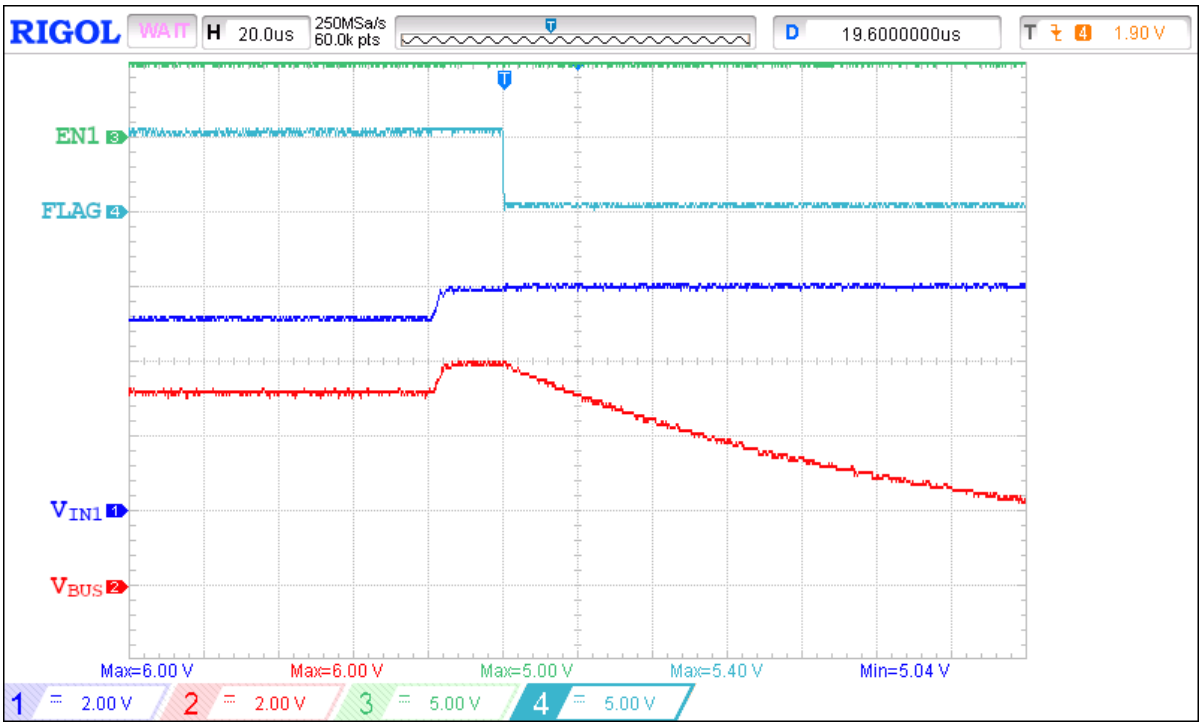

Figure 10: OVP behavior and proper recovery from Latch-Off waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V step up to 6 V, V_{IN2} = 12 V, EN1 = High, EN2 = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF (extended view)

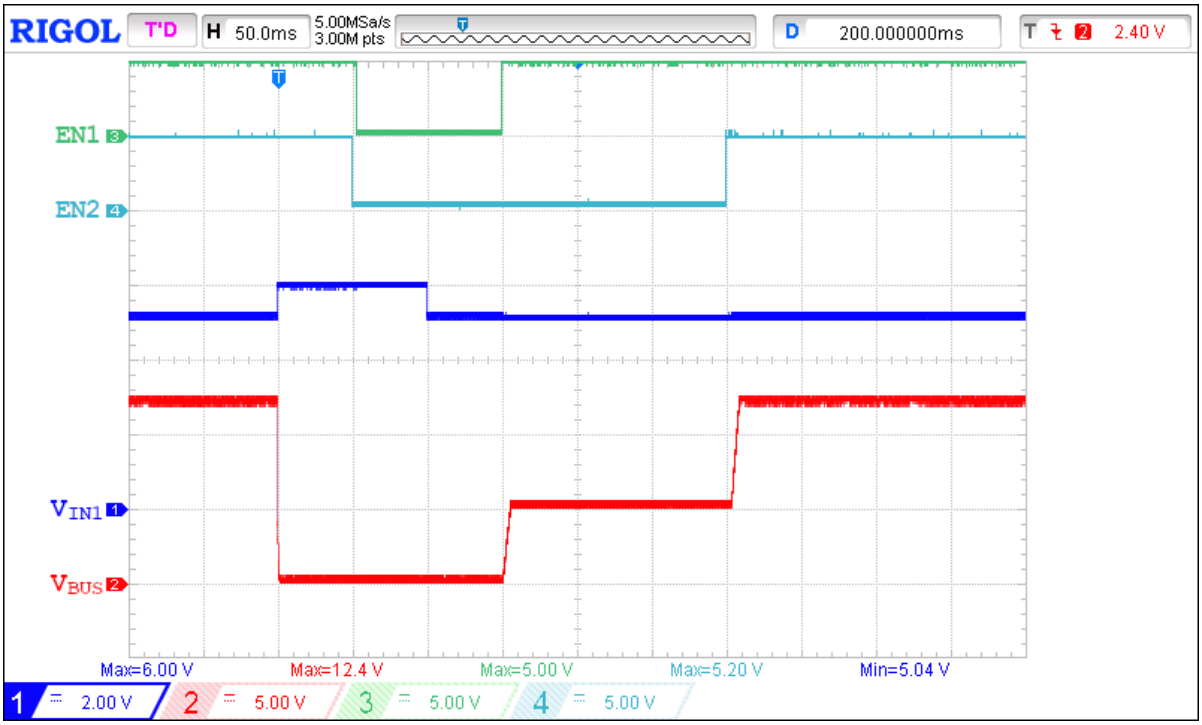

Figure 11: OVP behavior and proper recovery from Latch-Off waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V step up to 6 V, V_{IN2} = 12 V, EN1 = High, EN2 = High, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF

The following application scope-shots below demonstrate the OVP Latch-Off behavior and then proper recovery from Latch-Off of the SLG59H1405V device for V_{IN1} = 5 V, V_{IN2} = 12 V step up to 15 V. Figure 12 demonstrates when Channel 1 is active, and when Channel 2 is active are shown in Figure 13 and Figure 14. A typical connection diagram for these conditions is illustrated in Figure 4.

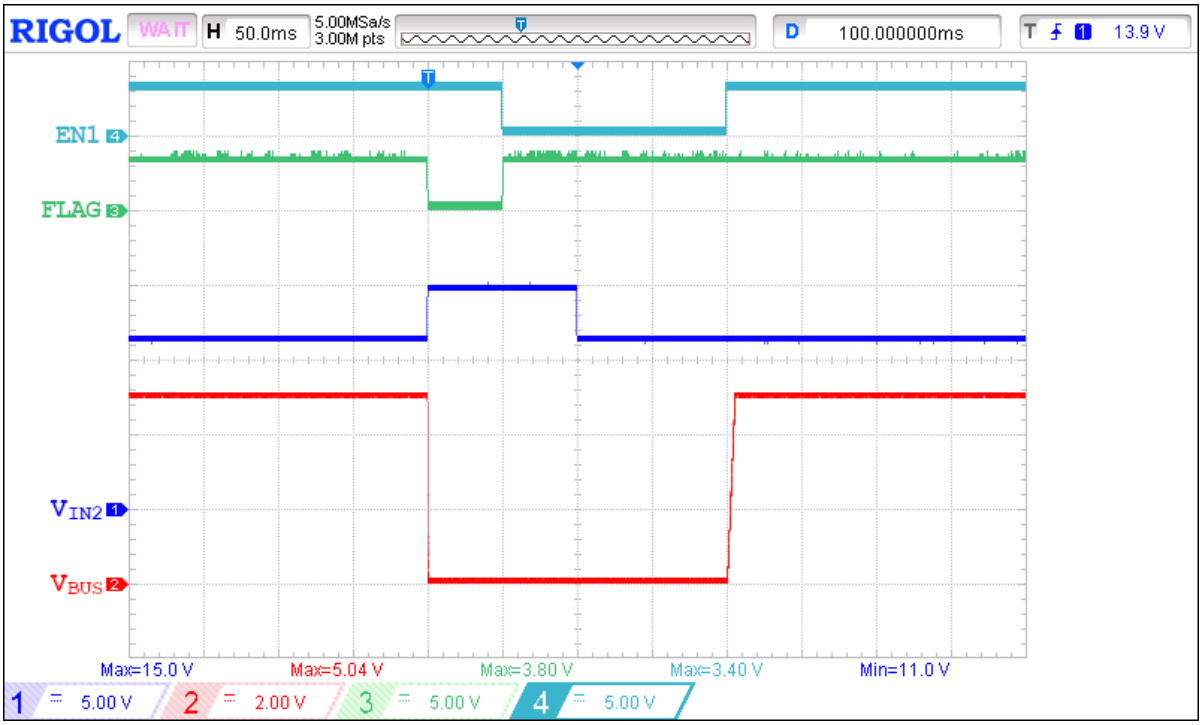

Figure 12: OVP behavior and proper recovery from Latch-Off waveform for Channel 2 of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V step up to 15 V, EN1 = High, EN2 = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF

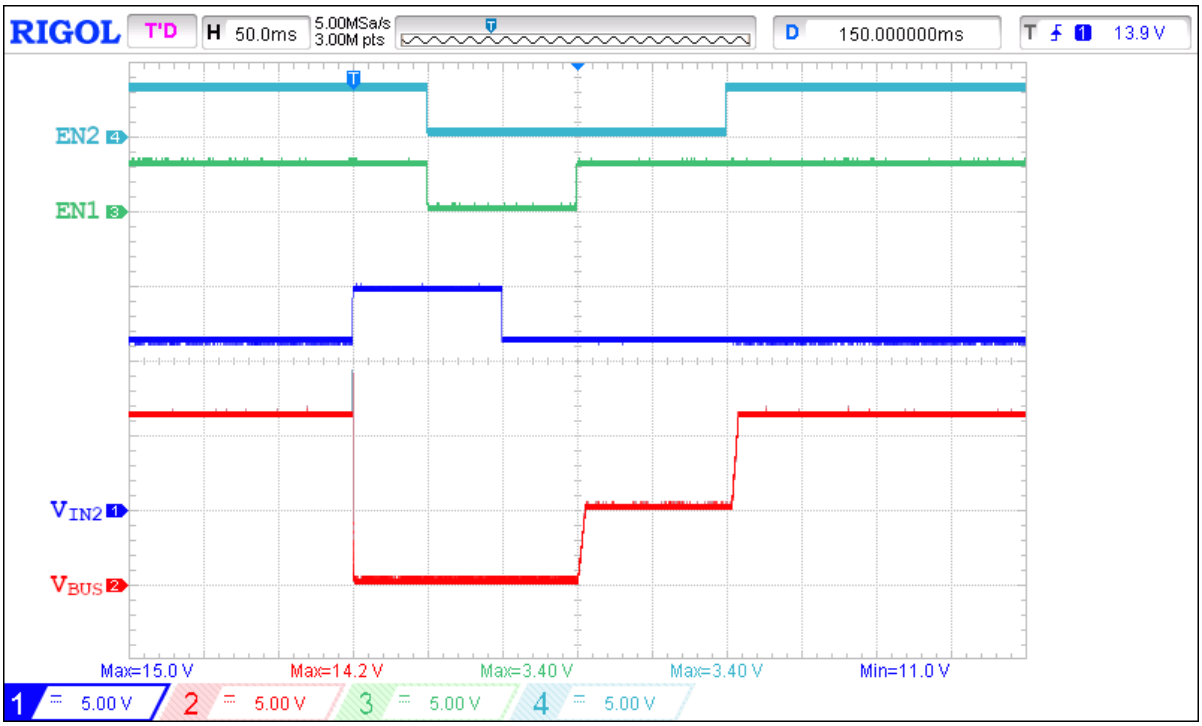

Figure 13: OVP behavior and proper recovery from Latch-Off waveform for Channel 2 of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V step up to 15 V, EN1 = High, EN2 = High, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF

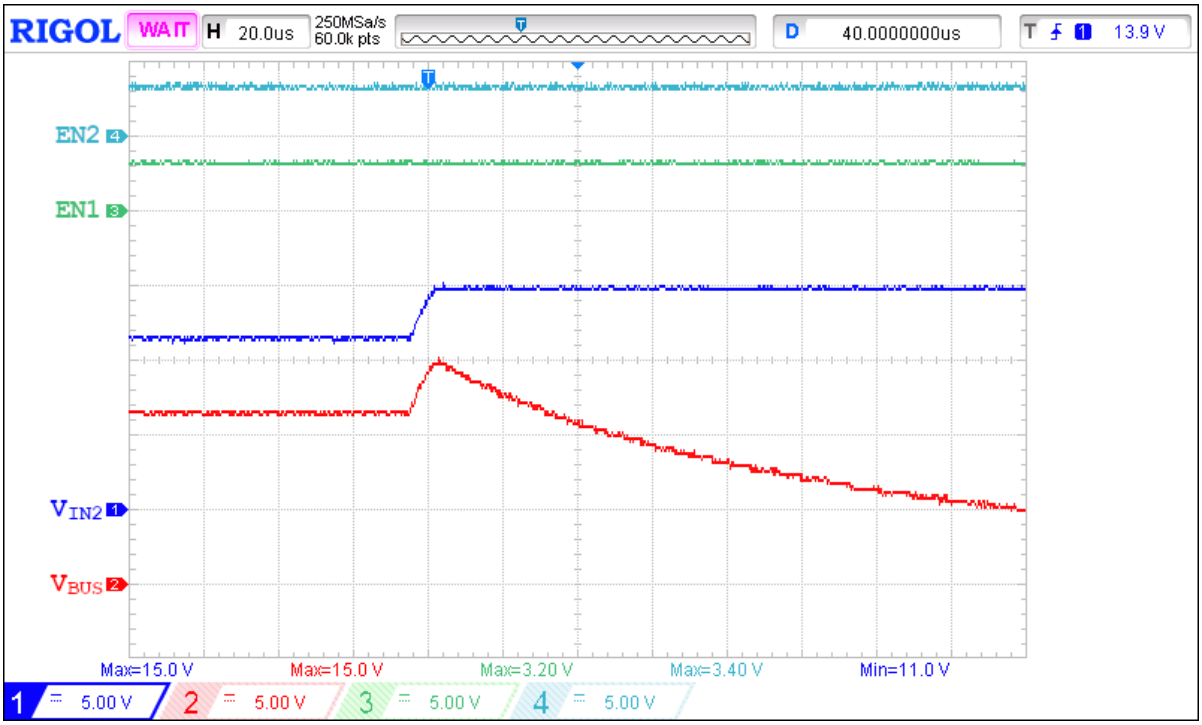

Figure 14: OVP behavior and proper recovery from Latch-Off waveform for Channel 2 of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V step up to 15 V, EN1 = High, EN2 = High, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF (extended view)

4.3.2. Under-Voltage Lockout

The Under-Voltage Lockout is always monitoring the input voltage regardless of the active channel. Once $V_{IN1} < V_{IN1\_UVLO} - V_{IN1\_UVLO\_HYS}$ or $V_{IN2} < V_{IN2\_UVLO} - V_{IN2\_UVLO\_HYS}$ an SLG59H1405V is turned off. To recover to normal operation both $V_{IN[1,2]}$ should be higher than $V_{IN[1,2]\_UVLO}$.

The following application scope-shots below demonstrates the Under-Voltage Lockout behavior of the SLG59H1405V device for V_{IN1} = 5 V step down to 3 V, V_{IN2} = 12 V. A typical connection diagram for these conditions is illustrated in Figure 4.

In case of UVLO occurring while Channel 2 is selected by using SLG59H1405V, then after both input voltages are back to normal, Channel 2 should be turned on according to the sequence described in Power-Up Considerations section [1]. On Figure 15 the UVLO behavior while Channel 2 is selected is shown.

Please note, if this sequence is not followed, Channel 2 will be disabled, signals on EN2 will be ignored, and only Channel 1 will be active as shown in Figure 16.

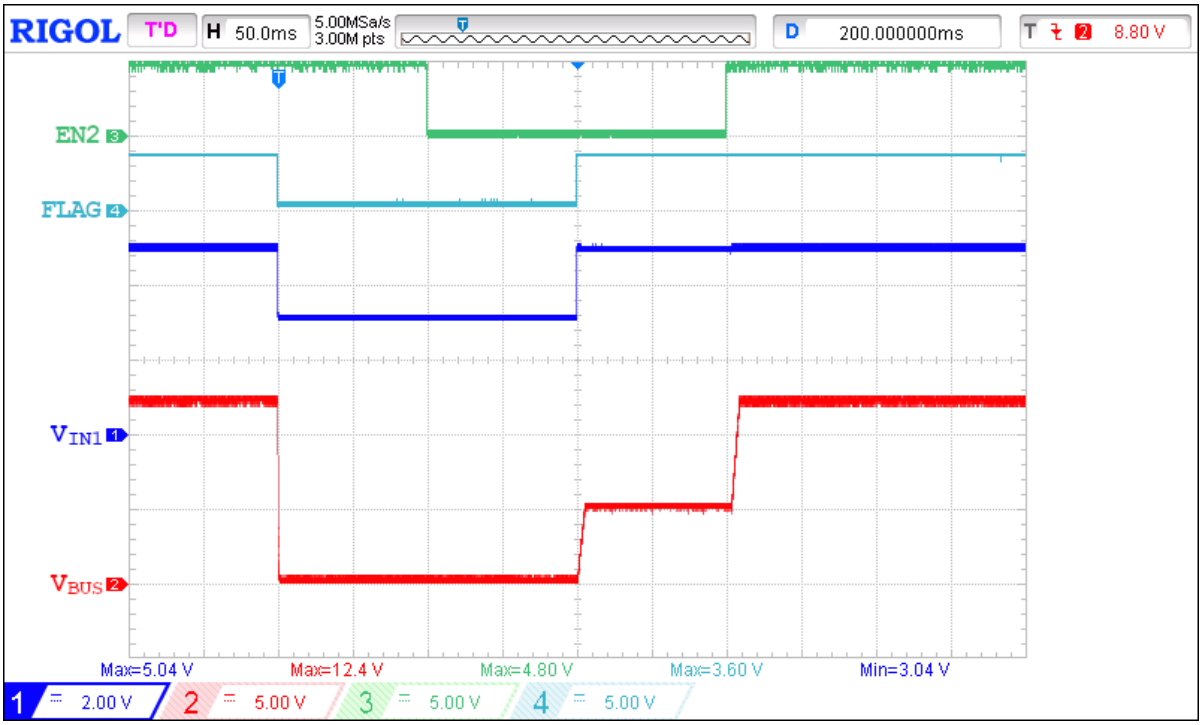

Figure 15: UVLO behavior and proper recovery waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V step down to 3 V, V_{IN2} = 12 V, EN1 = High, EN2 = High → Low → High, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF

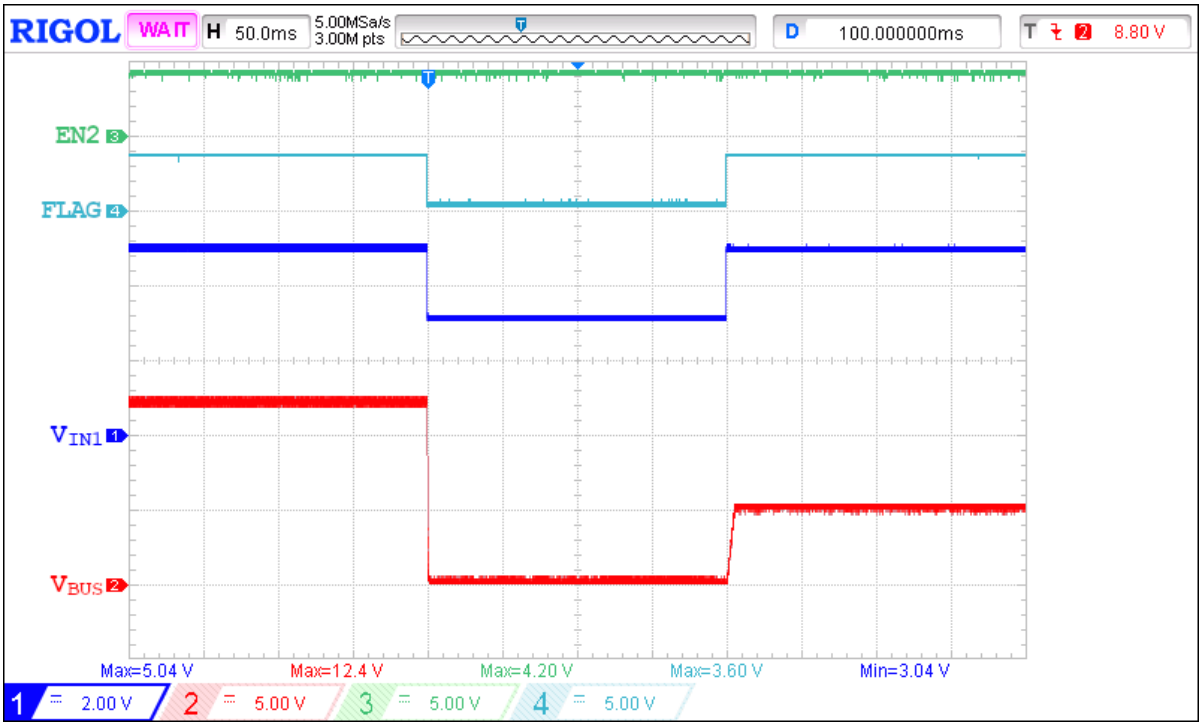

Figure 16: UVLO behavior waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V step down to 3 V, V_{IN2} = 12 V, EN1 = High, EN2 = High, R_{LOAD} = 100 Ω, C_{LOAD} = 2.2 µF

4.3.3. Over current protection

Overcurrent protection is designed to protect the entire device from damage due to the excessive current of the connected device. Such protection significantly increases the fault tolerance of the entire device.

The output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics Table 1. The current limiting circuit is very fast and responds within a few microseconds to sudden loads. When an overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceeding the Active Current Limit for T_{OCP_delay} and then, if the overcurrent condition persists, the SLG59H1405V is latched-off. To release the part from latch-off state, both EN[1,2] should be lower than EN[1,2]_V_{IL}.

The ACL level can be adjusted by choosing the appropriate ±1 %-tolerance R_{ILIM1} resistor value for Channel 1 and R_{ILIM2} resistor value for Channel 2 and can be calculated by the following equations:

For R_{ILIM1} ranging from 160 kΩ to 20 kΩ and for R_{ILIM2} ranging from 75 kΩ to 20 kΩ

$$I_{ACL\_VIN1}\ (A) = 54.985 \times {R_{ILIM1}}^{-0.874}, \text{and}$$

$$I_{ACL\_VIN2}\ (A) = 48.08 \times {R_{ILIM2}}^{-1.071},$$

where:

$R_{ILIM[1,2]}$ = Resistor on ILIM[1,2] pins, in kOhms (Ω)

Please note that if $R_{ILIM[1,2]}$ > 600 kΩ, $I_{LIM[1,2]}$ pin is open, $R_{ILIM[1,2]}$ < 2 kΩ or $I_{LIM[1,2]}$ pin is shorted to GND the ACL threshold will be $I_{ACL\_VIN[1,2]}$ = 0.5 A.

Table 1: Setting Current Limit level vs. $R_{ILIM[1,2]}$

R_{ILIM1}, (kΩ)	I_{ACL_VIN1} (A)	R_{ILIM2}, (kΩ)	I_{ACL_VIN2} (A)
600	0.5	600	0.5
160	0.65	75	0.47
130	0.78	56	0.65
80	1.19	40	0.93
40	2.19	27	1.41
27	3.08	20	1.94
20	4.01	2	0.5
2	0.5		

During active current limit operation, the die temperature rises due to the increased FET resistance. If the die temperature exceeds the $THERM_{ON}$ specification, the SLG59H1405V will also latch-off. To release the part from latch-off state both EN[1,2] should be lower than EN[1,2]_V_{IL}.

The following application scope-shot below demonstrates the Over Current Protections behavior for Channel 1 of the SLG59H1405V device for V_{IN1} = 5 V, V_{IN2} = 12 V, with abnormal step load R_{LOAD} = 1 Ω. A typical connection diagram for these conditions is illustrated in Figure 17.

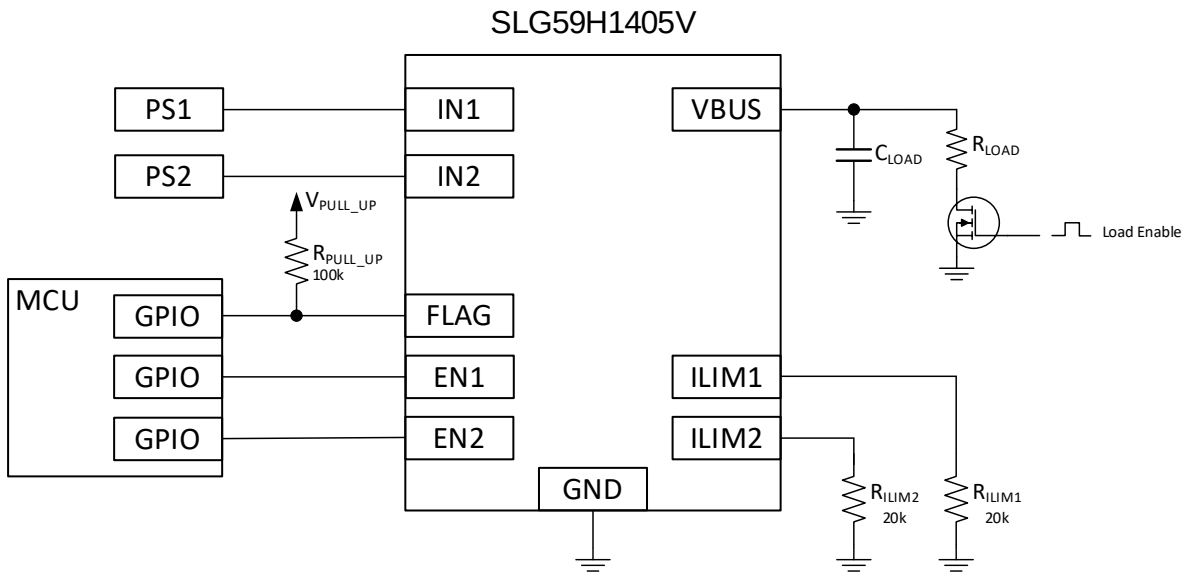

Figure 17: Connection diagram of using SLG59H1405V in PowerMUX applications during OCP for V_{IN1} = 5 V, V_{IN2} = 12 V

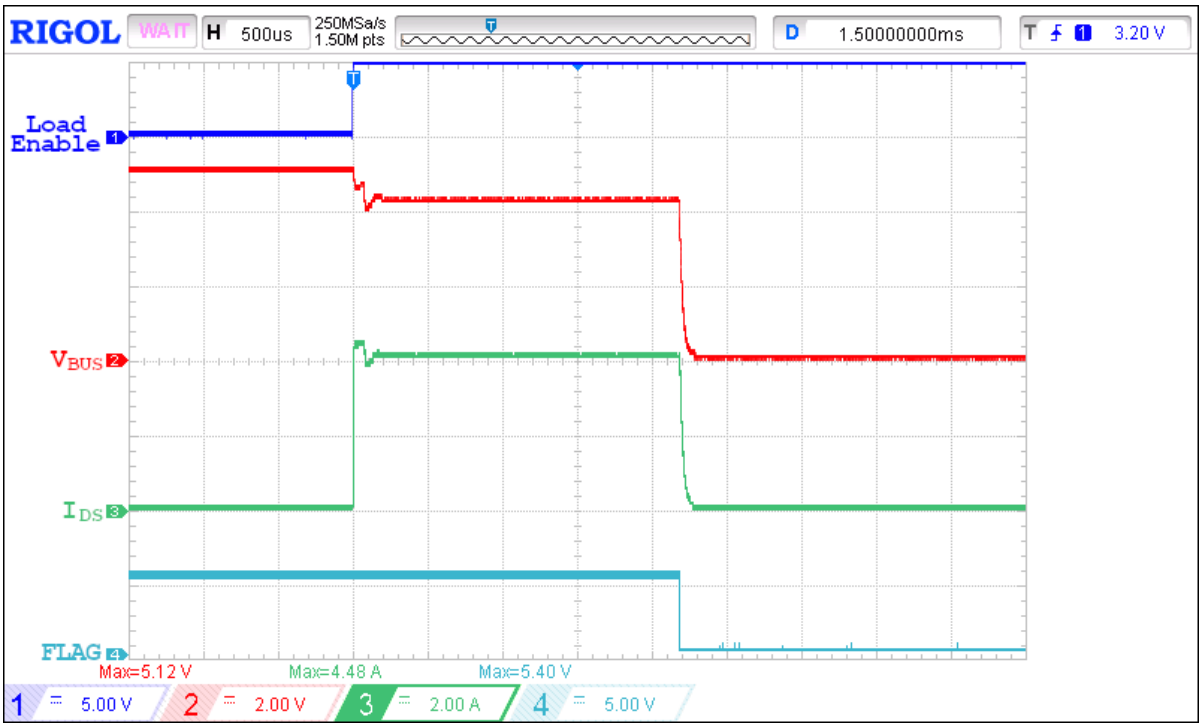

Figure 18: OCP behavior waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = High, EN2 = Low, R_{LOAD} = 1 Ω, C_{LOAD} = 20 µF

4.3.4. Short-Circuit Protection

Short-circuit protection is designed to protect the entire device from damage caused by high short-circuit currents. A short circuit can occur as a result of the failure of the connected device or as a result of mechanical impact on the device. Such protection significantly increases the fault tolerance of the entire device.

Once output I_{VBUS} current will hit the Short-Circuit Protection Threshold (I_{SCP}) the SLG59H1405V will immediately shutdown, and then repower-up with lower current limit threshold that can be calculated by following equation:

$$I_{LIM\_SCP}\ (A) = \frac{I_{ACL\_VIN[1,2]}}{I_{LIM\_FOLD}},$$

where:

I_{LIM_SCP} = VBUS Current Limit after Triggering VBUS Short Circuit Protection

$I_{ACL\_VIN[1,2]}$ = Active Current Limit threshold set by $R_{ILIM[1,2]}$

This repower-up will last during T_{OCP_delay} time and then SLG59H1405V will latch-off. To release the part from latch-off state both EN[1,2] should be lower than EN[1,2]_V_{IL}.

The following application scope-shots below demonstrate the Short-circuit Protections behavior for the Channel 1 of the SLG59H1405V device for V_{IN1} = 5 V, V_{IN2} = 12 V, with abnormal step load R_{SHORT} = 0.5 Ω. A typical connection diagram for these conditions is illustrated in Figure 19. For Channel 2 the Short-circuit Protections have the same behavior with corresponding I_{LIM_SCP} current.

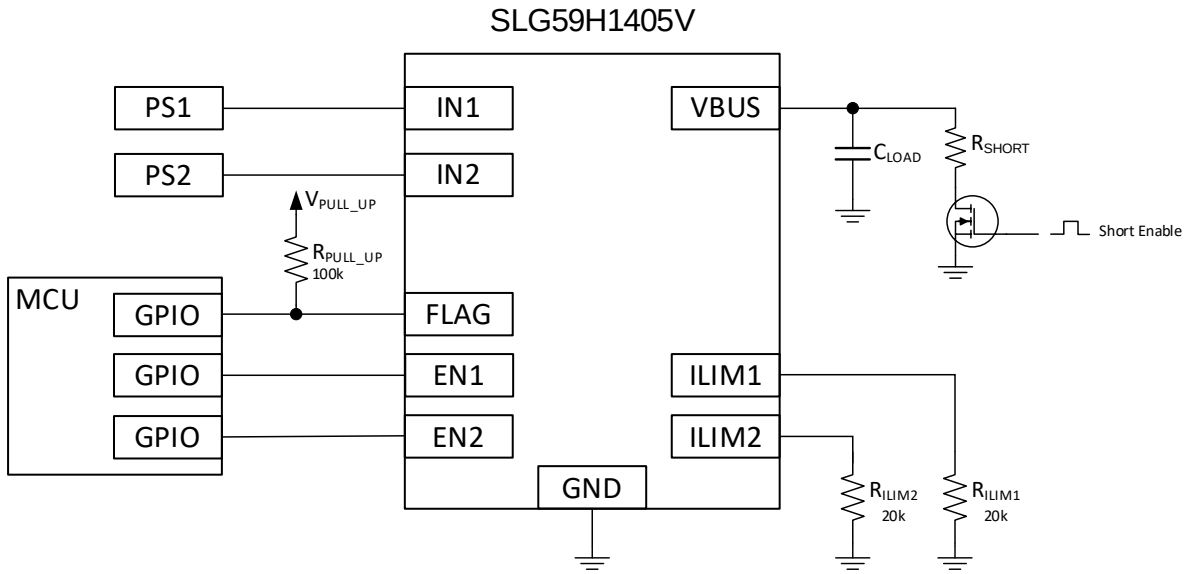

Figure 19: Connection diagram of using SLG59H1405V in PowerMUX applications during SCP for V_{IN1} = 5 V, V_{IN2} = 12 V

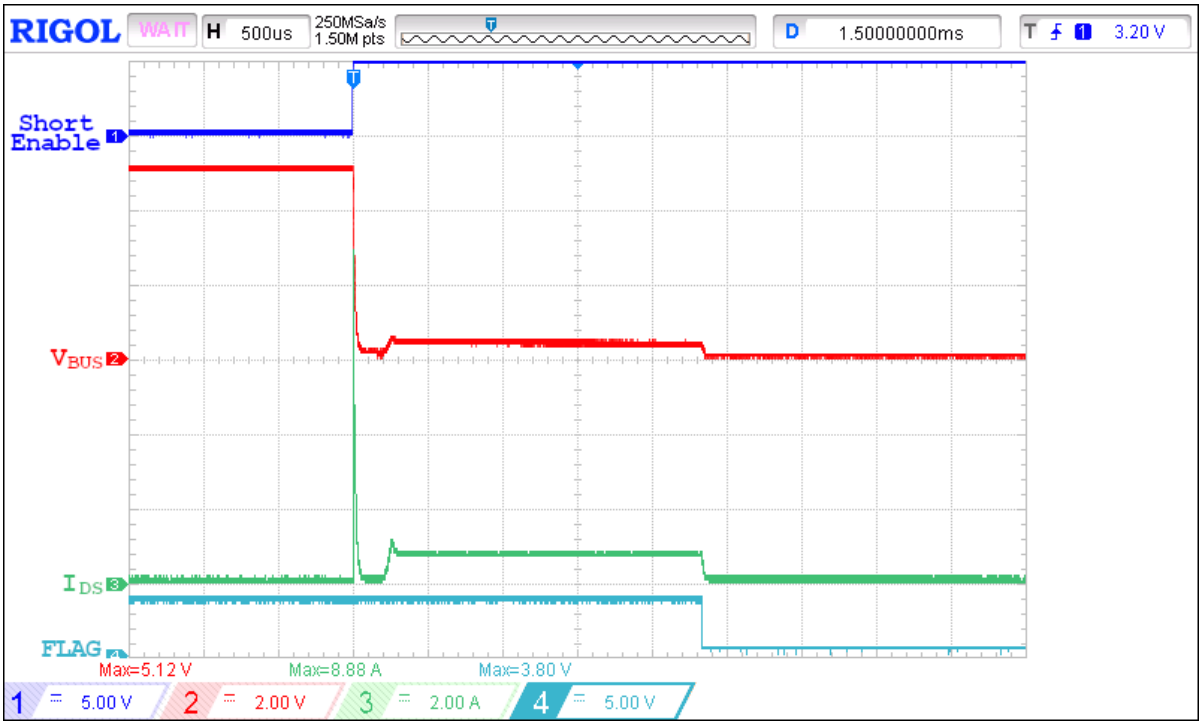

Figure 20: SCP behavior waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = High, EN2 = Low, R_{SHORT} = 0.5 Ω, C_{LOAD} = 20 µF

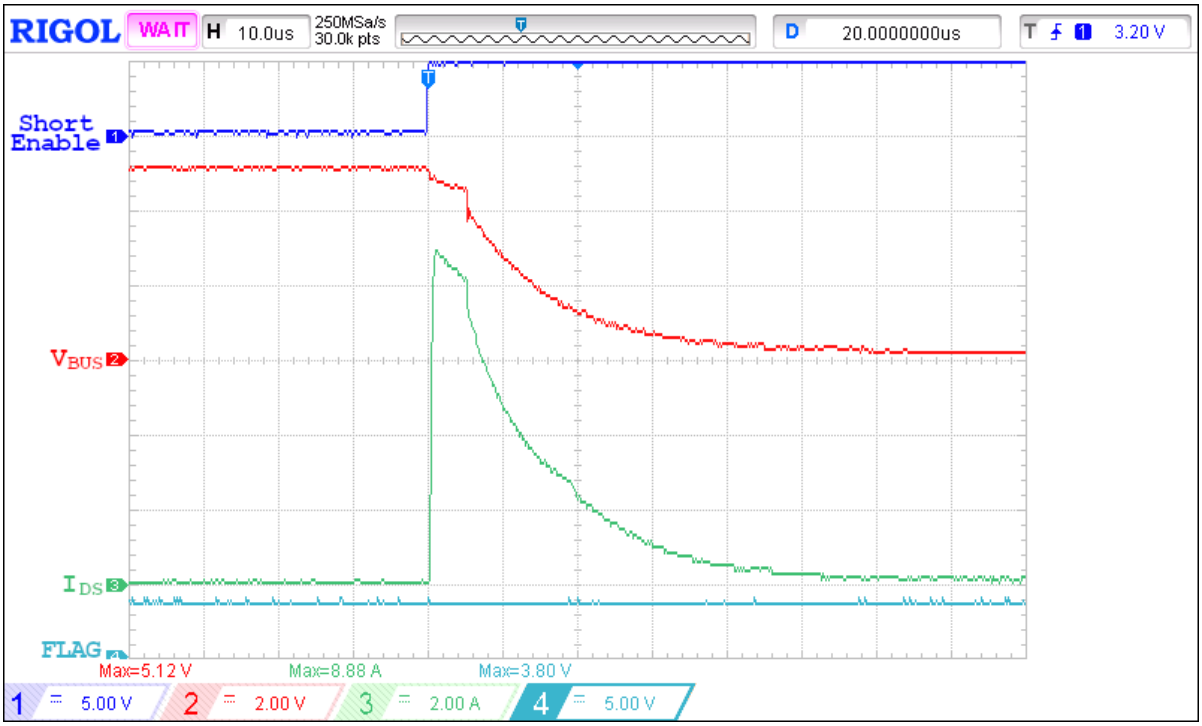

Figure 21: SCP behavior waveform for Channel 1 of the SLG59H1405V for V_{IN1} = 5 V, V_{IN2} = 12 V, EN1 = High, EN2 = Low, R_{SHORT} = 0.5 Ω, C_{LOAD} = 20 µF (extended view)

5. Conclusion

PowerMux is an indispensable device for the applications that uses several input powers supplies to a common output load. Using the Renesas SLG59H1405V device, which was specially designed for PowerMux applications, the process of controlling switching between different sources will be easier and safer, because Renesas SLG59H1405V IC has protection against over and under voltages as well as overcurrent and overtemperature and such solutions significantly increases system reliability.

6. Revision History

Revision	Date	Description
1.00	Jul 19, 2023	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.