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Renesas Electronics Corporation

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M16C/62 Group

A-D Converter OP-AMP Gain Adjustment Connection Mode

1. Abstract

This application note describes the operation of gain adjustment by using operational amplifier for A-D converter.

2. Introduction

This application note is applied to the M16C/62 group Microcomputers.

This program can be also operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/62 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Detailed description

This example describes the operation of gain adjustment by using external operational amplifier for M16C/62 group microcomputers.

3.1 Example of wiring

Figure 1 illustrates the operation of gain adjustment by using external operational amplifier.

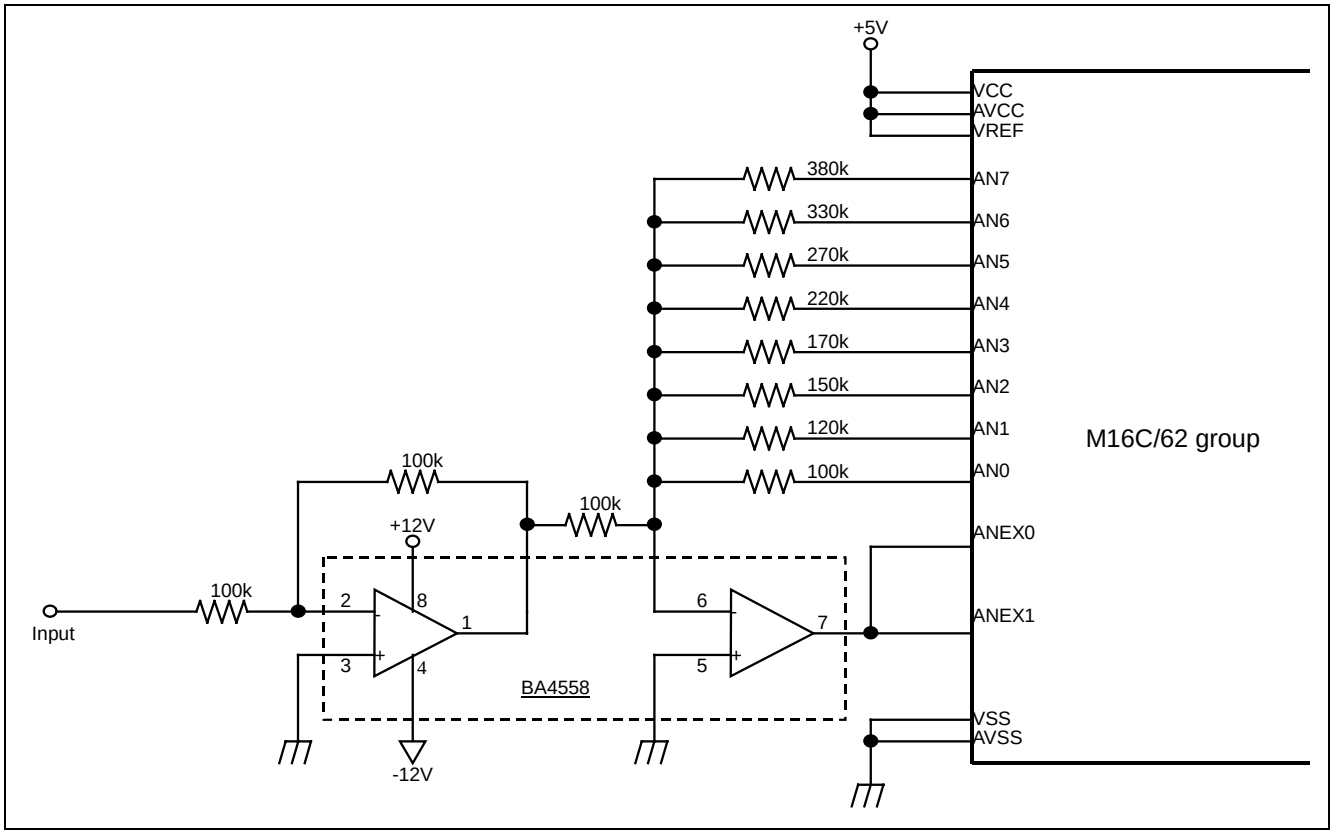


Figure1. Example of wiring

Note

(1)In this example, using 2nd inverting amplified circuit, feedback to in-phase.

The result shows a difference from this sample when use non-inverting amplified circuit.

(2)In this example, values input to AN0 to AN7 are amplified as below, due to the ratio of the value of resistance.

AN0: 100k/100k=1 (1 time amplified)

AN1: 120k/100k=1.2 (1.2 times amplified)

AN2: 150k/100k=1.5 (1.5 time amplified)

AN3: 170k/100k=1.7 (1.7 times amplified)

AN4: 220k/100k=2.2 (2.2 times amplified)

AN5: 270k/100k=2.7 (2.7 times amplified)

AN6: 330k/100k=3.3 (3.3 times amplified)

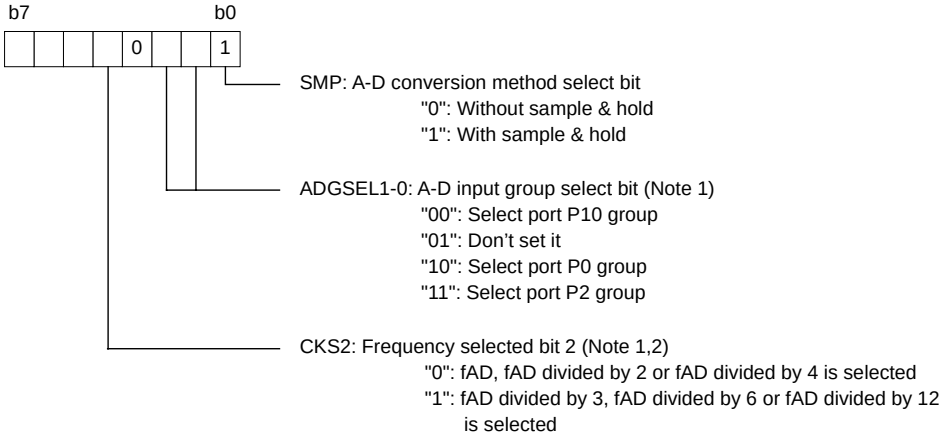
AN7: 380k/100k=3.8 (3.8 times amplified)

3.2 How to set up

This section shows the setting procedures when A-D conversion is carried out, for the output of the gain adjustment, by using external operational amplifier. Examples of A-D conversion with sample & hold function for one-shot mode and 10-bit mode are described.

(1) Setting ADCON2 register (A-D control register 2)

Setting A-D conversion method and frequency select bit

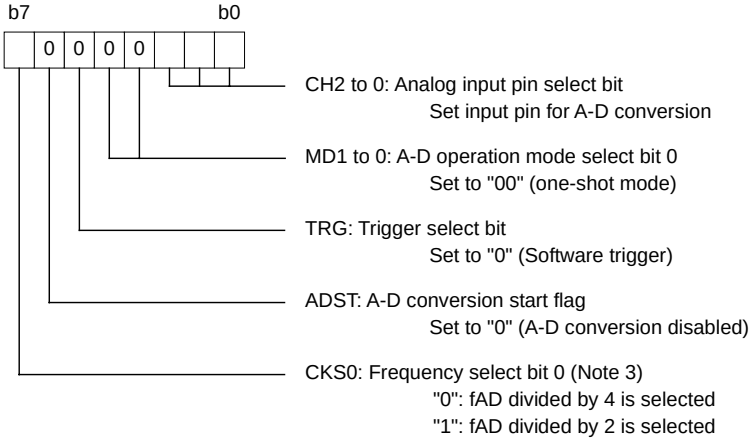


Note 1: Only applied to M16C/62P group. For other group please set to "00".
Note 2: Select the frequency of ϕAD for M16C/62P group according to the following combination.

CKS2	CKS1	CKS0	ϕAD
0	0	0	Divided-by-4 of fAD
0	0	1	Divided-by-2 of fAD
0	1	0	fAD
0	1	1	
1	0	0	Divided-by-12 of fAD
1	0	1	Divided-by-6 of fAD
1	1	0	Divided-by-3 of fAD
1	1	1	

(2) Setting ADCON0 register (A-D control register 0)

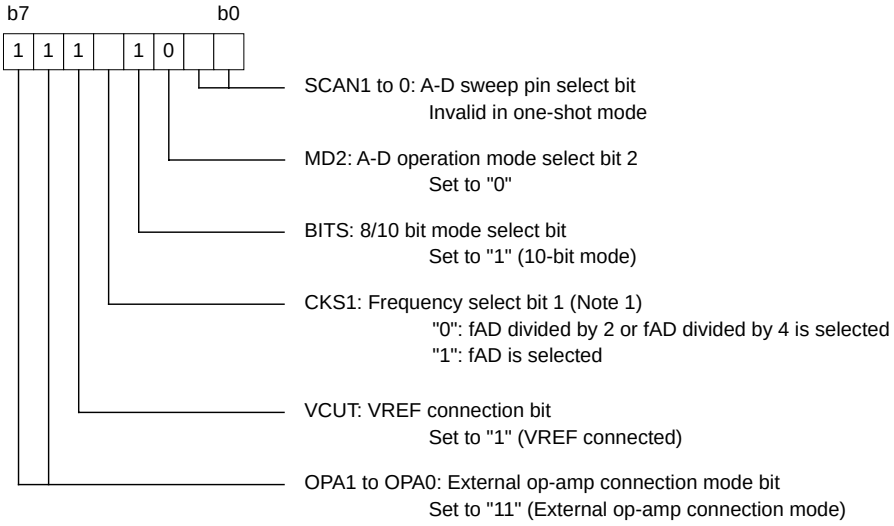
Analog input pin select bit, A-D operation mode, frequency select bit



Note 3: Refer to "3.2 (1) Note 2" for details the setting example for M16C/62P group.

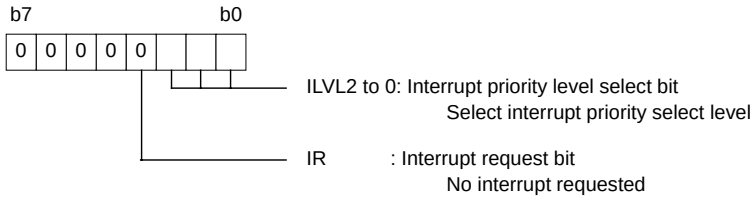
(3) Setting ADCON1 register (A-D control register 1)

Setting A-D operation mode select bit 1, 8/10-bit mode select bit, frequency select bit 1, external op- amp connection mode bit.



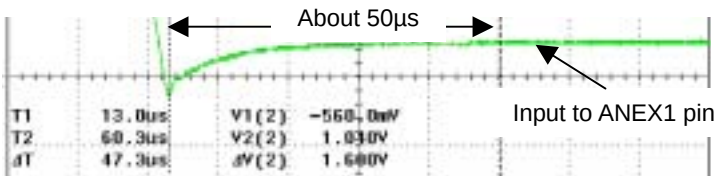
Note 1: Refer to "3.2 (1) Note 2" for details the setting example for M16C/62P group.

(4) ADIC register (A-D interrupt control register)



(5) Waiting until external op-amp operation is stable

Waiting until external op-amp operation is stable. (Varied from the op-amp being used)
In the wiring example of 3.1, it takes 50µs until input value to ANEX1 pin becomes stable.



(6) A-D conversion start

A-D conversion start when setting ADST bit of ADCON0 register to "1".

(7) Waiting for A-D conversion complete

Wait until IR bit in ADIC register reaches to "1" (interrupt request).

(8) Reading of result of A-D conversion

Read A-D register i (i=0 to 7) corresponding to selected pin in analog input select bit.

4. Reference

Hardware Manual

M16C/62 group (M16C/62P) Hardware Manual Rev.1.11
M16C/62 group data sheet Rev.H2
M16C/62A group data sheet Rev.C1
M16C/62N group data sheet Rev.1.1
(Use the latest version on the web-site: http://www.renesas.com)

User's Manual

M16C/62 group User's Manual Rev.C3
M16C/62A group User's Manual Rev.1.0
(Use the latest version on the web-site: http://www.renesas.com)

5. Web-site and contact for support

Renesas web-site

http://www.renesas.com/

Contact for Renesas technical support

E-mail: support_apl@renesas.com

6. The example of a reference program

The following program shows a sequential reading of gain amplified value from AN0 to AN7 by connecting to external operational amplifier.

```
;***********************************************************************
;
;   M16C/62 Group Program Collection
;
;   FILE NAME : rjj05b0441_src.a30
;   CPU       : M16C/62 Group
;   FUNCTION  : The example of A-D conversion at the time of external
;             operational amplifier gain adjustment
;   HISTORY   : 2004.01.15 Ver 1.00
;
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;
;***********************************************************************

;   ----- include define -----
    .list      off
    .include    sfr62p.inc
    .list      on

;
;   ----- Symbol define -----
vstack     .equ       0002b00h       ; Stack Pointer
vram       .equ       0000400h       ; Internal RAM area
vram_end    .equ       0002c00h       ;
vpro       .equ       00fc000h       ; Program Start address
vval_vec    .equ       00ffd00h       ; Variable vector address
vvector     .equ       00fffdch       ; Non-maskable vector address
;
;   ----- Internal RAM Area -----
    .section    ramdata,data
    .org       vram

;
;   ----- Program Area -----
    .section    program,code
    .org       vpro
reset:
;
;   ----- Initial setting -----
    ldc     #vstack,sp              ; Set stack-pointer address
    ldintb  #vval_vec               ; Set variable vector table address
;
    mov.b   #003h, prcr
    mov.b   #008h, cm0
    mov.b   #020h, cm1              ; main-clock divid by 0 mode
    mov.b   #000h, prcr

    mov.w   #00000h, p0
    mov.w   #0ffffh, pd0            ; Port0/1 output select
    mov.w   #00000h, p2
    mov.w   #0ffffh, pd2            ; Port2/3 output select
    mov.w   #00000h, p4
    mov.w   #0ffffh, pd4            ; Port4/5 output select
    mov.w   #00000h, p6
    mov.w   #0ffffh, pd6            ; Port6/7 output select

    bset    prc2
    mov.b   #000h, pd9              ; P9_5(ANEX0) & P9_6(ANEXq) is input port
    mov.b   #000h, pd10             ; P10_0(AN0) to P10_7(AN7) is input port
;
;----- Evaluation start -----
start:
    mov.b   #00000001b, adcon2
;              | ||+---------------------- conversion mode select  : sample&hold
;              | ++----------------------- input group select      : select P10 group
;              +------------------------- Freq select bit2        : fAD/2

    mov.b   #10000000b, adcon0
;           |||||+++---------------------- input select           : AN0 select
;           |||++------------------------- mode select bit0       : single mode
;           ||+--------------------------- trigger select         : software
;           |+---------------------------- AD start flag          : stop
;           +----------------------------- Freq select bit0       : fAD/2
```

```
    mov.b   #11100000b, adcon1
;           ||||||++--------------------- sweep pin select       : none
;           |||||+---------------------- mode select bit1       : 0 fix
;           ||||+----------------------- 8/10 bit select        : 8bit
;           |||+------------------------ Freq select bit1       : fAD/2
;           ||+------------------------- VREF connect bit       : VREF connect
;           ++-------------------------- Ext ope-amp connect mode : Ext ope-amp connebt

    mov.b   #007h,adic              ; set AD interrupt prioliry level

main_loop:
;
;   ----- AN0 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000000b, adcon0

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an0_wait:                           ; wait for AN0 conversion complate
    btst    ir_adic
    jnc     an0_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad0, p0                 ; conversion result display

;
;   ----- AN1 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000001b, adcon0
;               +++-------------------- input select    : AN1 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an1_wait:                           ; wait for AN1 conversion complate
    btst    ir_adic
    jnc     an1_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad1, p1                 ; conversion result display

;
;   ----- AN2 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000010b, adcon0
;               +++-------------------- input select    : AN2 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an2_wait:                           ; wait for AN2 conversion complate
    btst    ir_adic
    jnc     an2_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad2, p2                 ; conversion result display

;
;   ----- AN3 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000011b, adcon0
;               +++-------------------- input select    : AN3 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an3_wait:                           ; wait for AN3 conversion complate
    btst    ir_adic
    jnc     an3_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad3, p3                 ; conversion result display

;
;   ----- AN4 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000100b, adcon0
;               +++-------------------- input select    : AN4 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
```

```
an4_wait:                           ; wait for AN4 conversion complate
    btst    ir_adic
    jnc     an4_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad4, p4                 ; conversion result display

;
;   ----- AN5 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000101b, adcon0
;               +++---------------------- input select    : AN5 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an5_wait:                           ; wait for AN5 conversion complate
    btst    ir_adic
    jnc     an5_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad5, p5                 ; conversion result display

;
;   ----- AN6 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000110b, adcon0
;               +++---------------------- input select    : AN6 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an6_wait:                           ; wait for AN6 conversion complate
    btst    ir_adic
    jnc     an6_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad6, p6                 ; conversion result display

;
;   ----- AN7 conversion -----

    bclr    adst                    ; AD conversion stop
    mov.b   #10000111b, adcon0
;               +++---------------------- input select    : AN7 select

    jsr     AD_wait

    bset    adst                    ; AD conversion start
an7_wait:                           ; wait for AN7 conversion complate
    btst    ir_adic
    jnc     an7_wait
    bclr    ir_adic                 ; AD interrupt req clear

    mov.b   ad7, p7                 ; conversion result display

;   ----- AD conversion complated -----
    mov.b   #0ffh, pd8
    mov.b   #0ffh, p8
end_loop:
    jmp     end_loop                ; Infinity loop

;
;   ----- Opeamp wakeup wait routine -----
AD_wait:
    mov.b   #000b, ta0mr             ; for Opeamp wakeup wait
    mov.w   #1600-1, ta0             ; 100us(16MHz,f1)
    bset    ta0s                    ; TA0 start
ta0_wait:
    btst    ir_ta0ic                ; TA0 overflow wait
    jnc     ta0_wait
    bclr    ir_ta0ic

    rts
;
;----- Evaluation end -----
;
;/////////////////////////////////////////////////////////////////////
;   interrupt routine
;/////////////////////////////////////////////////////////////////////
dummyi:                             ; Dummy interrupt routine
;
       nop
       nop
       nop
       nop
```

```
      reit
;
;/////////////////////////////////////////////////////////////////////
;  Non-maskable interrupt routine
;/////////////////////////////////////////////////////////////////////
undi:                           ; Undefined instruction interrupt
ovfli:                          ; Overflow interrupt
brki:                           ; BRK instruction interrupt
addri:                          ; Address match interrupt
wdti:                           ; Watch-dog timer interrupt
nmii:                           ; NMI interrupt
;
   nop
   nop
   nop
   nop
   reit

;
;/////////////////////////////////////////////////////////////////////
;  Variale vector table
;/////////////////////////////////////////////////////////////////////
   .section   val_vector,romdata
   .org       vval_vec
;
   .lword     dummyi               ; 0=BRK instruction interrupt
   .lword     dummyi               ; 1=
   .lword     dummyi               ; 2=
   .lword     dummyi               ; 3=
   .lword     dummyi               ; 4=^INT3 interrupt
   .lword     dummyi               ; 5=TB5 interrupt
   .lword     dummyi               ; 6=TB4/Uart1 bus collision interrupt
   .lword     dummyi               ; 7=TB3/Uart0 bus collision interrupt
   .lword     dummyi               ; 8=SIO4/^INT5 interrupt
   .lword     dummyi               ; 9=SIO3/^INT4 interrupt
   .lword     dummyi               ;10=Uart2 bus collision interrupt
   .lword     dummyi               ;11=DMA0 interrupt
   .lword     dummyi               ;12=DMA1 interrupt
   .lword     dummyi               ;13=KEY input interrut
   .lword     dummyi               ;14=AD interrupt
   .lword     dummyi               ;15=Uart2 transmit/NACK2 interrupt
   .lword     dummyi               ;16=Uart2 receive/ACK2 interrupt
   .lword     dummyi               ;17=Uart0 transmit/NACK0 interrupt
   .lword     dummyi               ;18=Uart0 receive/ACK0 interrupt
   .lword     dummyi               ;19=Uart1 transmit/NACK1 interrupt
   .lword     dummyi               ;20=Uart1 receive/ACK1 interrupt
   .lword     dummyi               ;21=TA0 interrupt
   .lword     dummyi               ;22=TA1 interrupt
   .lword     dummyi               ;23=TA2 interrupt
   .lword     dummyi               ;24=TA3 interrupt
   .lword     dummyi               ;25=TA4 interrupt
   .lword     dummyi               ;26=TB0 interrupt
   .lword     dummyi               ;27=TB1 interrupt
   .lword     dummyi               ;28=TB2 interrupt
   .lword     dummyi               ;29=^INT0 interrupt
   .lword     dummyi               ;30=^INT1 interrupt
   .lword     dummyi               ;31=^INT2 interrupt
   .lword     dummyi               ;32=
   .lword     dummyi               ;33=
   .lword     dummyi               ;34=
   .lword     dummyi               ;35=
   .lword     dummyi               ;36=
   .lword     dummyi               ;37=
   .lword     dummyi               ;38=
   .lword     dummyi               ;39=
   .lword     dummyi               ;40=
   .lword     dummyi               ;41=
   .lword     dummyi               ;42=
   .lword     dummyi               ;43=
   .lword     dummyi               ;44=
   .lword     dummyi               ;45=
   .lword     dummyi               ;46=
   .lword     dummyi               ;47=
   .lword     dummyi               ;48=
   .lword     dummyi               ;49=
   .lword     dummyi               ;50=
   .lword     dummyi               ;51=
   .lword     dummyi               ;52=
   .lword     dummyi               ;53=
   .lword     dummyi               ;54=
   .lword     dummyi               ;55=
   .lword     dummyi               ;56=
   .lword     dummyi               ;57=
   .lword     dummyi               ;58=
   .lword     dummyi               ;59=
   .lword     dummyi               ;60=
   .lword     dummyi               ;61=
   .lword     dummyi               ;62=
```

```
    .lword     dummyi               ;63=

;
;/////////////////////////////////////////////////////////////////////
;   Non-Maskable interrupt vector table
;/////////////////////////////////////////////////////////////////////
    .section    vector,romdata
    .org       vvector
;
    .lword     undi                 ; ffffdc to f Undefined instruction interrupt
    .lword     ovfli                ; fffe0 to 3 Overflow interrupt
    .lword     brki                 ; fffe4 to 7 BRK instruction interrupt
    .lword     addri                ; fffe8 to b Address match interrupt
    .lword     dummyi               ; ffffec to f
    .lword     wdti                 ; fffff0 to 3 Watch-dog timer interrupt
    .lword     dummyi               ; fffff4 to 7
    .lword     nmii                 ; fffff8 to b NMI interrupt
    .lword     reset                ; fffffc to f RESET
;
.end
```

Revision history

Rev.	Issue date		Revised
		Page	Point
1.00	2004.03.18	-	First edition issued

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