Application Note

DA9061/2 Unused Pin Configuration

AN-PM-105

Abstract

This application note describes the recommended configuration for unused pins in applications that use either the DA9061 or DA9062 power management ICs

DA9061/2 Unused Pin Configuration

Contents

Tables

1 Terms and Definitions

DDR	Dual Data Rate
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
I/O	Input/Output
PMIC	Power Management Integrated Circuit
SCL	Serial Clock
SDA	Serial Data

2 References

[1] DA9061, Datasheet, Dialog Semiconductor.

[2] DA9062, Datasheet, Dialog Semiconductor.

3 Introduction

DA9061/2 is a power management integrated circuit (PMIC) optimized for supplying systems with single- and dual-core processors, I/O, DDR memory, and peripherals. It targets mobile devices, medical equipment, IVI systems, and FPGA-based applications.

In some applications, certain functions or features may not be required and, to minimize any potential issues with these unused functions, the pins related to them need to be configured correctly. This document provides guidance on how to configure unused connections on the DA9061/2.

4 DA9061 Functional Blocks

The following tables describe the recommended configurations for unused pins. Mandatory means that the pin is used in all applications.

Table 1: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power	GND	Ground

4.1 Power Manager

Table 2: Power Manager Connections

Pin Number	Signal Name	Type	Description	If Unused
15	nONKEY	DI	On/Off key with optional long press shutdown	Pull up to VSYS
38	nRESET	DO	Active-low reset for host	Leave floating
37	nIRQ	DO	IRQ line for host	Leave floating
23	VDDIO	PWR	I/O supply voltage rail	Mandatory
36	TP	PWR	Test pin: enables Power Commander boot mode and supply pin for OTP fusing voltage	Connect to GND
21	GPIO0	DIO	General purpose I/O	If GPI, tie to non-active state If GPO, leave floating
22	GPIO1	DIO	General purpose I/O	If GPI, tie to non-active state If GPO, leave floating
28	PWR_EN/GPIO2	DI/DIO	Hardware enable of power domain POWER / General purpose I/O	If GPI, tie to non-active state If GPO, leave floating
29	GPIO3	DIO	General purpose I/O	If GPI, tie to non-active state If GPO, leave floating
30	SYS_EN / GPIO4	DI/DIO	Hardware enable of power domain SYSTEM / General purpose I/O	If GPI, tie to non-active state If GPO, leave floating

4.2 2-Wire Interface

Table 3: 2-Wire Interface Connections

Pin Number	Signal Name	Type	Description	If Unused
13	SDA	DIO	2-wire data	Connect to GND
14	SCL	DI	2-wire clock	Connect to GND

4.3 LDO Voltage Regulators

Table 4: Voltage Regulator Connections

Pin Number	Signal Name	Type	Description	If Unused
40	VSYS	PWR	Supply voltage for PMIC, input for voltage supervision (decouple with 1.0 µF) and LDO1 supply	Mandatory
3	VDD_LDO2	PWR	Supply voltage for LDO2	Connect to GND
10	VDD_LDO34	PWR	Supply voltage for LDO3 and LDO4	Connect to GND
1	VLDO1	AO	Output voltage from LDO1	Leave floating Cap not required
2	VLDO2	AO	Output voltage from LDO2	Leave floating Cap not required
9	VLDO3	AO	Output voltage from LDO3	Leave floating Cap not required
11	VLDO4	AO	Output voltage from LDO4	Leave floating Cap not required
39	VDDCORE	AO	Regulated supply for internal circuitry (2.2 V / 2.5 V, decouple with 2.2 µF)	Mandatory

4.4 Buck Converters

Table 5: Buck Converter Connections

Pin Number	Signal Name	Type	Description	If Unused
32	VDD_BUCK1	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND
19	VDD_BUCK2	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND
18	VDD_BUCK3	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND
26	VBUCK1	AI	Voltage feedback for Buck1	Connect to GND
25	VBUCK2	AI	Voltage feedback for Buck2	Connect to GND
24	VBUCK3	AI	Voltage feedback for Buck3	Connect to GND
31	VLX_BUCK1	AO	Switching node for Buck1	Leave floating
20	VLX_BUCK2	AO	Switching node for Buck2	Leave floating
17	VLX_BUCK3	AO	Switching node for Buck3	Leave floating

4.5 Ancillary Functions

Table 6: Ancillary Connections

Pin Number	Signal Name	Type	Description	If Unused
5	VREF	AIO	Filter node for internal reference voltage (decouple with 2.2 µF)	Mandatory
4	IREF	AO	Connection for bias setting (configure with high-precision 200 kΩ resistor)	Mandatory

4.6 GPIO Interrupt Masks

When an unused GPIO is set to be GPI, it is recommended that the respective IRQ mask bit is set to ensure unintentional events are not triggered. This can be done in OTP or, preferably, via software configuration at boot time.

4.7 VSS

Table 7: VSS Connections

Pin Number	Signal Name	Type	Description	If Unused
7	GND	VSS	VSS_ANA	Mandatory

5 DA9062 Functional Blocks

The following tables describe the recommended configurations for unused pins. Mandatory means that the pin is used in all applications.

Table 8: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power	GND	Ground

5.1 Power Manager

Table 9: Power Manager Connections

Pin Number	Signal Name	Type	Description	If Unused
15	nONKEY	DI	On/Off key with optional long press shutdown	Pull up to VSYS
38	nRESET	DO	Active low reset for host	Leave floating
37	nIRQ	DO	IRQ line for host	Leave floating
23	VDDIO	PWR	I/O supply voltage rail	Mandatory
36	TP	PWR	Test pin: enables Power Commander boot mode and supply pin for OTP fusing voltage	Connect to GND

Pin Number	Signal Name	Type	Description	If Unused
28	PWR_EN / GPIO2	DI/DIO	Hardware enable of power domain POWER / General purpose I/O	If GPI, tie to non-active state If GPO, leave floating
29	GPIO3	DIO	General purpose I/O	If GPI, tie to non-active state If GPO, leave floating
30	SYS_EN / GPIO4	DI/DIO	Hardware enable of power domain SYSTEM / General purpose I/O	If GPI, tie to non-active state If GPO, leave floating

5.2 2-Wire Interface

Table 10: 2-Wire Interface Connections

Pin Number	Signal Name	Type	Description	If Unused
13	SDA	DIO	2-wire data	Connect to GND
14	SCL	DI	2-wire clock	Connect to GND

5.3 LDO Voltage Regulators

Table 11: Voltage Regulator Connections

Pin Number	Signal Name	Type	Description	If Unused
40	VSYS	PWR	Supply voltage for PMIC, input for voltage supervision (decouple with 1.0 µF) and LDO1 supply	Mandatory
3	VDD_LDO2	PWR	Supply voltage for LDO2	Connect to GND
10	VDD_LDO34	PWR	Supply voltage for LDO3 and LDO4	Connect to GND
1	VLDO1	AO	Output voltage from LDO1	Leave floating Capacitor not required
2	VLDO2	AO	Output voltage from LDO2	Leave floating Capacitor not required
9	VLDO3	AO	Output voltage from LDO3	Leave floating Capacitor not required
11	VLDO4	AO	Output voltage from LDO4	Leave floating Capacitor not required
39	VDDCORE	AO	Regulated supply for internal circuitry (2.2 V / 2.5 V, decouple with 2.2 µF)	Mandatory

5.4 Buck Converters

Table 12: Buck Converter Connections

Pin Number	Signal Name	Type	Description	If Unused
32	VDD_BUCK1	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND

DA9061/2 Unused Pin Configuration

Pin Number	Signal Name	Type	Description	If Unused
33	VDD_BUCK2	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND
19	VDD_BUCK3	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND
18	VDD_BUCK4	PWR	Supply voltage for buck To be connected to VSYS	Connect to GND
26	VBUCK1	AI	Voltage feedback for Buck1	Connect to GND
27	VBUCK2	AI	Voltage feedback for Buck2	Connect to GND
25	VBUCK3	AI	Voltage feedback for Buck3	Connect to GND
24	VBUCK4	AI	Voltage feedback for Buck4	Connect to GND
31	VLX_BUCK1	AO	Switching node for Buck1	Leave floating
34	VLX_BUCK2_A	AO	Switching node for Buck2	Leave floating
35	VLX_BUCK2_B	AO	Switching node for Buck2	Leave floating
20	VLX_BUCK3	AO	Switching node for Buck3	Leave floating
17	VLX_BUCK4	AO	Switching node for Buck4	Leave floating
21	VDDQ / GPIO0	AI/DO	VDDQ memory supply sense input / General purpose I/O	Leave floating Set BUCK4_VTTR_EN=0
22	VTTR / GPIO1	AO/DO	Memory termination reference voltage / General purpose I/O	Leave floating Set BUCK4_VTTR_EN=0

5.5 Ancillary Functions

Table 13: Ancillary Connections

Pin Number	Signal Name	Type	Description	If Unused
5	VREF	AIO	Filter node for internal reference voltage (decouple with 2.2 µF)	Mandatory
4	IREF	AO	Connection for bias setting (configure with high-precision 200 kΩ resistor)	Mandatory
6	XTAL_IN	AI	32 kHz crystal connection (adjust with 10 pF)	Connect to GND
8	XTAL_OUT	AIO	32 kHz crystal connection (adjust with 10 pF)	Connect to GND

5.6 GPIO Interrupt Masks

When an unused GPIO is set to be GPI, it is recommended that the respective IRQ mask bit is set to ensure unintentional events are not triggered. This can be done in OTP or, preferably, via software configuration at boot time.

5.7 Backup Battery Charger

Table 14: Backup Battery Charger Connections

Pin Number	Signal Name	Type	Description	If Unused
12	VBBAT	PWR	Backup battery connection Coin-cell or super-cap (decouple with 470 nF)	Fit 470 nF capacitor

5.8 VSS

Table 15: VSS Connections

Pin Number	Signal Name	Type	Description	If Unused
7	GND	VSS	VSS_ANA	Mandatory

6 Conclusion

Adherence to the recommendations of this document helps minimize spurious application issues such as noise and increased current consumption, and may avoid device damage due to incorrectly biased pins. For further information please refer to the datasheets [1], [2] on the Dialog website (https://www.dialog-semiconductor.com/pmics) or contact Dialog via either your sales representative or the support forum (https://support.dialog-semiconductor.com/forums/pmic-audio).

Revision History

Revision	Date	Description
1.0	09-Jan-2018	Initial version.
2.0	18-Feb-2022	File was rebranded with new logo, copyright and disclaimer

DA9061/2 Unused Pin Configuration

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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