Application Note

DA9080-61FCB2 Variant Overview - RZ/T2M, RZ/N2L and RZ/T2L MPUs

AN-PM-175

Abstract

This application note describes all the register default settings of the DA9080-61FCB2 variant (the x denotes the package option).

DA9080-61FCB2 is highly suited as the power management system solution for RZ/T2M, RZ/N2L and RZ/T2L MPUs.

DA9080-61FCB2 Variant Overview - RZ/T2M, RZ/N2L and RZ/T2L MPUs

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1 Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
LDO	Low drop out
OTP	One time programmable
PG	Power good
UQFN	Ultra-thin quad flat-pack no-lead (package)

2 References

[1] DA9080_Datasheet, Renesas Electronics.
[2] RZ/T2M Group Datasheet, Renesas Electronics.
[3] RZ/N2L Group Datasheet, Renesas Electronics.
[4] RZ/T2L Group Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3 RZ/T2M, RZ/N2L and RZ/T2L MPUs Power Requirements

For power-up, 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC) must be supplied first, then 3.3-V power (i.e. VCC33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e. RES#) must be held to Low level during the power-up.

For Power-down, 3.3-V power (i.e. VCC33) must go down first and then 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC). The power-down sequence must be completed within 100 ms.

Rise and fall time of each power supply for the power-up and the power-down must be larger than 10 µs.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

Stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when reset signal (i.e. RES#) is driven high.

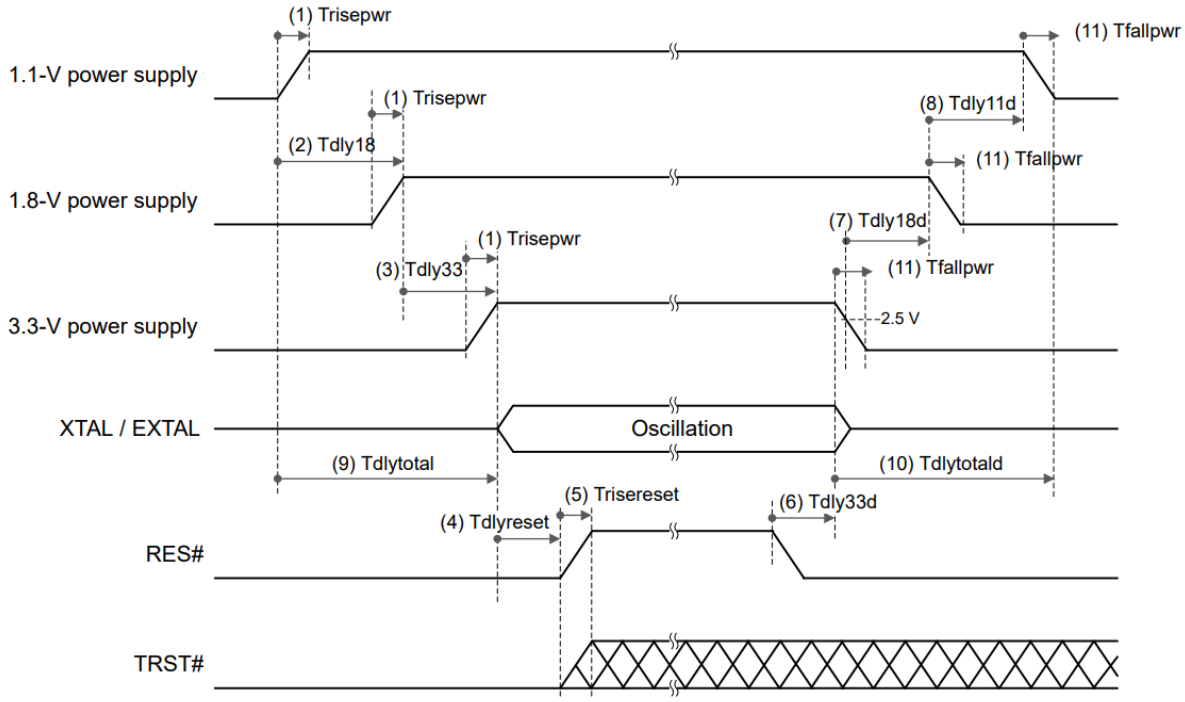

Figure 1: RZ/T2M, RZ/N2L and RZ/T2L MPUs Power On/Off Sequence

4 DA9080 - RZ/T2M, RZ/N2L, RZ/T2L Power Supply Tree Diagram (Top Level)

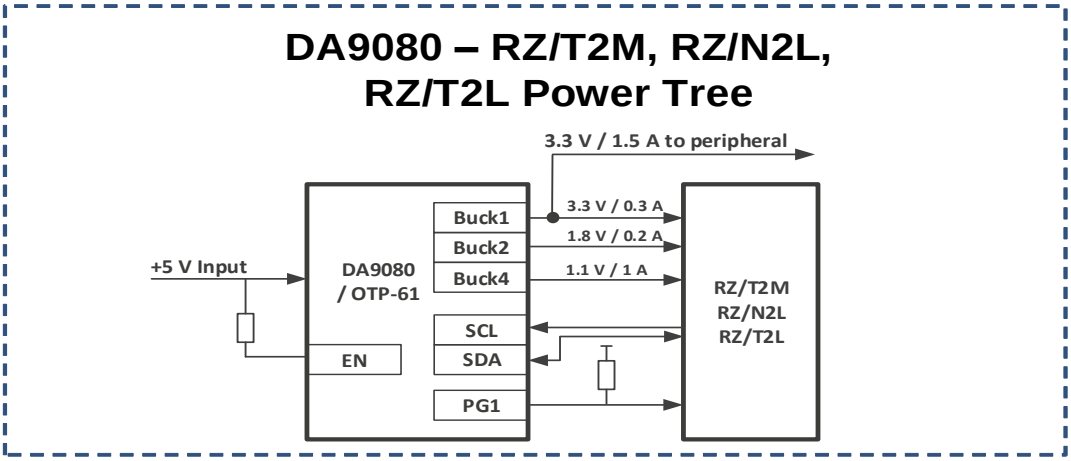

Figure 2: DA9080 - RZ/T2M, RZ/N2L, RZ/T2L Power Tree

5 DA9080 Power On/Off Sequences

Ch1: Buck1 (3.3 V), Ch2: Buck2 (1.8 V), CH3: Buck4 (1.1 V), Ch4: PG1 (OD/PU to 3.3 V)

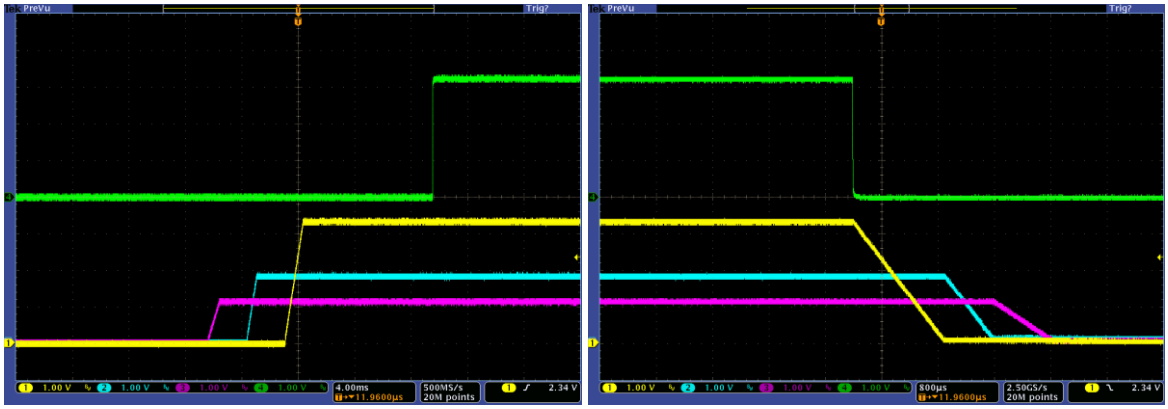

Figure 3: DA9080-61FCB2 Power On/Off Sequences

6 DA9080 Variant Table and Ordering Information

Table 1: Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9080-61FCB2	32 UQFN	5.0 x 5.0 by 0.5 mm pitch	Tape & Reel	4900

7 DA9080-61FCB2 Detailed Description - Production Release

Key settings:

- VCH1 = 3.30 V, VCH2 = 1.80 V, VCH4 = 1.10 V
- CH3 (0.90 V) disabled
- VLDO (3.3 V) disabled
- CH1 = SLOT3, CH2 = SLOT2, CH4 = SLOT1
- CH<x> operates in AUTO mode, 2 MHz
- I^2C standard speed. I^2C slave address = 0x1B (7-bit)

Table 2: Register Settings DA9080-61FCB2 Variant

Register Address	Function	Default Value	Description
0x04	PMC_ADC_ENABLE	0x01	ADC enabled
0x05	PMC_CH_EN	0x16	CH1, CH2 and CH4 enabled CH3 and LDO disabled
0x07	PMC_VOUT_BUCK1	0x3C	VCH1 = 3.30 V
0x08	PMC_VOUT_BUCK2	0x0F	VCH2 = 1.80 V
0x09	PMC_VOUT_BUCK3	0x00	VCH3 = 0.90 V
0x0A	PMC_VOUT_BUCK4	0x3C	VCH4 = 1.10 V
0x0B	PMC_PHASE_INTERLEAVING	0x88	BUCK1_PHASE = 0º BUCK2_PHASE = 180º BUCK3_PHASE = 0º BUCK4_PHASE = 180º
0x0C	PMC_BUCK_SEQ_GRP	0x06	CH1 = SLOT3, CH2 = SLOT2 CH3 = SLOT1, CH4 = SLOT1
0x0D	PMC_LDO_SEQ_GRP	0x00	LDO = SLOT1
0x0E	PMC_PG1	0x16	CH1, CH2 and CH4 assigned to PG1
0x0F	PMC_PG2	0x00	PG2 unused
0x10	PMC_DISCHARGE	0x1F	CH<x> and LDO discharge enabled
0x62	OTP_CONFIG_ID	0x61	OTP variant number: DA9080-61FCB2

8 DA9080-61FCB2 Variant Overview

Table 3: OTP Variant Overview

Reg Add	Function	Standard Variant DA9080-61FCB2
0x04	PMC_ADC_ENABLE	0x01
0x05	PMC_CH_EN	0x16
0x07	PMC_VOUT_BUCK1	0x3C
0x08	PMC_VOUT_BUCK2	0x0F
0x09	PMC_VOUT_BUCK3	0x00
0x0A	PMC_VOUT_BUCK4	0x3C
0x0B	PMC_PHASE_INTERLEAVING	0x88
0x0C	PMC_BUCK_SEQ_GRP	0x06
0x0D	PMC_LDO_SEQ_GRP	0x00
0x0E	PMC_PG1	0x16
0x0F	PMC_PG2	0x00
0x10	PMC_DISCHARGE	0x1F
0x62	OTP_CONFIG_ID	0x61

Revision History

Revision	Date	Description
1	30-Aug-2023	Initial version.
2	05-Oct-2023	File updated to show support for RZ/T2M, RZ/N2L and RZ/T2L MPUs.

DA9080-61FCB2 Variant Overview - RZ/T2M, RZ/N2L and RZ/T2L MPUs

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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