RX140 Group, RX110 Group

Differences Between the RX140 Group and the RX110 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX140 Group and RX110 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 80-pin package version of the RX140 Group and the 64-pin package version of the RX110 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX140 Group and RX110 Group

Contents

1. Comparison of Built-In Functions of RX140 Group and RX110 Group

A comparison of the built-in functions of the RX140 Group and RX110 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX140 Group and RX110 Group.

Table 1.1 Comparison of Built-In Functions of RX140 Group and RX110 Group

Function	RX110	RX140
CPU	●	
Operating modes	○	
Address space	●	
Resets	●	
Option-setting memory (OFSM)	●/■	
Voltage detection circuit (LVDAa): RX110, (LVDAb): RX140	●	
Clock generation circuit	●	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●	
Register write protection function	▲	
Exception handling	●	
Interrupt controller (ICUb)	●	
Buses	●	
Data transfer controller (DTCa): RX110, (DTCb): RX140	●	
Event link controller (ELC)	×	○
I/O ports	●/■	
Multi-function pin controller (MPC)	▲/●	
Multi-function timer pulse unit 2 (MTU2b): RX110, (MTU2a): RX140	●	
Port output enable 2 (POE2a)	×	○
8-bit timer (TMRa)	×	○
Compare match timer (CMT)	●	
Realtime clock (RTCA): RX110, (RTCc): RX140	■	
Low-power timer (LPTa)	×	○
Independent watchdog timer (IWDTa)	○	
Serial communications interface (SCIe, SCIf): RX110, (SCIg*1, SCIk, SCIh): RX140	●	
I²C bus interface (RIIC): RX110, (RIICa): RX140	●	
CAN module (RSCAN0)	×	○*1
Serial peripheral interface (RSPI): RX110, (RSPIc): RX140	●/▲	
CRC calculator (CRC)	○	
Capacitive touch sensing unit (CTSU2SL, CTSU2L)	×	○
AESA	×	○
RNGA	×	○
12-bit A/D converter (S12ADb): RX110, (S12ADE): RX140	▲/●	
D/A converter (DAa)	×	○
Temperature sensor (TEMPSA)	▲	
Comparator B (CMPBa)	×	○
Data operation circuit (DOC)	●	
RAM	●/■	
Flash memory (FLASH)	●/■	
Packages	●/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Note: 1. Not implemented on products with ROM capacity of 64 KB.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX110	RX140
CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 48 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX110	RX140
EXTB	—	—	Exception table register
FPSW	—	—	Floating-point status word
ACC (RX110) ACC0, ACC1 (RX140)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Address Space

Figure 2.1 is a comparative memory map of single-chip mode.

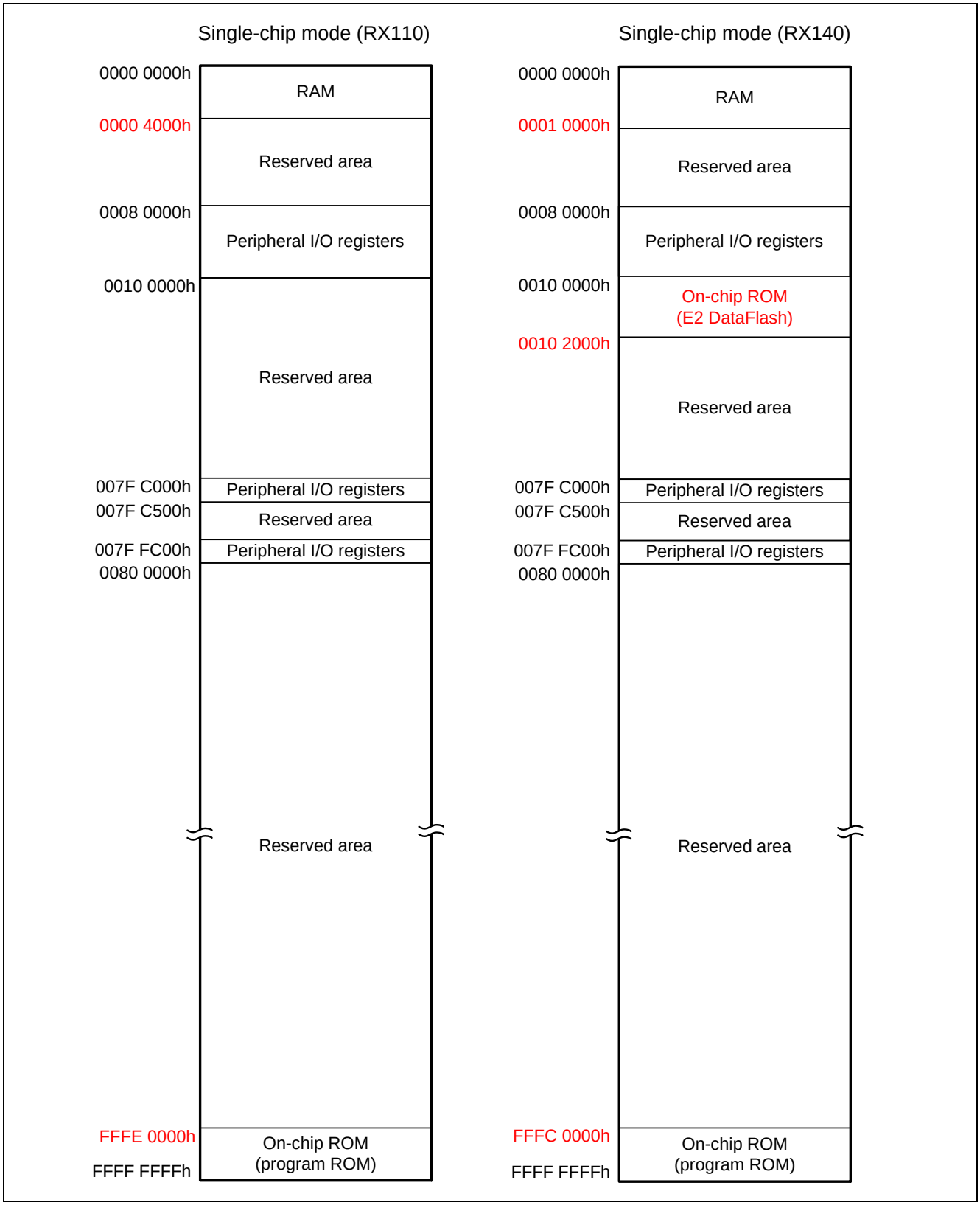

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Resets

Table 2.3 is a comparative overview of resets, and Table 2.4 is a comparison of reset-related registers.

Table 2.3 Comparative Overview of Resets

Item	RX110	RX140
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage detection: VPOR).	VCC rises (voltage detection: VPOR).
Voltage monitoring 0 reset	—	VCC falls (voltage detection: Vdet0).
Voltage monitoring 1 reset	VCC falls (voltage detection: Vdet1).	VCC falls (voltage detection: Vdet1).
Voltage monitoring 2 reset	VCC falls (voltage detection: Vdet2).	VCC falls (voltage detection: Vdet2).
Independent watchdog timer reset	The independent watchdog timer underflows or a refresh error occurs.	The independent watchdog timer underflows or a refresh error occurs.
Software reset	Register setting	Register setting

Table 2.4 Comparison of Reset-Related Registers

Register	Bit	RX110	RX140
RSTSR0	LVD0RF	—	Voltage monitor 0 reset detect flag

2.4 Option-Setting Memory

Table 2.5 is a comparison of option-setting memory registers.

Table 2.5 Comparison of Option-Setting Memory Registers

Register	Bit	RX110	RX140 (OFSM)
OFS1	FASTSTUP	Power-on fast startup time bit (b0)	Power-on fast startup time bit (b3)
	VDSEL[1:0]	—	Voltage detection 0 level select bits
	LVDAS	—	Voltage detection 0 circuit start bit
	STUPLVD1REN	Startup voltage monitoring 1 reset enable bits	—
	STUPLVD1LVL [3:0]	Startup voltage monitoring 1 reset detection level select bits	—
	HOCOFQ[1:0]	—	HOCO frequency selection bits

2.5 Voltage Detection Circuit

Table 2.6 is a comparative overview of the voltage detection circuits, and Table 2.7 is a comparison of voltage detection circuit registers.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX110 (LVDAa)		RX140 (LVDAb)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2
			Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.			Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.
	Detection voltage	Selectable from ten levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits	Selectable from four levels using the OFS1 register	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits
	Monitoring flags	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection	—	LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	Voltage monitoring 0 interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin	Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin

Item		RX110 (LVDAa)		RX140 (LVDAb)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Interrupts	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or CMPA2 pin, VCC or CMPA2 pin > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both
Event link function		—	—	—	Available: Event output at Vdet passage detection	—

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX110 (LVDAa)	RX140 (LVDAb)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.06 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.
	LVD2LVL[1:0]	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 2.90 V 0 1: 2.60 V 1 0: 2.00 V 1 1: 1.80 V*1	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V

Note: 1. When the value of the LVCMPCR.EXVCCINP2 bit is 0 (power supply voltage (VCC)), the setting value of 11b is prohibited.

2.6 Clock Generation Circuit

Table 2.8 is a comparative overview of the clock generation circuits, and Table 2.9 is a comparison of clock generation circuit registers.

Table 2.8 Comparative Overview of Clock Generation Circuits

Item	RX110	RX140
Uses	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT • Generates the LPT clock (LPTCLK) to be supplied to the LPT.
Operating frequency	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM) • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz	• ICLK: 48 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 48 MHz (max.) • FCLK: — 1 MHz to 48 MHz (for programming and erasing the ROM and E2 DataFlash) — 48 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • CANMCLK: 20 MHz (max.) • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as clock from selected oscillator

Item	RX110	RX140
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V), 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN and XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function
PLL circuit	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12 MHz • Frequency multiplication ratio: Selectable from 4 to 12 (increments of 0.5) • Oscillation frequency: 24 MHz to 48 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 24 MHz, 32 MHz, 48 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Table 2.9 Comparison of Clock Generation Circuit Registers

Register	Bit	RX110	RX140
SCKCR3	CKSEL[2:0]	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator Settings other than the above are prohibited.	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.
PLLCR	—	—	PLL control register
PLLCR2	—	—	PLL control register 2

Register	Bit	RX110	RX140
SOSCCR	SOSTP	Sub-clock oscillator stop bit	Sub-clock oscillator stop bit This bit is not initialized by reset sources other than a power-on reset.
		Initial value after a reset differs.	
OSCOVFSR	PLOVF	—	PLL clock oscillation stabilization flag b2 0: PLL is stopped or not stabilized. 1: Oscillation is stable and the clock can be used as the system clock.
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait time bits b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, typ.)	Main clock oscillator wait time bits b4 b0 0 0 0 0 0: Wait time = 0 cycles (0 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) 0 1 0 0 0: Wait time = 131,072 cycles (32.768 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, typ.)
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—

Register	Bit	RX110	RX140
CKOCR	CKOSEL[2:0] (RX110) CKOSEL[3:0] (RX140)	CLKOUT output source select bits b10 b8 0 0 0: LOCO clock 0 0 1: HOCO clock 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator Settings other than the above are prohibited.	CLKOUT output source select bits b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock oscillator 0 0 1 1: Sub-clock oscillator 0 1 0 0: PLL 1 0 0 0: CTSU internal clock Settings other than the above are prohibited.
CKOCR	CKODIV[2:0]	CLKOUT output division ratio select bits b14 b12 0 0 0: No division 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 Settings other than the above are prohibited.	CLKOUT output division ratio select bits b14 b12 0 0 0: No division 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64 1 1 1: ×1/128
MOFCR	MODRV21	Main clock oscillator drive capability switch bit VCC ≥ 2.4 V 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited	Main clock oscillator drive capability switch bit 0: 1 MHz to less than 10 MHz 1: 10 MHz to 20 MHz
LOCOTRR2	—	—	Low-speed on-chip oscillator trimming register 2
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0)
SOMCR	—	—	Sub-clock oscillator mode control register

2.7 Low Power Consumption

Table 2.10 is a comparative overview of the low power consumption functions, Table 2.11 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.12 is a comparison of low power consumption registers.

Table 2.10 Comparative Overview of Low Power Consumption Functions

Item	RX110	RX140
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.11 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX110	RX140
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 3FFFh: RX110, 0000 0000h to 0000 FFFFh: RX140)	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	—	Operation possible
Deep sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 3FFFh: RX110, 0000 0000h to 0000 FFFFh: RX140)	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX110	RX140
Deep sleep mode	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	—	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Operation possible
	Low-speed on-chip oscillator	Stopped	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 3FFFh: RX110, 0000 0000h to 0000 FFFFh: RX140)	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	—	Operation possible
Snooze mode	Transition method	—	Occurrence of snooze request condition while in software standby mode
	Method of cancellation other than reset	—	Interrupt or occurrence of snooze end condition
	State after cancellation	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX110	RX140
Snooze mode	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0000 3FFFh: RX110, 0000 0000h to 0000 FFFFh: RX140)	—	Operation possible (retained)
	DTC	—	Operation possible
	Flash memory	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Operation possible
	I/O ports	—	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible

Note: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.12 Comparison of Low Power Consumption Registers

Register	Bit	RX110	RX140
MSTPCRA	MSTPA4	—	8-bit timer 3/2 (unit 1) module stop bit
	MSTPA5	—	8-bit timer 1/0 (unit 0) module stop bit
	MSTPA19	—	D/A converter module stop bit
MSTPCRB	MSTPB0	—	CAN module module stop bit
	MSTPB9	—	ELC module stop bit
	MSTPB10	—	Comparator B module stop bit
	MSTPB25	—	Serial communication interface 6 module stop bit
MSTPCRC	—	Module stop control register C	Module stop control register C
		Initial value after a reset differs.	
	MSTPC26	—	Serial communication interface 9 module stop bit
	MSTPC27	—	Serial communication interface 8 module stop bit
MSTPCRD	—	—	Module stop control register D
OPCCR	OPCM[2:0]	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than the above are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1 0 0: Middle-speed operating mode 2 Settings other than the above are prohibited.
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2

2.8 Register Write Protection Function

Table 2.13 is a comparative overview of the register write protection functions, and Table 2.14 is a comparison of register write protection function registers.

Table 2.13 Comparative Overview of Register Write Protection Functions

Item	RX110	RX140
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the clock generation circuit: HOCOWTCR	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.14 Comparison of Register Write Protection Function Registers

Register	Bit	RX110	RX140
PRCR	PRC2	Enables writing to the registers related to the clock generation circuit.	Enables writing to the registers related to the low-power timer.

2.9 Exception Handling

Table 2.15 is a comparative overview of exception handling, Table 2.16 is a comparative listing of vectors, and Table 2.17 is a comparative listing of instructions for returning from exception handling routines.

Table 2.15 Comparative Overview of Exception Handling

Item	RX110	RX140
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.16 Comparative Listing of Vectors

Item		RX110	RX140
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		—	Exception vector table (EXTB)
Floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Relocatable vector table (INTB)

Table 2.17 Comparative Listing of Instructions for Returning from Exception Handling Routines

Item		RX110	RX140
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		—	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controller

Table 2.18 is a comparative overview of the interrupt controllers, and Table 2.19 is a comparison of interrupt controller registers.

Table 2.18 Comparative Overview of Interrupt Controllers

Item		RX110 (ICUb)	RX140 (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • Digital filter function: Supported
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupts	—	An ELSR8I or ELSR18I interrupt can be generated by an ELC event.
	Interrupt priority	Specified by registers.	Specified by registers.
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	Faster interrupt handling by the CPU can be specified for a single interrupt source only.
	DTC control	The DTC can be activated by an interrupt source.	The DTC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item	RX110 (ICUb)	RX140 (ICUb)
Return from low power consumption state	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or an RTC alarm or periodic interrupt.	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or an RTC alarm or periodic interrupt.

Table 2.19 Comparison of Interrupt Controller Registers

Register	Bit	RX110 (ICUb)	RX140 (ICUb)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register n (n = 000 to 255)
DTCERn*1	—	DTC activation enable register n (n = 027 to 248)	DTC transfer request enable register n (n = 027 to 255)

Note: 1. On the RX110 Group n = 250 to 255 correspond to a reserved area.

2.11 Buses

Table 2.20 is a comparative overview of the buses, and Table 2.21 is a comparison of bus registers.

Table 2.20 Comparative Overview of Buses

Bus Type		RX110	RX140
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules • Operates in synchronization with the peripheral module clock (PCLKB, PCLKD)
	Internal peripheral bus 3	—	• Connected to peripheral modules (CTSU, RSCAN0) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 6	• Connected to ROM (P/E) • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.21 Comparison of Bus Registers

Register	Bit	RX110	RX140
BUSPRI	BPGB[1:0]	Internal peripheral bus 2 priority control bits	Internal peripheral bus 2 and 3 priority control bits

2.12 Data Transfer Controller

Table 2.22 is a comparative overview of the data transfer controllers, and Table 2.23 is a comparison of data transfer controller registers.

Table 2.22 Comparative Overview of Data Transfer Controllers

Item	RX110 (DTCa)	RX140 (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfers can be executed in response to a single transfer request (chain transfer). • Either “performed only when the transfer counter reaches 0” or “performed every time” can be selected for chain transfers.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX110 (DTCa)	RX140 (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	—	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Transfer information read skipping can be specified.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back can be skipped when the address of the transfer source or destination is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.23 Comparison of Data Transfer Controller Registers

Register	Bit	RX110 (DTCa)	RX140 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.13 I/O Ports

Table 2.24 and Table 2.25 are comparative overviews of the I/O ports, Table 2.26 is a comparison of I/O port functions, and Table 2.27 is a comparison of I/O port registers.

Table 2.24 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX110 (64-Pin)	RX140 (64-Pin)
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTE	PE0 to PE7	PE0 to PE5
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3, PH6*1, PH7*1
PORTJ	PJ6, PJ7	PJ6, PJ7

Note: 1. A product with a ROM capacity of 64 KB is not equipped with this pin.

Table 2.25 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX110 (48-Pin)	RX140 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P35	P30, P31, P35 to P37
PORT4	P40 to P42, P46	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC0 to PC7
PORTE	PE0 to PE4, PE7	PE1 to PE4
PORTG	—	PG7
PORTH	PH0 to PH3	PH0 to PH3
PORTJ	PJ6, PJ7	PJ6, PJ7

Table 2.26 Comparison of I/O Port Functions

Item	Port Symbol	RX110	RX140
Input pull-up function	PORT0	P03, P05	P03 to P07
	PORT1	P14, P15, P16, P17	P12 to P17
	PORT2	P26, P27	P20, P21, P26, P27
	PORT3	P30 to P32	P30 to P32, P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	P54, P55	P54, P55
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0 to PA6
	PORTB	PB0, PB1, PB3, PB5 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC2 to PC7
	PORTD	—	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE3, PE4, PE5
	PORTG	—	PG7
	PORTH	PH0 to PH3	PH0 to PH3
	PORTJ	—	PJ1, PJ6, PJ7
Open drain output function	PORT1	P14 to P17	P12 to P17
	PORT2	P26, P27	P20, P21, P26, P27
	PORT3	P30 to P32	P30 to P32, P34, P36, P37
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0 to PA6
	PORTB	PB0, PB1, PB3, PB5 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC2 to PC7
	PORTD	—	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE3
	PORTG	—	PG7
5 V tolerant	PORT1	P16, P17	P12, P13, P16, P17
	PORTA	PA6	—
	PORTB	PB0	—

Table 2.27 Comparison of I/O Port Registers

Register	Bit	RX110	RX140
PDR	B0 to B7	Pm0 to Pm7 direction control bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 direction control bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 5, A to C, E, H, J) 0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral function.	Pm0 pin mode control bits (m = 0 to 5, A to E, G, H, J) 0: Use pin as general I/O port. 1: Use pin as I/O port for peripheral function. PG7 only 0: Use pin as general I/O port. 1: Use pin as I/O port for MD function (initial value).

Register	Bit	RX110	RX140
ODR0	B0, B4, B6	Pm0, Pm2, and Pm3 output type select bits (m = 3, A to C, E)	Pm0, Pm2, and Pm3 output type select bits (m =1 to 3, A to E, J)
	B2, B3	Pm1 output type select bits (m = 3, A to C, E) • P31, PA1, PB1, and PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Setting prohibited	Pm1 output type select bits (m =1 to 3, A to E, J) • P21, P31, PA1, PB1, and PD1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z
ODR1	B0, B1 (RX110) B0 (RX140)	Pm4 output type select bits (m = 1, 2, A to C, E) • PA4, PC4, and PE4 b0 0: CMOS output 1: N-channel open-drain b1 This bit is read as 0. The write value should be 0. • P14 b1 b0 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Setting prohibited	Pm4 output type select bits (m = 1 to 3, A to C, G) b0 0: CMOS output 1: N-channel open-drain
	B2, B4, B6	Pm5, Pm6, and Pm7 output type select bits (m = 1, 2, A to C, E)	Pm5, Pm6, and Pm7 output type select bits (m =1 to 3, A to C, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 3, 5, A to C, E, H)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
PRWCNTR	—	—	Port read wait control register

2.14 Multi-Function Pin Controller

Table 2.28 is a comparison of the assignments of multiplexed pins, and Table 2.29 to Table 2.41 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **blue text** designates pins that exist on the RX140 Group only and **orange text** pins that exist on the RX110 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.28 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○
	IRQ0 (input)	P30	○	×	○	○
		PE0	○	○	×	×
		PH1	○	○	○	○
	IRQ1 (input)	P31	○	×	○	○
		PE1	○	○	×	×
		PH2	○	○	○	○
	IRQ2 (input)	P32	○	×	○	×
		PB0	○	○	×	×
		PC4	○	○	×	×
		P36	×	×	○	○
	IRQ3 (input)	P27	○	○	×	×
		PE3	○	○	×	×
		PA6	○	○	×	×
	IRQ4 (input)	P14	○	○	○	○
		PB1	○	○	○	○
		PE4	○	○	×	×
		P37	×	×	○	○
	IRQ5 (input)	P15	○	○	○	○
		PA4	○	○	○	○
		PE5	○	×	○	×
	IRQ6 (input)	P16	○	○	○	○
		PA3	○	○	○	○
		PE6	○	×	×	×
	IRQ7 (input)	P17	○	○	○	○
		PE2	○	○	○	○
		PE7	○	○	×	×
Multi-function timer unit 2	MTIOC0A (input/output)	P14	○	○	×	×
		PB3	○	○	○	○
		PE3	○	○	×	×
		PC4	×	×	○	○
	MTIOC0B (input/output)	P15	○	○	○	○
		PA1	○	○	○	○
	MTIOC0C (input/output)	P17	○	○	×	×
		P32	○	×	○	×
		PB0	○	○	×	×
		PB1	○	○	○	○
		PC5	×	×	○	○
	MTIOC0D (input/output)	PA3	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC1A (input/output)	PE4	○	○	○	○
		PH3	○	○	×	×
	MTIOC1B (input/output)	PA3	○	○	×	×
		PB5	○	○	○	○
		PE3	○	○	○	○
		PH0	○	○	×	×
	MTIOC2A (input/output)	P26	○	○	○	○
		PA6	○	○	×	×
		PB5	○	○	○	○
		PE0	○	○	×	×
	MTIOC2B (input/output)	P27	○	○	○	○
		PA4	○	○	×	×
		PE5	○	×	○	×
	MTIOC3A (input/output)	P14			○	○
		P17			○	○
		PC7			○	○
	MTIOC3B (input/output)	P17			○	○
		PA1			○	○
		PB7			○	×
		PC5			○	○
		PH0			○	○
	MTIOC3C (input/output)	P16			○	○
		PC6			○	○
	MTIOC3D (input/output)	P16			○	○
		PA6			○	○
		PB0			○	○
		PB6			○	×
		PC4			○	○
		PH1			○	○
	MTIOC4A (input/output)	P55			○	×
		PA0			○	×
		PB3			○	○
		PE2			○	○
		PE4			○	○
	MTIOC4B (input/output)	P30			○	○
		P54			○	×
		PC2			○	×
		PE3			○	○
	MTIOC4C (input/output)	PA4			○	○
		PB1			○	○
		PE1			○	○
		PE5			○	×
		PH2			○	○
	MTIOC4D (input/output)	P31			○	○
		P55			○	×
		PA3			○	○
		PC3			○	×
		PE4			○	○
		PH3			○	○
	MTIC5U (input)	PA4	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIC5V (input)	PA6	○	○	○	○
		PA3	×	×	○	○
	MTIC5W (input)	PB0	○	○	○	○
	MTCLKA (input)	P14	○	○	○	○
		PA4	○	○	○	○
		PC6	○	○	○	○
	MTCLKB (input)	P15	○	○	○	○
		PA6	○	○	○	○
		PC7	○	○	○	○
	MTCLKC (input)	PA1	○	○	○	○
		PC4	○	○	○	○
	MTCLKD (input)	PA3	○	○	○	○
		PC5	○	○	○	○
Serial communications interface	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○	○
		P30	○	×	○	○
		PC6	○	○	×	×
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○	○
		P26	○	○	○	○
		PC7	○	○	×	×
	SCK1 (input/output)	P17	○	○	○	○
		P27	○	○	○	○
		PC5	○	○	×	×
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○	○
		P31	○	×	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA3	○	○	○	○
		PC2	○	×	○	×
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	○	○	○
		PC3	○	×	○	×
	SCK5 (input/output)	PA1	○	○	○	○
		PC4	○	○	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	○	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	PB0			○*1	○*1
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P32			○*1	×
		PB1			○*1	○*1
	SCK6 (input/output)	PB3			○*1	○*1

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Serial communications interface	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6			○*1	○*1
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7			○*1	○*1
	SCK8 (input/output)	PC5			○*1	○*1
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4			○*1	○*1
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6			○*1	×
	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7			○*1	×
	SCK9 (input/output)	PB5			○*1	×
	CTS9# (input) / RTS9# (output) / SS9# (input)	PB4			○*1	×
	SCK12 (input/output)	PE0	○	○	○	×
		P27	○	○	×	×
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○	○	○	○*3
		P17	○	○	×	×
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○	○	○	○*4
		P14	○	○	×	×
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○	○	○	○*5
I²C bus interface	SCL0 (input/output)	P16	○	○	○	○
		PB0	○	○	×	×
	SDA0 (input/output)	P17	○	○	○	○
		PA6	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Serial peripheral interface	RSPCKA (input/output)	P15	○	○	×	×
		PB0	○	○	○	○
		PC5	○	○	○	○
		PE3	○	○	×	×
	MOSIA (input/output)	P16	○	○	○	○
		PA6	○	○	○	○
		PE4	○	○	×	×
		PC6	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○
		PC7	○	○	○	○
		PA3	○	○	×	×
	SSLA0 (input/output)	P14	○	○	×	×
		PA4	○	○	○	○
		PC4	○	○	○	○
	SSLA1 (output)	PA0	○	×	○	×
	SSLA2 (output)	PA1	○	○	○	○
	SSLA3 (output)	PC2	○	×	○	×
Realtime clock	RTCOUT (output)	P16	○	○	○	○
		P32	○	×	○	×
		PB0	○	○	×	×
		PA1	○	○	×	×
12-bit A/D converter	AN000 (input)*2	P40	○	○	○	○
	AN001 (input)*2	P41	○	○	○	○
	AN002 (input)*2	P42	○	○	○	○
	AN003 (input)*2	P43	○	×	○	×
	AN004 (input)*2	P44	○	×	○	×
	AN005 (input)*2	P45			○	○
	AN006 (input)*2	P46	○	○	○	○
	AN007 (input)*2	P47			○	○
	AN008 (input)*2	PE0	○	○		
	AN009 (input)*2	PE1	○	○		
	AN010 (input)*2	PE2	○	○		
	AN011 (input)*2	PE3	○	○		
	AN012 (input)*2	PE4	○	○		
	AN013 (input)*2	PE5	○	×		
	AN014 (input)*2	PE6	○	×		
	AN015 (input)*2	PE7	○	○		
	AN016 (input)*2	PE0			○	×
	AN017 (input)*2	PE1			○	○
	AN018 (input)*2	PE2			○	○
	AN019 (input)*2	PE3			○	○
	AN020 (input)*2	PE4			○	○
	AN021 (input)*2	PE5			○	×
	VREFH0 (input)	PJ6	○	○		
	VREFL0 (input)	PJ7	○	○		
	ADTRG0# (input)	P16	○	○	○	○
		P27	○	○	×	×
		PB0	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Clock generation circuit	CLKOUT (output)	P15	○	○	×	×
		PC4	○	○	×	×
		PE3	×	×	○	○
		PE4	×	×	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	P27	○	○	×	×
		PA0	○	×	○	×
		PC7	○	○	○	○
		PH0	○	○	○	○
Voltage detection circuit	CMPA2 (input)*2	P27	○	○	×	×
		PE4	×	×	○	○
Port output enable 2	POE0# (input)	PC4			○	○
	POE1# (input)	PB5			○	○
	POE2# (input)	PA6			○	○
	POE3# (input)	PB3			○	○
	POE8# (input)	P17			○	○
		P30			○	○
		PE3			○	○
8-bit timer	TMO0 (output)	PB3			○	○
		PH1			○	○
	TMCI0 (input)	PB1			○	○
		PH3			○	○
	TMRI0 (input)	PA4			○	○
		PH2			○	○
	TMO1 (output)	P17			○	○
		P26			○	○
	TMCI1 (input)	P54			○	×
		PC4			○	○
	TMRI1 (input)	PB5			○	○
	TMO2 (output)	P16			○	○
		PC7			○	○
	TMCI2 (input)	P15			○	○
		P31			○	○
		PC6			○	○
	TMRI2 (input)	P14			○	○
		PC5			○	○
	TMO3 (output)	P32			○	×
		P55			○	×
	TMCI3 (input)	P27			○	○
		PA6			○	○
	TMRI3 (input)	P30			○	○
Low-power timer	LPTO (output)	P26			○	○
		PB3			○	○
		PC7			○	○
CAN module	CTXD0 (output)	P14			○*1	○*1
		P54			○*1	×
	CRXD0 (input)	P15			○*1	○*1
		P55			○*1	×
D/A converter	DA0 (output)*2	P03			○	×
	DA1 (output)*2	P05			○	×

Module/ Function	Pin Function	Port Allocation	RX110		RX140	
			64-Pin	48-Pin	64-Pin	48-Pin
Comparator B	CMPB0 (input)*2	PE1			○	○
	CVREFB0 (input)*2	PE2			○	○
	CMPOB0 (output)	PE5			○	×
	CMPB1 (input)*2	PA3			○	○
	CVREFB1 (input)*2	PA4			○	○
	CMPOB1 (output)	PB1			○	○
Capacitive touch sensing unit	TS0 (input/output)	P32			○*1	×
	TS1 (input/output)	P31			○*1	○*1
	TS2 (input/output)	P30			○*1	○*1
	TS3 (input/output)	P27			○	○
	TS4 (input/output)	P26			○	○
	TS5 (input/output)	P15			○*1	○*1
	TS6 (input/output)	P14			○*1	○*1
	TS7 (input/output)	PH3			○*1	○*1
	TS8 (input/output)	PH2			○*1	○*1
	TS9 (input/output)	PH1			○*1	○*1
	TS10 (input/output)	PH0			○*1	○*1
	TS11 (input/output)	P55			○*1	×
	TS12 (input/output)	P54			○*1	×
	TS13 (input/output)	PC7			○	○
	TS14 (input/output)	PC6			○	○
	TS15 (input/output)	PC5			○	○
	TS16 (input/output)	PC3			○*1	×
	TS17 (input/output)	PC2			○*1	×
	TS18 (input/output)	PB7			○*1	×
	TS19 (input/output)	PB6			○*1	×
	TS20 (input/output)	PB5			○*1	○*1
	TS22 (input/output)	PB3			○*1	○*1
	TS24 (input/output)	PB1			○*1	○*1
	TS25 (input/output)	PB0			○	○
	TS26 (input/output)	PA6			○*1	○
	TS28 (input/output)	PA4			○	○
	TS29 (input/output)	PA3			○	○
	TS31 (input/output)	PA1			○	○
	TS32 (input/output)	PA0			○*1	×
	TS33 (input/output)	PE4			○	○
	TS34 (input/output)	PE3			○	○
	TS35 (input/output)	PE2			○	○
	TSCAP (—)	PC4			○	○

Notes: 1. This function is not implemented on RX140 Group products with ROM capacity of 64 KB.
2. To use these pin functions, set the relevant pins as general I/O ports (PORT.PDR.Bm and PORT.PMR.Bm bits both cleared to 0).
3. The SMISO12 function is not implemented on 48-pin package products.
4. The SMOSI12 function is not implemented on 48-pin package products.
5. The SS12# function is not implemented on 48-pin package products.

Table 2.29 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX110	RX140 (n = 3, 5, 7)
P0nPFS	—	—	P0n pin function control register

Table 2.30 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX110 (n = 4 to 7)	RX140 (n = 2 to 7)
P12PFS	—	—	P12 pin function control register
P13PFS	—	—	P13 pin function control register
P14PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTCLKA 00011b: MTIOC0A 01011b: CTS1#/RTS1#/SS1# 01100b: TXD12/SMOSI12/SSDA12/ TXD12/SIOX12 01101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 11001b: TS6 11100b: CTXD0
P15PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 01001b: CLKOUT 01010b: RXD1/SMISO1/SSCL1 01101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 11001b: TS5 11100b: CRXD0
P16PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL

Register	Bit	RX110 (n = 4 to 7)	RX140 (n = 2 to 7)
P17PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00011b: MTIOC0C 01010b: SCK1 01100b: RXD12/SMISO12/ SSCL12/RXDX12 01101b: MISOA 01111b: SDA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00101b: TMO1 00111b: POE8# 01010b: SCK1 01101b: MISOA 01111b: SDA0
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P14: IRQ4 (64/48/40/36-pin) P15: IRQ5 (64/48/40/36-pin) P16: IRQ6 (64/48/40/36-pin) P17: IRQ7 (64/48/40/36-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (80-pin) P13: IRQ3 (80-pin) P14: IRQ4 (80/64/48-pin) P15: IRQ5 (80/64/48-pin) P16: IRQ6 (80/64/48/32-pin) P17: IRQ7 (80/64/48/32-pin)

Table 2.31 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX110 (n = 6, 7)	RX140 (n = 0, 1, 6, 7)
P20PFS	—	—	P20 pin function control register
P21PFS	—	—	P21 pin function control register
P26PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 01010b: TXD1/SMOSI1/SSDA1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 11001b: TS4 11011b: LPTO
P27PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00111b: CACREF 01001b: ADTRG0# 01010b: SCK1 01100b: SCK12	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 01010b: SCK1 11001b: TS3
P2nPFS	ISEL	Interrupt input function select bit	—
	ASEL	Analog function select bit	—

Table 2.32 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX110 (n = 0 to 2)	RX140 (n = 0 to 2, 4, 6, 7)
P30PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: RXD1/SMISO1/SSCL1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 11001b: TS2
P31PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01011b: CTS#1/RTS#1/SS1#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 01011b: CTS#1/RTS#1/SS1# 11001b: TS1
P32PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00111b: RTCOUT	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 11001b: TS0
P34PFS	—	—	P34 pin function control register
P36PFS	—	—	P36 pin function control register
P37PFS	—	—	P37 pin function control register
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (64-pin) P31: IRQ1 (64-pin) P32: IRQ2 (64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (80/64/48/32-pin) P31: IRQ1 (80/64/48/32-pin) P32: IRQ2 (80/64-pin) P34: IRQ4 (80-pin) P36: IRQ2 (80/64/48/32-pin) P37: IRQ4 (80/64/48-pin)

Table 2.33 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX110 (n = 0 to 4, 6)	RX140 (n = 0 to 7)
P4nPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (64/48-pin) P41: AN001 (64/48/40/36-pin) P42: AN002 (64/48/40/36-pin) P43: AN003 (64-pin) P44: AN004 (64-pin) P46: AN006 (64/48/40-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (80/64/48/32-pin) P41: AN001 (80/64/48/32-pin) P42: AN002 (80/64/48/32-pin) P43: AN003 (80/64-pin) P44: AN004 (80/64-pin) P45: AN005 (80/64/48-pin) P46: AN006 (80/64/48-pin) P47: AN007 (80/64/48-pin)

Table 2.34 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX110	RX140 (n = 4, 5)
P5nPFS	—	—	P5n pin function control register

Table 2.35 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX110 (n = 0, 1, 3, 4, 6)	RX140 (n = 0 to 6)
PA0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: CACREF 01101b: SSLA1	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00111b: CACREF 01101b: SSLA1 11001b: TS32
PA1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00111b: RTCOUT 01010b: SCK5 01101b: SSLA2	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: MTIOC3B 01010b: SCK5 01101b: SSLA2 11001b: TS31
PA2PFS	—	—	PA2 pin function control register
PA3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: MTIOC1B 01010b: RXD5/SMISO5/SSCL5 01101b: MISOA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: MTIOC4D 00100b: MTIC5V 01010b: RXD5/SMISO5/SSCL5 11001b: TS29

Register	Bit	RX110 (n = 0, 1, 3, 4, 6)	RX140 (n = 0 to 6)
PA4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: MTIOC2B 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: MTIOC4C 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 11001b: TS28
PA5PFS	—	—	PA5 pin function control register
PA6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: MTIOC2A 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 01111b: SDA0	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: MTIOC3D 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 11001b: TS26
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 (64/48/40/36-pin) PA4: IRQ5 (64/48/40/36-pin) PA6: IRQ3 (64/48/40/36-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 (80/64/48/32-pin) PA4: IRQ5 (80/64/48/32-pin)
	ASEL	—	Analog function select bit

Table 2.36 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX110 (n = 0, 1, 3, 5 to 7)	RX140 (n = 0 to 7)
PB0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00010b: MTIOC0C 00111b: RTCOUT 01001b: ADTRG0# 01101b: RSPCKA 01111b: SCL0	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00010b: MTIOC3D 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25

Register	Bit	RX110 (n = 0, 1, 3, 5 to 7)	RX140 (n = 0 to 7)
PB1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11001b: TS24
PB2PFS	—	—	PB2 pin function control register
PB3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22 11011b: LPTO
PB4PFS	—	—	PB4 pin function control register
PB5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 00111b: POE1# 01010b: SCK9 11001b: TS20
PB6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 01010b: RXD9/SMISO9/SSCL9 11001b: TS19
PB7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 01010b: TXD9/SMOSI9/SSDA9 11001b: TS18
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ2 (64/48/40/36-pin) PB1: IRQ4 (64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (80/64/48-pin)

Table 2.37 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX110 (n = 2 to 7)	RX140 (n = 2 to 7)
PC2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS17
PC3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 01010b: TXD5/SMOSI5/SSDA5 11001b: TS16
PC4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTCLKC 01001b: CLKOUT 01010b: SCK5 01101b: SSLA0	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00011b: MTIOC0A 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP
PC5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTCLKD 01011b: SCK1 01101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00011b: MTIOC0C 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS15
PC6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTCLKA 01011b: RXD1/SMISO1/SSCL1 01101b: MOSIA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 11001b: TS14

Register	Bit	RX110 (n = 2 to 7)	RX140 (n = 2 to 7)
PC7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTCLKB 00111b: CACREF 01011b: TXD1/SMOSI1/SSDA1 01101b: MISOA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA 11001b: TS13 11011b: LPTO
PCnPFS	ISEL	Interrupt input function select bit	—

Table 2.38 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX110	RX140 (n = 0 to 2)
PDnPFS	—	—	PDn pin function control register

Table 2.39 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX110 (n = 0 to 7)	RX140 (n = 0 to 5)
PE0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTIOC2A 01100b: SCK12	Pin function select bits 00000b: Hi-Z 01100b: SCK12
PE1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 01100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12
PE2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01100b: RXD12/SMISO12/ SSCL12/RXDX12	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 01100b: RXD12/SMISO12/ SSCL12/RXDX12 11001b: TS35
PE3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC0A 01100b: CTS12#/RTS12#/SS12# 01101b: RSPCKA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00010b: MTIOC1B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 11001b: TS34

Register	Bit	RX110 (n = 0 to 7)	RX140 (n = 0 to 5)
PE4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTIOC1A 01101b: MOSIA	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00011b: MTIOC4A 01001b: CLKOUT 11001b: TS33
PE5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00010b: MTIOC2B	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 10000b: CMPOB0
PE6PFS	—	PE6 pin function control register	—
PE7PFS	—	PE7 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ0 (64/48/40/36-pin) PE1: IRQ1 (64/48/40/36-pin) PE2: IRQ7 (64/48/40/36-pin) PE3: IRQ3 (64/48/40/36-pin) PE4: IRQ4 (64/48/40/36-pin) PE5: IRQ5 (64-pin) PE6: IRQ6 (64-pin) PE7: IRQ7 (64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (80/64/48/32-pin) PE5: IRQ5 (80/64-pin)
	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (64/48/40/36-pin) PE1: AN009 (64/48/40/36-pin) PE2: AN010 (64/48/40/36-pin) PE3: AN011 (64/48/40/36-pin) PE4: AN012 (64/48/40/36-pin) PE5: AN013 (64-pin) PE6: AN014 (64-pin) PE7: AN015 (64/48-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN016 (80/64-pin) PE1: AN017, CMPB0 (80/64/48/32-pin) PE2: AN018, CVREFB0 (80/64/48/32-pin) PE3: AN019 (80/64/48/32-pin) PE4: AN020, CMPA2 (80/64/48/32-pin) PE5: AN021 (80/64-pin)

Table 2.40 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX110 (n = 0 to 3)	RX140 (n = 0 to 3)
PH0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00111b: CACREF	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00111b: CACREF 11001b: TS10
PH1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00101b: TMO0 11001b: TS9
PH2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00101b: TMRI0 11001b: TS8
PH3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI0 11001b: TS7

Table 2.41 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX110 (n = 6, 7)	RX140 (n = 1, 6, 7)
PJ1PFS	—	—	PJ1 pin function control register
PJ6PFS	ASEL	Analog function select bit 0: The AVCC0 pin is selected as the reference power supply pin for the high-potential side. 1: The VREFH0 pin is selected as the reference power supply pin for the high-potential side.	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PJ6: VREFH0 (80/64/48-pin)
PJ7PFS	ASEL	Analog function select bit 0: The AVSS0 pin is selected as the reference power supply ground pin for the low-potential side. 1: The VREFL0 pin is selected as the reference power supply ground pin for the low-potential side.	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PJ7: VREFL0 (80/64/48-pin)

2.15 Multi-Function Timer Pulse Unit 2

Table 2.42 is a comparative overview of multi-function timer pulse unit 2, and Table 2.43 is a comparison of multi-function timer pulse unit 2 registers.

Table 2.42 Comparative Overview of Multi-Function Timer Pulse Unit 2

Item	RX110 (MTU2b)	RX140 (MTU2a)
Pulse input/output	Max. 8 lines	Max. 16 lines
Pulse input	3 lines	3 lines
Count clocks	Eight or Seven clocks for each channel (four clocks for MTU5)	Eight or Seven clocks for each channel (four clocks for MTU5)
Available operations	[MTU0 to MTU2] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 8-phase PWM output in combination with synchronous operation [MTU0] • Ability to specify buffer operation [MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation [MTU5] • Input capture function (noise filter setting) • Counter clear operation	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation [MMTU0, MTU3, MTU4] • Ability to specify buffer operation • Ability to specify AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset-synchronized PWM and to select between two types of waveform output (chopping or level) [MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation [MTU3, MTU4] • Ability to output three positive and three negative phases (total six phases) using continuous operation of complementary PWM or reset-synchronized PWM [MTU5] • Counter function for dead time compensation • Input capture function (noise filter setting) • Counter clear operation

Item	RX110 (MTU2b)	RX140 (MTU2a)
Complementary PWM mode	—	• Interrupts at peaks or troughs of counter • A/D converter conversion start trigger skipping function
Interrupt sources	18 sources	28 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data
Trigger generation	Ability to generate A/D converter start trigger	Ability to generate A/D converter start trigger
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.43 Comparison of Multi-Function Timer Pulse Unit 2 Registers

Register	Bit	RX110 (MTU2b)	RX140 (MTU2a)
TMDR	MD[3:0]	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 x x x: Setting prohibited	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Setting prohibited 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at peak) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at peak and trough)

Register	Bit	RX110 (MTU2b)	RX140 (MTU2a)
TIORU TIORV TIORW	IOC[4:0]	I/O control C bits b4 b0 0 0 0 0 0: Compare match 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Setting prohibited 1 1 0 0 0: Setting prohibited 1 1 0 0 1: Measurement of low pulse width of external input signal 1 1 0 1 0: Measurement of low pulse width of external input signal 1 1 0 1 1: Measurement of low pulse width of external input signal 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Measurement of high pulse width of external input signal 1 1 1 1 0: Measurement of high pulse width of external input signal 1 1 1 1 1: Measurement of high pulse width of external input signal	I/O control C bits b4 b0 0 0 0 0 0: No function 0 0 0 0 1: Setting prohibited 0 0 0 1 x: Setting prohibited 0 0 1 x x: Setting prohibited 0 1 x x x: Setting prohibited 1 0 0 0 0: Setting prohibited 1 0 0 0 1: Input capture at rising edge 1 0 0 1 0: Input capture at falling edge 1 0 0 1 1: Input capture at both edges 1 0 1 x x: Setting prohibited 1 1 0 0 0: Setting prohibited 1 1 0 0 1: Measurement of low pulse width of external input signal Capture at trough in complementary PWM mode 1 1 0 1 0: Measurement of low pulse width of external input signal Capture at peak in complementary PWM mode 1 1 0 1 1: Measurement of low pulse width of external input signal Capture at peak and trough in complementary PWM mode 1 1 1 0 0: Setting prohibited 1 1 1 0 1: Measurement of high pulse width of external input signal Capture at trough in complementary PWM mode 1 1 1 1 0: Measurement of high pulse width of external input signal Capture at peak in complementary PWM mode 1 1 1 1 1: Measurement of high pulse width of external input signal Capture at peak and trough in complementary PWM mode
TIER	TTGE2	—	A/D converter start request enable 2 bit
TADCR	—	—	Timer A/D converter start request control register
TADCORA TADCORB	—	—	Timer A/D converter start request cycle set registers A and B
TADCOBRA TADCOBRB	—	—	Timer A/D converter start request cycle set buffer registers A and B
TSTR	CTS3	—	Counter start 3 bit
	CTS4	—	Counter start 4 bit
TSYR	SYNC3	—	Timer synchronous operation 3 bit
	SYNC4	—	Timer synchronous operation 4 bit
TRWER	—	—	Timer read/write enable register

Register	Bit	RX110 (MTU2b)	RX140 (MTU2a)
TOER	—	—	Timer output master enable register
TOCR1	—	—	Timer output control register 1
TOCR2	—	—	Timer output control register 2
TOLBR	—	—	Timer output level buffer register
TGCR	—	—	Timer gate control register
TCNTS	—	—	Timer subcounter
TDDR	—	—	Timer dead time data register
TCDR	—	—	Timer cycle data register
TCBR	—	—	Timer cycle buffer register
TITCR	—	—	Timer interrupt skipping set register
TITCNT	—	—	Timer interrupt skipping counter
TBTER	—	—	Timer buffer transfer set register
TDER	—	—	Timer dead time enable register
TWCR	—	—	Timer waveform control register

2.16 Compare Match Timer

Table 2.44 is a comparative overview of the compare match timers.

Table 2.44 Comparative Overview of Compare Match Timers

Item	RX110	RX140
Count clocks	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

2.17 Realtime Clock

Table 2.45 is a comparison of realtime clock registers.

Table 2.45 Comparison of Realtime Clock Registers

Register	Bit	RX110 (RTCA)	RX140 (RTCc)
RCR3	—	RTC control register 3	—

2.18 Serial Communications Interface

Table 2.46 is a comparative overview of the serial communications interfaces, and Table 2.47 is a comparison of serial communications interface channel specifications, and Table 2.48 is a comparison of serial communications interface registers.

Table 2.46 Comparative Overview of Serial Communications Interfaces

Item		RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
Number of channels		• SCIe: 2 channels • SCIf: 1 channel	• SCIg: 3 channels • SCIk: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently (SCI1 and SCI5).
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, and data match (SCI1 and SCI5), completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
Asynchronous mode	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they are matched (SCI1 and SCI5)
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point (SCI1 and SCI5).
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed (SCI1 and SCI5).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag (SCI1 or SCI5).
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI1, SCI5, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.

Item		RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
Simple I²C mode	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		—	Correction of outputs from the on-chip baud rate generator can reduce errors.

Item	RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
Event link function (supported by SCI5 only)	—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.47 Comparison of Serial Communications Interface Channel Specifications

Item	RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
Synchronous mode	SCI1, SCI5, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Clock synchronous mode	SCI1, SCI5, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Smart card interface mode	SCI1, SCI5, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple I²C mode	SCI1, SCI5, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Simple SPI mode	SCI1, SCI5, SCI12	SCI1, SCI5, SCI6, SCI8, SCI9, SCI12
Data match detection	—	SCI1, SCI5
Extended serial mode	SCI12	SCI12
MTU clock input (RX110) TMR clock input (RX140)	SCI1, SCI5, SCI12	SCI5, SCI6, SCI12
Event link function	—	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5, SCI12	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9, SCI12

Table 2.48 Comparison of Serial Communications Interface Registers

Register	Bit	RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
RDRH RDRL RDRHL	—	—	Receive data registers H, L, and HL
TDRH TDRL TDRHL	—	—	Transmit data registers H, L, and HL
SMR	CHR	Character length bit (Valid only in asynchronous mode) 0: Selects 8 bits as the data length for transmission and reception 1: Selects 7 bits as the data length for transmission and reception	Character length bit (Valid only in asynchronous mode) Selections are made in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Selects 9 bits as the data length for transmission and reception 0 1: Selects 9 bits as the data length for transmission and reception 1 0: Selects 8 bits as the data length for transmission and reception (initial value) 1 1: Selects 7 bits as the data length for transmission and reception

Register	Bit	RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
SCR (when SCMR.SMIF = 0)	CKE[1:0]	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin can be used as an I/O port by means of an I/O port setting. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or MTU clock • When using an external clock, input a clock with a frequency 16 times the bit rate on the SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency eight times the bit rate. • The MTU clock can be used. When using the MTU clock, the SCKn pin can be used as an I/O port by means of an I/O port setting. (Clock synchronous mode) b1 b0 0 x: Internal clock: The SCKn pin functions as the clock output pin. 1 x: External clock: The SCKn pin functions as the clock input pin.	Clock enable bits (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is in the high-impedance state. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock*1 • When using an external clock, input a clock with a frequency 16 times the bit rate on the SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency eight times the bit rate. • When using the TMR clock, the SCKn pin is in the high-impedance state. (Clock synchronous mode) b1 b0 0 x: Internal clock: The SCKn pin functions as the clock output pin. 1 x: External clock: The SCKn pin functions as the clock input pin.
	MPIE	Multi-processor interrupt enable bit (Valid in asynchronous mode when SMR.MP bit = 1) 0: Normal receive operation 1: When data is received while the multi-processor bit is set to 0, the data is skipped, and setting (to 1) of status flags ORER, and FER in SSR is disabled. When data is received while the multi-processor bit is set to 1, the MPIE bit is automatically cleared to 0, and normal receive operation resumes.	Multi-processor interrupt enable bit (Valid in asynchronous mode when SMR.MP bit = 1) 0: Normal receive operation 1: When data is received while the multi-processor bit is set to 0, the data is skipped, and setting (to 1) of status flags RDRF, ORER, and FER in SSR is disabled. When data is received while the multi-processor bit is set to 1, the MPIE bit is automatically cleared to 0, and normal receive operation resumes.

Register	Bit	RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
SCR (when SCMR.SMIF = 1)	CKE[1:0]	Clock enable bits (When the SMR.GM bit = 0) b1 b0 0 0: Output disabled (The SCKn pin can be used as an I/O port by means of an I/O port setting.) 0 1: Clock output 1 x: (Setting prohibited) (When the SMR.GM bit = 1) b1 b0 0 0: Low-level output fixed x 1: Clock output 1 0: High-level output fixed	Clock enable bits (When the SMR.GM bit = 0) b1 b0 0 0: Output disabled The SCKn pin is in the high-impedance state. 0 1: Clock output 1 x: Setting prohibited (When the SMR.GM bit = 1) b1 b0 0 0: Low-level output fixed x 1: Clock output 1 0: High-level output fixed
SCMR	CHR1	—	Character length bit
MDDR	—	—	Modulation duty register
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock 1: Logical AND of two compare matches output from MTU	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) The compare match outputs that can be used differ according to the SCI channel.
	ITE	—	Immediate transmission enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Asynchronous basic clock select extended bit
	BGDM	—	Baud rate generator double-speed mode select bit
SPMR	MSS	Master slave select bit 0: TXDn pin: transmission, RXDn pin: reception (master mode) 1: TXDn pin: reception, RXDn pin: transmission (slave mode)	Master slave select bit 0: SMOSIn pin: transmission, SMISOn pin: reception (master mode) 1: SMOSIn pin: reception, SMISOn pin: transmission (slave mode)
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

Register	Bit	RX110 (SCIe, SCIf)	RX140 (SCIg, SCIk, SCIh)
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Setting prohibited	Bus collision detection clock select bits (When the SEMR.BGDM bit is cleared to 0 or the SEMR.BGDM bit is set to 1 and the SMR.CKS[1:0] bits are set to a value other than 00b) b5 b4 0 0: Base clock 0 1: Base clock frequency divided by 2 1 0: Base clock frequency divided by 4 1 1: Setting prohibited (When the SEMR.BGDM bit is set to 1 and the SMR.CKS[1:0] bits are set to 00b) b5 b4 0 0: Base clock frequency divided by 2 0 1: Base clock frequency divided by 4 1 0: Setting prohibited 1 1: Setting prohibited

Note: 1. Selectable on SCI5, SCI6, and SCI12 only.

2.19 I²C bus Interface

Table 2.49 is a comparative overview of the I²C bus interfaces, and Table 2.50 is a comparison of I²C bus interface registers.

Table 2.49 Comparative Overview of I²C Bus Interfaces

Item	RX110 (RIIC)	RX140 (RIICa)
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Fast mode is supported (up to 400 kbps).	Fast mode is supported (up to 400 kbps).
Serial clock (SCL)	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	• Start, restart, and stop conditions are generated automatically. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are generated automatically. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles	For reception, the following wait periods can be obtained by holding the SCL line at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX110 (RIIC)	RX140 (RIICa)
Arbitration	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events (detection of arbitration, NACK, time out, a start condition including a restart condition, or a stop condition) • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission complete	Four sources: • Error in transfer or occurrence of events (detection of arbitration loss, NACK, timeout, a start condition including a restart condition, or a stop condition) • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX110 (RIIC)	RX140 (RIICa)
Event link function (output)	—	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration loss, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Table 2.50 Comparison of I²C Bus Interface Registers

Register	Bit	RX110 (RIIC)	RX140 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNTL TMOCNTU	—	Timeout internal counter	—

2.20 Serial Peripheral Interface

Table 2.51 is a comparative overview of serial peripheral interfaces, and Table 2.52 is a comparison of serial peripheral interface registers.

Table 2.51 Comparative Overview of Serial Peripheral Interfaces

Item	RX110 (RSPI)	RX140 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection

Item	RX110 (RSPI)	RX140 (RSPIc)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range:1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state.	Ability to specify module stop state.

Table 2.52 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX110 (RSPIa)	RX140 (RSPIc)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode fault error flag 0: Neither a mode fault error nor an underrun error occurs 1: A mode fault error or an underrun error occurs
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Accessible size • Longwords access (SPDCR.SPLW = 1) • Words access (SPDCR.SPLW = 0)	RSPI data register Accessible size • Longwords access (SPDCR.SPLW = 1, SPBYTE = 0) • Words access (SPDCR.SPLW = 0, SPBYTE = 0) • Bytes access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed (when SPCR.TXMD = 0). A parity bit is added to transmit data, but no parity checking of receive data is performed (when SPCR.TXMD = 1).	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed.
	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2

2.21 12-Bit A/D Converter

Table 2.53 is a comparative overview of the 12-bit A/D converters, and Table 2.54 is a comparison of 12-bit A/D converter registers, and Table 2.55 is a comparison of A/D conversion start triggers that can be set in the ADSTRGR registers.

Table 2.53 Comparative Overview of 12-Bit A/D Converters

Item	RX110 (S12ADb)	RX140 (S12ADE)
Number of units	1 unit	1 unit
Input channels	14 channels	18 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when A/D conversion clock ADCLK = 32 MHz)	Per channel Conversion cycle bit = 0: 0.88 µs, conversion cycle bit = 1: 0.67 µs (when A/D conversion clock (ADCLK) = 48 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data registers	• 14 registers for analog input and one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • The results of A/D conversion are stored in 12-bit A/D data registers.	• 18 registers for analog input, one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion

Item	RX110 (S12ADb)	RX140 (S12ADE)
Data registers	• In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data. • Duplication of A/D conversion data — A/D conversion data of one selected analog input channel is stored in A/D data register y when conversion is started by the first trigger and into the duplication register when started by the second trigger. — Duplication is available only in single scan mode or group scan mode when double trigger mode is selected.	• The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 14 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 14 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 14 channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 18 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 18 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 18 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times.

Item	RX110 (S12ADb)	RX140 (S12ADE)
Operating mode		• Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by MTU • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Variable sampling state count • A/D-converted value addition mode • Double trigger mode (duplication of A/D conversion data)	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used

Item	RX110 (S12ADb)	RX140 (S12ADE)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the data transfer controller (DTC).
Event link function	—	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.54 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX110 (S12ADb)	RX140 (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 4, 6, 8 to 15)	A/D data register y (y = 0 to 8, 16 to 21, 24 to 26)
ADRD	—	—	A/D self-diagnosis data register
ADANSA	—	AD channel select register A	—
ADANSA0	—	—	AD channel select register A0
ADANSA1	—	—	AD channel select register A1
ADANSB	—	AD channel select register B	—
ADANSB0	—	—	AD channel select register B0
ADANSB1	—	—	AD channel select register B1
ADADS	—	A/D-converted value addition mode select register	—
ADADS0	—	—	A/D-converted value addition/ average channel select register 0
ADADS1	—	—	A/D-converted value addition/ average channel select register 1
ADADC	ADC[1:0] (RX110) ADC[2:0] (RX140)	Addition count select bits (b1, b0) b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (1 addition) 1 0: 3-time conversion (2 additions) 1 1: 4-time conversion (3 additions)	Addition count select bits (b2 to b0) b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (1 addition) 0 1 0: 3-time conversion (2 additions) 0 1 1: 4-time conversion (3 additions) 1 0 1: 16-time conversion (15 additions) Settings other than the above are prohibited.
	AVEE	—	Average mode enable bit
ADCER	DIAGVAL[1:0]	—	Self-diagnosis conversion voltage select bits
	DIAGLD	—	Self-diagnosis mode select bit
	DIAGM	—	Self-diagnosis enable bit
ADEXICR	TSS (RX110) TSSA (RX140)	Temperature sensor output A/D conversion select bits	Temperature sensor output A/D conversion select bits
	OCS (RX110) OCSA (RX140)	Internal reference voltage A/D conversion select bits	Internal reference voltage A/D conversion select bits
ADSTRGR	TRSB[3:0] (RX110) TRSB[5:0] (RX140)	A/D conversion start trigger select bits for group B (b0 to b3)	A/D conversion start trigger select bits for group B (b0 to b5)
	TRSA[3:0] (RX110) TRSA[5:0] (RX140)	A/D conversion start trigger select bits (b8 to b11)	A/D conversion start trigger select bits (b8 to b13)
ADSSTRn	—	A/D sampling state register n (n = 0 to 4, 6, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)

Register	Bit	RX110 (S12ADb)	RX140 (S12ADE)
ADDISCR	—	—	A/D disconnection detection control register
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D compare function control register
ADCMPANSR0	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	A/D compare function window A comparison condition setting register 0
ADCMPLR1	—	—	A/D compare function window A comparison condition setting register 1
ADCMPLER	—	—	A/D compare function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D compare function window A lower-side level setting register
ADCMPDR1	—	—	A/D compare function window A upper-side level setting register
ADCMPSR0	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	A/D compare function window A extended input channel status register
ADHVREFCNT	—	—	A/D high-potential/low-potential reference voltage control register
ADWINMON	—	—	A/D compare function window A/B status monitor register
ADCMPBNSR	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	A/D compare function window B lower-side level setting register
ADWINULB	—	—	A/D compare function window B upper-side level setting register
ADCMPBSR	—	—	A/D compare function window B channel status register
ADBUFn	—	—	A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register
ADCCR	—	—	A/D conversion cycle control register

Table 2.55 Comparison of A/D Conversion Start Triggers Set in the ADSTRGR Registers

Bit	RX110 (S12ADb)	RX140 (S12ADE)
TRSB[3:0] (RX110) TRSB[5:0] (RX140)	A/D conversion start trigger select for group B bits b3 b0 0 0 0 1: TRG0AN 0 0 1 0: TRG0BN 0 0 1 1: TRGAN 0 1 0 0: TRG0EN 0 1 0 1: TRG0FN	A/D conversion start trigger select for group B bits b5 b0 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRG0AN 0 0 0 0 1 0: TRG0BN 0 0 0 0 1 1: TRGAN 0 0 0 1 0 0: TRG0EN 0 0 0 1 0 1: TRG0FN 0 0 0 1 1 0: TRG4AN 0 0 1 1 1 1: TRG4BN 0 0 1 0 0 0: TRG4ABN 0 0 1 0 0 1: ELCTRG0
TRSA[3:0] (RX110) TRSA[5:0] (RX140)	A/D conversion start trigger select bits b11 b8 0 0 0 0: ADTRG0# 0 0 0 1: TRG0AN 0 0 1 0: TRG0BN 0 0 1 1: TRGAN 0 1 0 0: TRG0EN 0 1 0 1: TRG0FN	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRG0AN 0 0 0 0 1 0: TRG0BN 0 0 0 0 1 1: TRGAN 0 0 0 1 0 0: TRG0EN 0 0 0 1 0 1: TRG0FN 0 0 0 1 1 0: TRG4AN 0 0 0 1 1 1: TRG4BN 0 0 1 0 0 0: TRG4ABN 0 0 1 0 0 1: ELCTRG0

2.22 Temperature Sensor

Table 2.56 is a comparison of temperature sensor registers.

Table 2.56 Comparison of Temperature Sensor Registers

Register	Bit	RX110 (TEMPSA)	RX140 (TEMPSA)
TSCDRH, TSCDRL (RX110) TSCDR (RX140)	—	Temperature sensor calibration data register	Temperature sensor calibration data register

2.23 Data Operation Circuit

Table 2.57 is a comparative overview of data operation circuit.

Table 2.57 Comparative Overview of Data Operation Circuit

Item	RX110	RX140
Data operation function	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• The compared values either match or mismatch • The result of data addition is greater than FFFFh (overflow) • The result of data subtraction is less than 0000h (underflow)
Event linking function (output)	—	• The compared values either match or mismatch • The result of data addition is greater than FFFFh (overflow) • The result of data subtraction is less than 0000h (underflow)

2.24 RAM

Table 2.58 is a comparative overview of RAM.

Table 2.58 Comparative Overview of RAM

Item	RX110	RX140
RAM capacity	Max. 16 KB	Max. 64 KB
RAM address	• RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh • RAM capacity 10 KB RAM0: 0000 0000h to 0000 27FFh • RAM capacity 8 KB RAM0: 0000 0000h to 0000 1FFFh	• RAM capacity 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh
Access	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • RAM can be enabled or disabled.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

2.25 Flash Memory

Table 2.59 is a comparative overview of flash memory, and Table 2.60 is a comparison of flash memory registers.

Table 2.59 Comparative Overview of Flash Memory

Item	RX110	RX140 (FLASH)
Memory capacity	• User area: Up to 128 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 256 KB • Data area: Up to 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 96 KB FFFE 8000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh • Products with capacity of 32 KB FFFF 8000h to FFFF FFFFh	• Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh
Software commands	• The following software commands are implemented: Program, blank check, block erase, and unique ID read • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program, access window protect, and access window information program
Value after erasure	ROM: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area can be programmed. • Self-programming (single-chip mode) — The user area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.

Item	RX110	RX140 (FLASH)
Off-board programming	The user area can be programmed using a flash programmer compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID code protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 15.	This function is used to safely program blocks 0 to 7.
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	—	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.60 Comparison of Flash Memory Registers

Register	Bit	RX110	RX140 (FLASH)
DFLCTL	—	—	E2 DataFlash control register
FENTRYR	FENTRYD	—	E2 DataFlash P/E mode entry bit
MEMWAITR	—	—	Memory wait cycle setting register
DFLWAITR	—	—	Data flash wait cycle setting register
FPMCR	FMS0, FMS1, FSM2 (RX110) FMS0, FMS1 (RX140)	Flash operating mode select bits 0, 1, and 2 FMS2 FMS1 FMS0 0 0 0: ROM read mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.	Flash operating mode select bits 0 and 1 FMS1 FMS0 0 0: ROM/E2 DataFlash read mode 0 1: ROMP/E mode 1 0: E2 DataFlash P/E mode 1 1: Setting prohibited
	LVPE	Low-voltage P/E mode enable bit	—
FISR	PCKA[4:0] (RX110) PCKA[5:0] (RX140)	Peripheral clock notification bits	Peripheral clock notification bits
FASR	EXS	Extra area select bit 0: User area 1: Extra area	Extra area select bit 0: User area or data area 1: Extra area

Register	Bit	RX110	RX140 (FLASH)
FCR	CMD[3:0]	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 0 1: Unique ID read Settings other than the above are prohibited.	Software command setting bits b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than the above are prohibited.
	DRC	Data read completion bit	—
FEXCR	CMD[2:0]	Software command setting bits b2 b0 0 0 1: Start-up area information program 0 1 0: Access window information program Settings other than the above are prohibited.	Software command setting bits b2 b0 0 0 1: Start-up area information program/access window protect 0 1 0: Access window information program Settings other than the above are prohibited.
FSARH	—	Flash processing start address register H FSARH is an 8-bit register.	Flash processing start address register H FSARH is a 16-bit register.
FEARH	—	Flash processing end address register H FEARH is an 8-bit register.	Flash processing end address register H FEARH is a 16-bit register.
FRBH	—	Flash read buffer register H	—
FRBL	—	Flash read buffer register L	—
FWBH, FWBL (RX110) FWBn (RX140)	—	Flash write buffer register H, Flash write buffer register L	Flash write buffer register n (n = 0 to 3)
FSTATR1	DRRDY	Data read ready flag	-
FEAMH	—	Flash error address monitor register H FEAMH is an 8-bit register.	Flash error address monitor register H FEAMH is a 16-bit register.
FSCMR	AWPR	—	Access window protect flag
FAWSMR	—	Flash access window start address monitor register	Flash access window start address monitor register
		Initial value after a reset differs.	
FAWEMR	—	Flash access window end address monitor register	Flash access window end address monitor register
		Initial value after a reset differs.	
UIDRn	—	Unique ID register n (n = 0 to 31) UIDRn is an 8-bit register.	Unique ID register n (n = 0 to 3) UIDRn is a 32-bit register.

2.26 Packages

As indicated in Table 2.61, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.61 Packages

Package Type	Renesas Code	
	RX110	**RX140**
80-pin LFQFP	×	○
64-pin LFQFP	×	○
64-pin WFLGA	○	×
48-pin LFQFP	PLQP0048KB-A	PLQP0048KB-B
48-pin HWQFN	PWQN0048KB-A	PWQN0048KC-A
40-pin HWQFN	○	×
36-pin WFLGA	○	×
32-pin LQFP	×	○
32-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 64-Pin Package

Table 3.1 is a comparative listing of the pin functions of 64-pin package products.

Table 3.1 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP/ LQFP	RX110	RX140
1	P03	P03*1/DA0
2	P27/MTIOC2B/SCK1/SCK12/IRQ3/CMPA2/ CACREF/ADTRG0#	VCL
3	P26/MTIOC2A/TXD1/SMOSI1/SSDA1	MD/PG7/FINED
4	P30/RXD1/SMISO1/SSCL1/IRQ0	XCIN/PH7*3
5	P31/CTS1#/RTS1#/SS1#/IRQ1	XCOUT/PH6*3
6	MD/FINED	RES#
7	RES#	XTAL/P37/IRQ4
8	XCOUT	VSS
9	XCIN	EXTAL/P36/IRQ2
10	P35/NMI	VCC
11	XTAL	P35/NMI
12	EXTAL	P32/MTIOC0C/TMO3/TXD6*3/SMOSI6*3/ SSDA6*3/TS0*3/IRQ2/RTCOUT
13	VCL	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1
14	VSS	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0
15	VCC	P27/MTIOC2B/TMCI3/SCK1/TS3
16	P32/MTIOC0C/RTCOUT/IRQ2	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
17	P17/MTIOC0C/SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
18	P16/RTCOUT/TXD1/SMOSI1/SSDA1/ MOSIA/SCL0/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ RTCOUT/ADTRG0#
19	P15/MTIOC0B/MTCLKB/RXD1/SMISO1/ SSCL1/RSPCKA/IRQ5/CLKOUT	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*3/IRQ5
20	P14/MTIOC0A/MTCLKA/CTS1#/RTS1#/ SS1#/SSLA0/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*3/IRQ4
21	PH3/MTIOC1A	PH3/MTIOC4D/TMCI0/TS7*3
22	PH2/IRQ1	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1
23	PH1/IRQ0	PH1/MTIOC3D/TMO0/TS9*3/IRQ0
24	PH0/MTIOC1B/CACREF	PH0/MTIOC3B/TS10*3/CACREF
25	P55	P55/MTIOC4A/MTIOC4D/TMO3/CRXD0/ TS11*3
26	P54	P54/MTIOC4B/TMCI1/CTXD0/TS12*3

64-Pin LFQFP/ LQFP	RX110	RX140
27	PC7/MTCLKB/TXD1/SMOSI1/SSDA1/ MISOA/CACREF	PC7/MTIOC3A/MTCLKB/TMO2/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/TS13/ CACREF
28	PC6/MTCLKA/RXD1/SMISO1/SSCL1/ MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14
29	PC5/MTCLKD/SCK1/RSPCKA	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15
30	PC4/MTCLKC/SCK5/SSLA0/IRQ2/CLKOUT	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP
31	PC3/TXD5/SMOSI5/SSDA5	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ TS16*3
32	PC2/RXD5/SMISO5/SSCL5/SSLA3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ SSLA3/TS17*3
33	PB7/PC1	PB7/PC1*2/MTIOC3B/TXD9*3/SMOSI9*3/ SSDA9*3/TS18*3
34	PB6/PC0	PB6/PC0*2/MTIOC3D/RXD9*3/SMISO9*3/ SSCL9*3/TS19*3
35	PB5/MTIOC2A/MTIOC1B	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/ SCK9*3/TS20*3
36	PB3/MTIOC0A	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/ LPTO/SCK6*3/TS22*3
37	PB1/MTIOC0C/IRQ4	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6*3/ SMOSI6*3/SSDA6*3/TS24*3/IRQ4/CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/MTIOC0C/RTCOUT/SCL0/ RSPCKA/IRQ2/ADTRG0#	PB0/MTIOC3D/MTIC5W/RXD6*3/SMISO6*3/ SSCL6*3/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/MTIOC2A/CTS5#/ RTS5#/SS5#/SDA0/MOSIA/IRQ3	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3
42	PA4/MTIC5U/MTCLKA/MTIOC2B/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
43	PA3/MTIOC0D/MTCLKD/MTIOC1B/RXD5/ SMISO5/SSCL5/MISOA/IRQ6	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/RTCOUT/SCK5/ SSLA2	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
45	PA0/SSLA1/CACREF	PA0/MTIOC4A/SSLA1/TS32*3/CACREF
46	PE5/MTIOC2B/IRQ5/AN013	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/ CMPOB0
47	PE4/MTIOC1A/MOSIA/IRQ4/AN012	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
48	PE3/MTIOC0A/MTIOC1B/CTS12#/RTS12#/ SS12#/RSPCKA/IRQ3/AN011	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/TS34/AN019/CLKOUT
49	PE2/RXD12/RXDX12/SMISO12/SSCL12/ IRQ7/AN010	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/ SSCL12/TS35/IRQ7/AN018/CVREFB0
50	PE1/TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/IRQ1/AN009	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/AN017/CMPB0
51	PE0/MTIOC2A/SCK12/IRQ0/AN008	PE0/SCK12/AN016
52	PE7/IRQ7/AN015	P47*1/AN007
53	PE6/IRQ6/AN014	P46*1/AN006

64-Pin LFQFP/ LQFP	RX110	RX140
54	P46*1/AN006	P45*1/AN005
55	P44*1/AN004	P44*1/AN004
56	P43*1/AN003	P43*1/AN003
57	P42*1/AN002	P42*1/AN002
58	P41*1/AN001	P41*1/AN001
59	VREFL0/PJ7*1	VREFL0/PJ7*1
60	P40*1/AN000	P40*1/AN000
61	VREFH0/PJ6*1	VREFH0/PJ6*1
62	AVSS0	AVCC0
63	AVCC0	P05*1/DA1
64	P05	AVSS0

Notes: 1. The power supply of the I/O buffer for these pins is AVCC0.
2. PC0 and PC1 are valid only when the port switching function is selected.
3. Not implemented on products with ROM capacity of 64 KB.

3.2 48-Pin Package

Table 3.2 is a comparative listing of the pin functions of 48-pin package products.

Table 3.2 Comparative Listing of 48-Pin Package Pin Functions

48-Pin LFQFP/ HWQFN	RX110	RX140
1	P27/MTIOC2B/SCK1/SCK12/IRQ3/CMPA2/ CACREF/ADTRG0#	VCL
2	P26/MTIOC2A/TXD1/SMOSI1/SSDA1	MD/PG7/FINED
3	MD/FINED	RES#
4	RES#	XTAL/P37/IRQ4
5	XCOUT	VSS
6	XCIN	EXTAL/P36/IRQ2
7	P35/NMI	VCC
8	XTAL	P35/NMI
9	EXTAL	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ TS1*3/IRQ1
10	VCL	P30/MTIOC4B/TMRI3/POE8#/RXD1/ SMISO1/SSCL1/TS2*3/IRQ0
11	VSS	P27/MTIOC2B/TMCI3/SCK1/TS3
12	VCC	P26/MTIOC2A/TMO1/LPTO/TXD1/SMOSI1/ SSDA1/TS4
13	P17/MTIOC0C/SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ SCK1/MISOA/SDA0/IRQ7
14	P16/RTCOUT/TXD1/SMOSI1/SSDA1/ MOSIA/SCL0/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/ SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ ADTRG0#/RTCOUT
15	P15/MTIOC0B/MTCLKB/RXD1/SMISO1/ SSCL1/RSPCKA/IRQ5/CLKOUT	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/CRXD0/TS5*3/IRQ5
16	P14/MTIOC0A/MTCLKA/CTS1#/RTS1#/ SS1#/SSLA0/TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTXD0/TS6*3/IRQ4
17	PH3/MTIOC1A	PH3/MTIOC4D/TMCI0/TS7*3
18	PH2/IRQ1	PH2/MTIOC4C/TMRI0/TS8*3/IRQ1
19	PH1/IRQ0	PH1/MTIOC3D/TMO0/TS9*3/IRQ0
20	PH0/MTIOC1B/CACREF	PH0/MTIOC3B/TS10*3/CACREF
21	PC7/MTCLKB/TXD1/SMOSI1/SSDA1/ MISOA/CACREF	PC7/MTIOC3A/TMO2/MTCLKB/LPTO/ TXD8*3/SMOSI8*3/SSDA8*3/MISOA/TS13/ CACREF
22	PC6/MTCLKA/RXD1/SMISO1/SSCL1/MOSIA	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8*3/ SMISO8*3/SSCL8*3/MOSIA/TS14
23	PC5/MTCLKD/SCK1/RSPCKA	PC5/MTIOC0C/MTIOC3B/MTCLKD/TMRI2/ SCK8*3/RSPCKA/TS15
24	PC4/MTCLKC/SCK5/SSLA0/IRQ2/CLKOUT	PC4/MTIOC0A/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#*3/RTS8#*3/SS8#*3/ SSLA0/TSCAP
25	PB5/PC3/MTIOC2A/MTIOC1B	PB5/PC3*1/MTIOC2A/MTIOC1B/TMRI1/ POE1#/TS20*3
26	PB3/PC2/MTIOC0A	PB3/PC2*1/MTIOC0A/MTIOC4A/TMO0/ POE3#/LPTO/SCK6*3/TS22*3

48-Pin LFQFP/ HWQFN	RX110	RX140
27	PB1/PC1/MTIOC0C/IRQ4	PB1/PC1*1/MTIOC0C/MTIOC4C/TMCI0/ TXD6*3/SMOSI6*3/SSDA6*3/TS24*3/IRQ4/ CMPOB1
28	VCC	VCC
29	PB0/PC0/MTIC5W/MTIOC0C/RTCOUT/ SCL0/RSPCKA/IRQ2/ADTRG0#	PB0/PC0*1/MTIOC3D/MTIC5W/RXD6*3/ SMISO6*3/SSCL6*3/RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/MTIOC2A/CTS5#/ RTS5#/SS5#/SDA0/MOSIA/IRQ3	PA6/MTIOC3D/MTIC5V/MTCLKB/TMCI3/ POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26*3
32	PA4/MTIC5U/MTCLKA/MTIOC2B/TXD5/ SMOSI5/SSDA5/SSLA0/IRQ5	PA4/MTIOC4C/MTIC5U/MTCLKA/TMRI0/ TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/ CVREFB1
33	PA3/MTIOC0D/MTCLKD/MTIOC1B/RXD5/ SMISO5/SSCL5/MISOA/IRQ6	PA3/MTIOC0D/MTIOC4D/MTIC5V/MTCLKD/ RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/RTCOUT/SCK5/ SSLA2	PA1/MTIOC0B/MTIOC3B/MTCLKC/SCK5/ SSLA2/TS31
35	PE4/MTIOC1A/MOSIA/IRQ4/AN012	PE4/MTIOC4D/MTIOC1A/MTIOC4A/TS33/ AN020/CMPA2/CLKOUT
36	PE3/MTIOC0A/MTIOC1B/CTS12#/RTS12#/ SS12#/RSPCKA/IRQ3/AN011	PE3/MTIOC1B/MTIOC4B/POE8#/CTS12#/ RTS12#/TS34/AN019/CLKOUT
37	PE2/RXD12/RXDX12/SMISO12/SSCL12/ IRQ7/AN010	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/ TS35/IRQ7/AN018/CVREFB0
38	PE1/TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/IRQ1/AN009	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/ SSDA12/AN017/CMPB0
39	PE0/MTIOC2A/SCK12/IRQ0/AN008	P47*2/AN007
40	PE7/IRQ7/AN015	P46*2/AN006
41	P46*2/AN006	P45*2/AN005
42	P42*2/AN002	P42*2/AN002
43	P41*2/AN001	P41*2/AN001
44	VREFL0/PJ7*2	VREFL0/PJ7*2
45	P40*2/AN000	P40*2/AN000
46	VREFH0/PJ6*2	VREFH0/PJ6*2
47	AVSS0	AVCC0
48	AVCC0	AVSS0

Notes: 1. PC0 to PC3 are valid only when the port switching function is selected.
2. The power supply of the I/O buffer for these pins is AVCC0.
3. Not implemented on products with ROM capacity of 64 KB.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX140 Group and the RX110 Group. 4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX110 Group is compatible with the RX140 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX140 Group and RX110 Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 12-Bit AD Converter

The RX140 Group incorporates significant changes to the 12-bit A/D converter registers, compared to the RX110 Group. This results in a reduction in software compatibility.

4.1.2 Exception Vector Table

On the RX110 Group the vector table is assigned to a fixed address space, but on the RX140 Group the vector table address can be changed by specifying a value for the start address in the exception table register (EXTB).

4.1.3 Restrictions on Comparison Function

On the RX140 Group the comparison function of the 12-bit A/D converter has the following restrictions:

1. Use of the self-diagnostic function and double-trigger mode are prohibited.
   (The ADRD and ADDBLDR registers are not covered by the comparison function.)
2. Single scan mode must be used for matching or unmatching event output.
3. When temperature sensor or internal reference voltage is selected for window A, operation of window B is prohibited.
4. When temperature sensor or internal reference voltage is selected for window B, operation of window A is prohibited.
5. The same channel cannot be set for both window A and window B.
6. Single scan mode must be selected in order to use the buffer function.
   (The buffer function cannot be used in conjunction with double trigger mode.)
7. It is necessary to make settings such that high-side reference value ≥ low-side reference value.

4.1.4 Port Direction Register (PDR) Initialization

PDR register initialization differs even between products with the same pin count.

4.1.5 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time of the 12-bit A/D converter differs on the RX110 Group and RX140 Group. The scan conversion time (t_{SCAN}) for single scan operation where the number of selected channels is n is shown below for each group. For details, refer to the description of analog input sampling and scan conversion time on the 12-bit A/D converter in the User's Manual: Hardware of the RX110 Group and RX140 Group, respectively, listed in 5, Reference Documents.

RX110: $t_{SCAN} = t_D + (t_{SPL} + t_{CONV}) \ n + t_{ED}$

RX140: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_D: Start-of-scanning-delay time

t_{SPL}: Sampling time

t_{DIS}: Disconnection detection assistance processing time

t_{DIAG}: Self-diagnosis A/D conversion processing time

t_{CONV}: A/D conversion processing time

t_{ED}: End-of-scanning-delay time

4.1.6 I^2C Bus Interface Noise Cancellation

The RX110 Group incorporates analog noise filters for the SCL and SDA lines, but the RX140 Group does not have analog noise filters.

5. Reference Documents

User's Manual: Hardware

RX110 Group User's Manual: Hardware Rev.1.20 (R01UH0421EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX140 Group User's Manual: Hardware Rev.1.10 (R01UH0905EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

RX Family Design Guide for Migration between RX Family Differences in Package External Form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Updates/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

TN-RX*-A180A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A0230A/E

TN-RX*-A0224B/E

TN-RX*-A0241B/E

TN-RX*-A0258A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 24, 2021	—	First edition issued
1.10	Mar.28, 2022	16	*Revised:* Table 2.9 Comparison of Clock Generation Circuit Registers
		29	*Revised:* Table 2.24 Comparative Overview of I/O Ports (64-Pin)
		82	*Revised:* Table 3.1 Comparative Listing of 64-Pin Package Pin Functions
1.11	May.26, 2022	82	*Revised:* Table 3.1 Comparative Listing of 64-Pin Package Pin Functions
		85	*Revised:* Table 3.2 Comparative Listing of 48-Pin Package Pin Functions

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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