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# SH7263 Group

## Display Operation of the LCD Controller

### Introduction

This application note describes an example of setting up the LCD controller (LCDC) of the SH7263 to control a display panel. Please use the sample program for technical reference in software development.

### Target Device

SH7263

### Contents

# 1. Preface

## 1.1 Specifications

In this sample program, after release from a power on reset, peripheral modules are initialized and display operation of the LCD controller (LCDC) proceeds.

- The program is located in flash memory within the CS0 space.
- Synchronous DRAM (SDRAM) where display data are stored is connected to the CS3 space via a 16-bit bus.
- An LCD (TFT-LCD) panel is connected and the color depth is set to 16 bpp.
- Images are displayed at QVGA size (240 × 320 pixels).

## 1.2 Modules Used

- Clock pulse generator (CPG)
- Bus state controller (BSC)
- Pin function controller (PFC)
- LCD controller (LCDC)

## 1.3 Applicable Conditions

| | |
|---|---|
| MCU | SH7263 |
| Operating frequency | Internal clock: 200 MHz<br>Bus clock: 66 MHz<br>Peripheral clock: 33 MHz |
| Evaluation board | SH7263 evaluation board: R0K572630D001BR<br>16-MB SDRAM with fixed 16-bit bus: EDS1216AATA-75E available from Elpida Memory<br>4-MB NOR-type flash memory: M5M29KT331AVP available from Renesas Technology |
| LCD panel | Color TFT-LCD: H320 × V240 |
| C compiler: | SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01,<br>available from Renesas Technology |
| Compiler options: | -cpu = sh2afpu -fpu = single -include = "$(WORKSPDIR)\inc" -message<br>-object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto –fpscr = safe<br>-chgincpath -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0<br>-del_vacant_loop = 0 -struct_alloc = 1 -nologo |

## 1.4 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the application note *Example of Initial Configuration* for the SH7263/SH7203 (REJ06B0740). Please refer to that document in combination with this one.

## 2. Description of the Sample Application

This application note describes initialization for the control of an LCD display.

To execute this program, a separate initialization program that handles the minimum of settings for hardware initialization, such as the initialization of memory, is also required.

### 2.1 Overview of LCD Controller

A unified memory architecture is adopted for the LCD controller (LCDC) so that the image data for display is stored in system memory. The LCDC module reads data from system memory, uses the palette memory to determine the colors, then puts the display on the LCD panel. Furthermore, data for display on the LCD panel can be directly read from the system memory. The LCDC is connectable to LCD modules of the STN, dual-STN, and TFT type that employ a serial interface.

A certain area of SDRAM (CS3 space)* that has been connected to the CPU is used as video RAM (VRAM) for storing image data for display on the LCDC, which makes dedicated display memory unnecessary. Furthermore, the LCDC includes a 2.4-KB line buffer so that stable displays are possible.

Table 1 gives an outline of the LCDC functions and figure 1 is a block diagram of the LCDC.

Configurations of pins and registers are given in tables 2 and 3, respectively.

Note: * Display operation with the VRAM in SDRAM (CS2 space) or on-chip RAM is not possible.

**Table 1 Outline of the LCDC Functions**

| Features | Description | Note |
|---|---|---|
| Panel interface | Serial interface method | — |
| Type of LCD | STN/Dual-STN/TFT | — |
| Panel data format | 8/12/16/18-bit bus width | — |
| Color mode | 4/8/15/16 bpp | — |
| Grayscale mode | 1/2/4/6 bpp | — |
| Panel size | 16 × 1 to 1,024 × 1,024 | — |
| Color palette | 24 bits | 16 of the 24 bits are valid; R: 5/G: 6/B: 5 |
| Display in neutral colors for STN/DSTN panels | 24-bit space-modulation FRC with 8-bit RGB values for reduced flicker | Controller applies 65,536-color control for reduced flicker. |
| VRAM | A certain area of the synchronous DRAM (CS3 space) is used as VRAM. | Dedicated display memory is not required. |
| Line buffer | 2.4 KB | Display is stabilized. |
| Signal polarity | Programmable | A facility for inverting the levels of output signals is available. |
| Data format | The endian of bytes and a packed pixel method are selectable. | — |
| Hardware-rotation mode | Available | The width for display on the panel before rotation must be within 320 pixels. |
| Interrupt | An interrupt can be generated at a user-specified position. | Tiering (flicker) is prevented. |

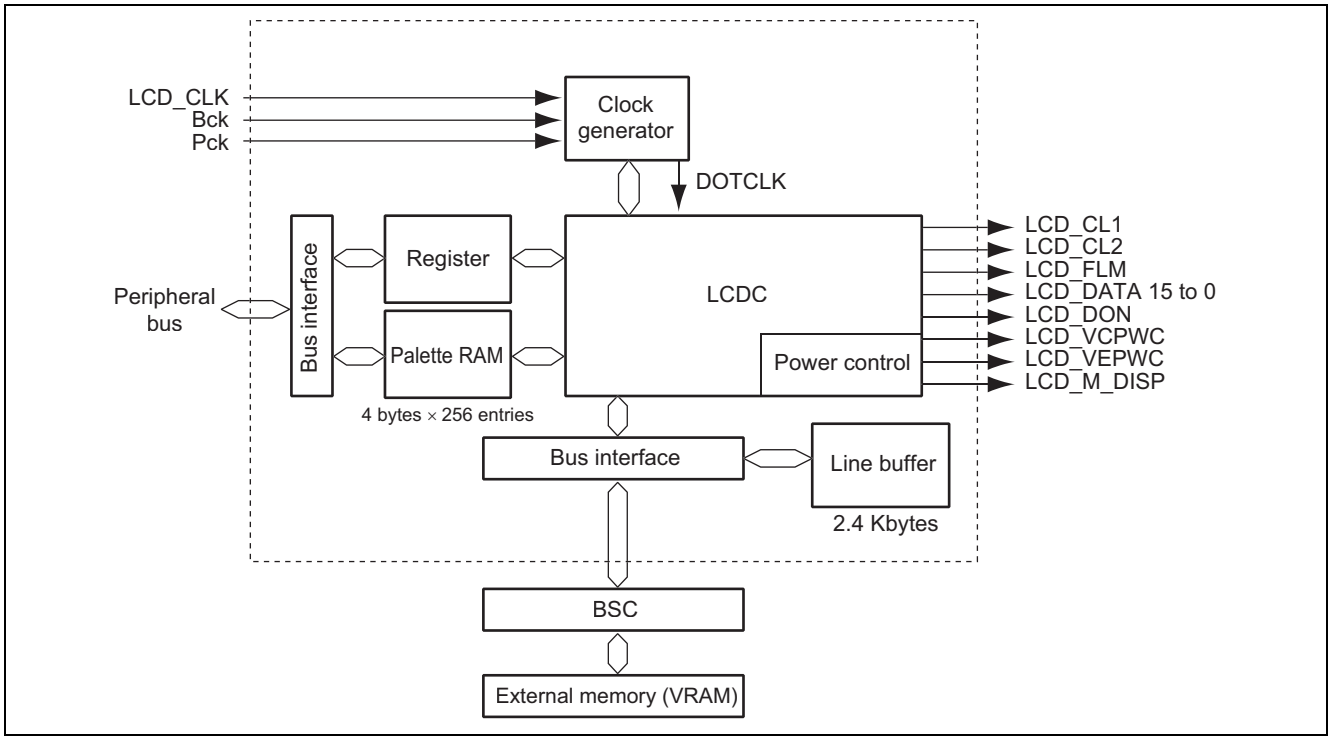


**Figure 1 LCDC Block Diagram**

**Table 2 Pin Configuration**

| Pin Name | I/O | Function |
|---|---|---|
| LCD_DATA15 to 0 | Output | Data for LCD panel |
| LCD_DON | Output | Display-on signal (DON) |
| LCD_CL1 | Output | Shift-clock 1 (STN/DSTN)/horizontal sync signal (HSYNC) (TFT) |
| LCD_CL2 | Output | Shift-clock 2 (STN/DSTN)/dot clock (DOTCLK) (TFT) |
| LCD_M_DISP | Output | LCD current-alternating signal/DISP signal |
| LCD_FLM | Output | First line marker/vertical sync signal (VSYNC) (TFT) |
| LCD_VCPWC | Output | LCD-module power control (VCC) |
| LCD_VEPWC | Output | LCD-module power control (VEE) |
| LCD_CLK | Input | LCD clock-source input |

**Table 3 Register Configuration**

| Register Name | Abbreviation | R/W | Initial Value | Address | Access Size |
|---|---|---|---|---|---|
| LCDC input clock register | LDICKR | R/W | H'0101 | H'FFFF FC00 | 16 |
| LCDC module type register | LDMTR | R/W | H'0109 | H'FFFF FC02 | 16 |
| LCDC data format register | LDDFR | R/W | H'000C | H'FFFF FC04 | 16 |
| LCDC scan mode register | LDSMR | R/W | H'0000 | H'FFFF FC06 | 16 |
| LCDC start address register for upper display panel data fetch | LDSARU | R/W | H'0C00 0000 | H'FFFF FC08 | 32 |
| LCDC start address register for lower display panel data fetch | LDSARL | R/W | H'0C00 0000 | H'FFFF FC0C | 32 |
| LCDC line address offset register for display panel fetch data | LDLAOR | R/W | H'0280 | H'FFFF FC10 | 16 |
| LCDC palette control register | LDPALCR | R/W | H'0000 | H'FFFF FC12 | 16 |
| Palette data registers 00 to FF | LDPR00 to LDPRFF | R/W | — | H'FFFF F800 to H'FFFF FBFC | 32 |
| LCDC horizontal character number register | LDHCNR | R/W | H'4F52 | H'FFFF FC14 | 16 |
| LCDC horizontal sync signal register | LDHSYNR | R/W | H'0050 | H'FFFF FC16 | 16 |
| LCDC vertical display line number register | LDVDLNR | R/W | H'01DF | H'FFFF FC18 | 16 |
| LCDC vertical total line number register | LDVTLNR | R/W | H'01DF | H'FFFF FC1A | 16 |
| LCDC vertical sync signal register | LDVSYNR | R/W | H'01DF | H'FFFF FC1C | 16 |
| LCDC AC modulation signal toggle line number register | LDACLNR | R/W | H'000C | H'FFFF FC1E | 16 |
| LCDC interrupt control register | LDINTR | R/W | H'0000 | H'FFFF FC20 | 16 |
| LCDC power management mode register | LDPMMR | R/W | H'0010 | H'FFFF FC24 | 16 |
| LCDC power-supply sequence period register | LDPSPR | R/W | H'F60F | H'FFFF FC26 | 16 |
| LCDC control register | LDCNTR | R/W | H'0000 | H'FFFF FC28 | 16 |
| LCDC user specified interrupt control register | LDUINTR | R/W | H'0000 | H'FFFF FC34 | 16 |
| LCDC user specified interrupt line number register | LDUINTLNR | R/W | H'004F | H'FFFF FC36 | 16 |
| LCDC memory access interval number register | LDLIRNR | R/W | H'0000 | H'FFFF FC40 | 16 |

## 2.2 Example of Circuitry for LCD Connection

### 2.2.1 Connecting the Evaluation Circuit for LCD

The LCD panel (TFT-LCD) which is used in this sample program accepts 16-bit RGB data for a display at the QVGA size. SDRAM in the CS3 space (0x0C00 0000 to 0x0FFF FFFF: cache enabled space, or 0x2C00 0000 to 0x2FFF FFFF: cache disabled space) is used as VRAM, i.e. memory for the storage of image data for display.

Figure 2 shows the hardware configuration for this sample application.

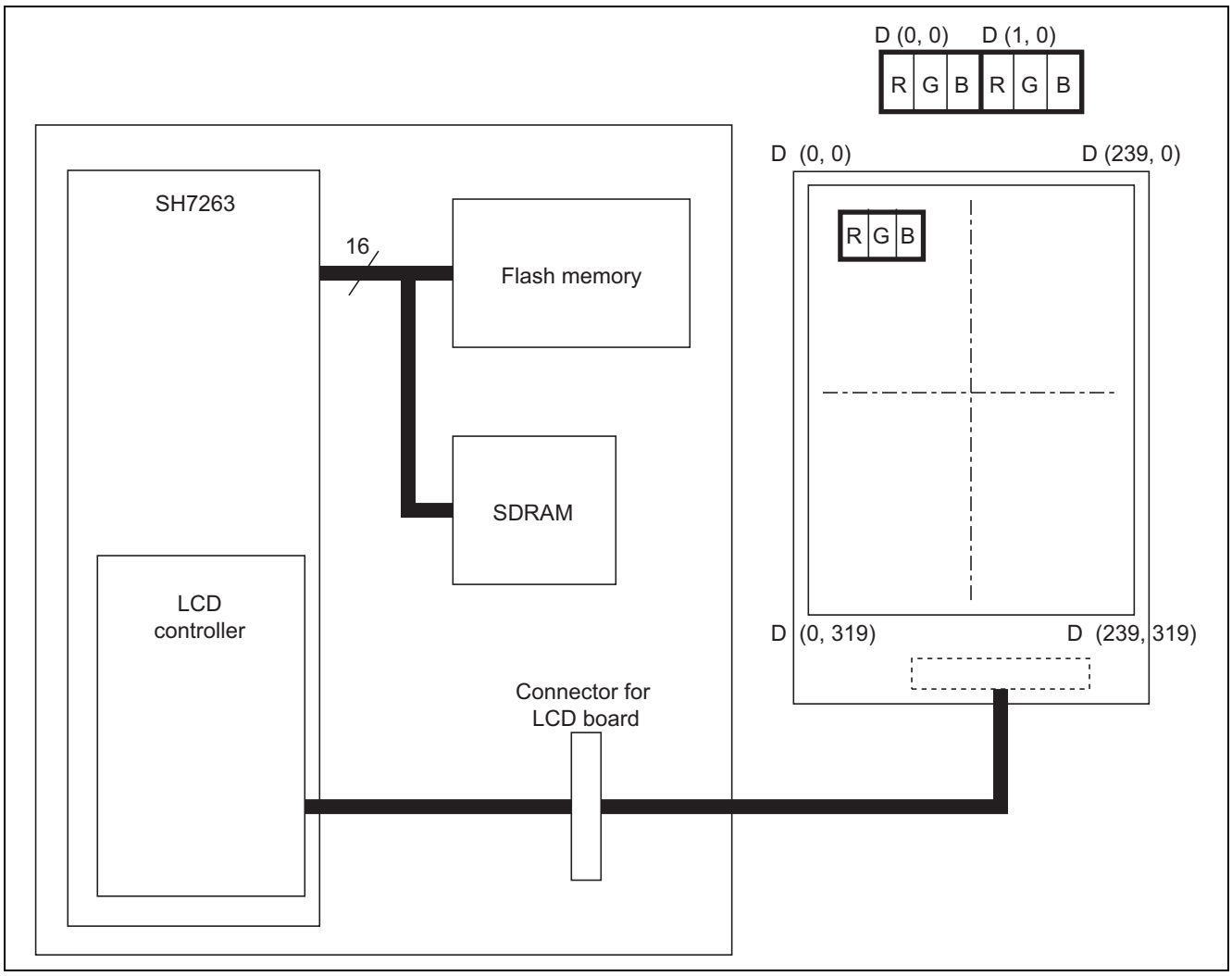


**Figure 2 Hardware Configuration for the Sample Application**

### 2.2.2 Connection with the LCD Panel

Figure 3 shows an example of connection with the LCD panel used in this sample application.

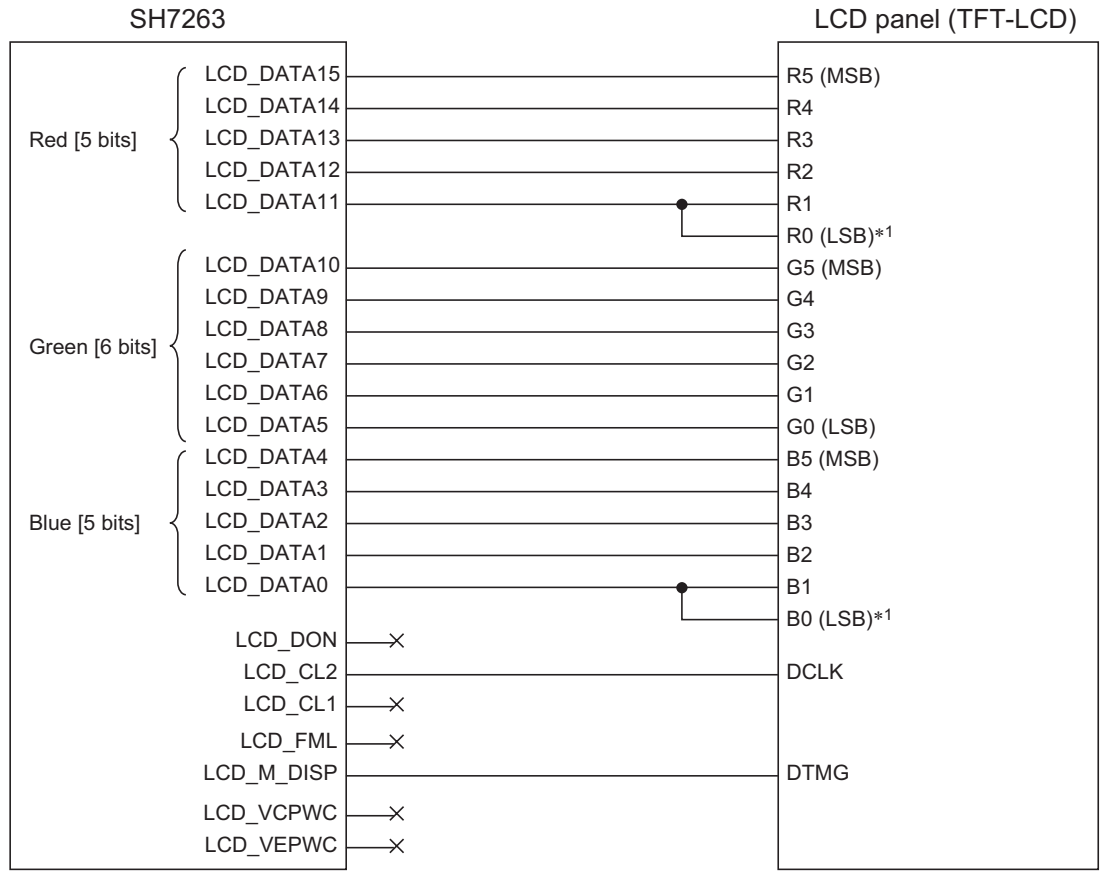


**Figure 3 Example of Connection with the LCD Panel**

**Table 4 List of LCD Pins**

| Pin Name | Function |
|---|---|
| LCD_DATA15 to 0 | Data for LCD panel |
| LCD_DON | LCD display-on signal |
| LCD_CL1 | Shift-clock 1: horizontal sync signal |
| LCD_CL2 | Shift-clock 2: dot clock |
| LCD_M_DISP | LCD current-alternating signal |
| LCD_FLM | First line marker (vertical sync signal) |
| LCD_VCPWC | LCD-module power control (VCC) |
| LCD_VEPWC | LCD-module power control (VEE) |
| LCD_CLK | LCD clock-source input |

### 2.2.3 Example of Clock and LCD Data Signals

Figure 4 shows an example of LCD data signals.

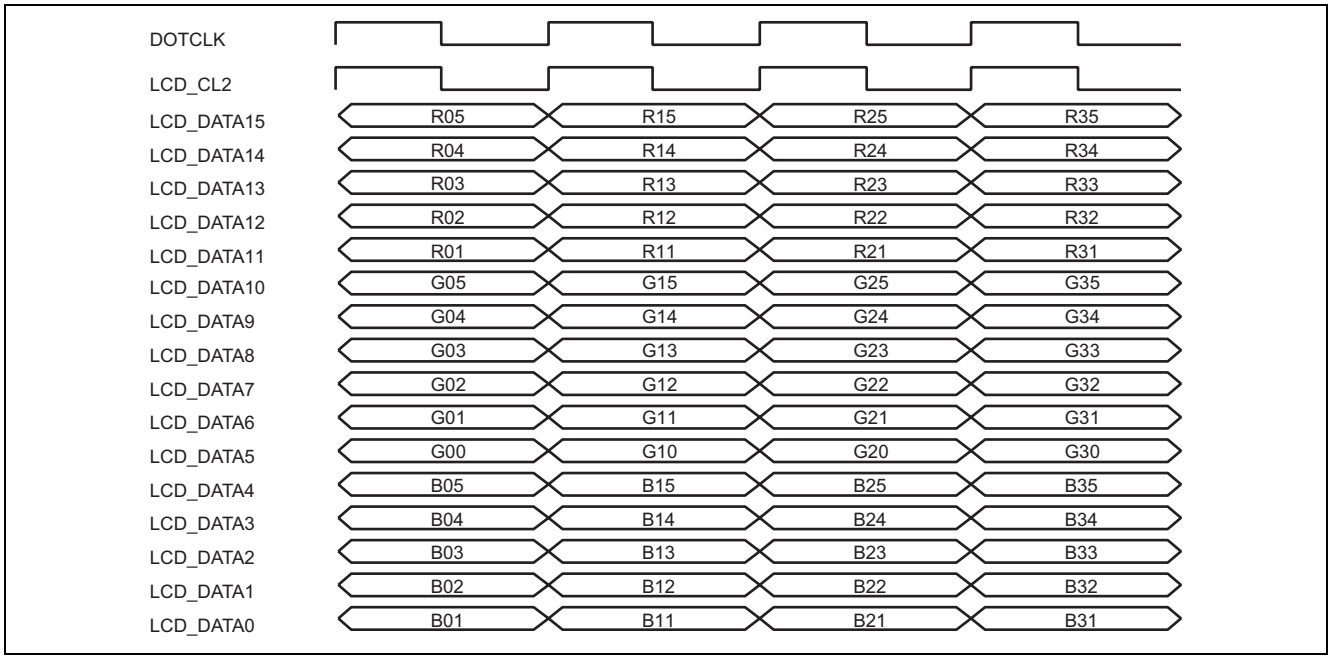


**Figure 4 Example of LCD Data Signals (Color TFT Module for a 16-Bit Data Bus)**

## 2.3 Outline of Areas

The SH7263 has a 32-bit address space that is divided into cacheable space, non-cacheable space, and internal space (on-chip RAM, on-chip peripheral modules, reserved) by the higher-order bits.

Figure 5 shows the memory map for the sample application.

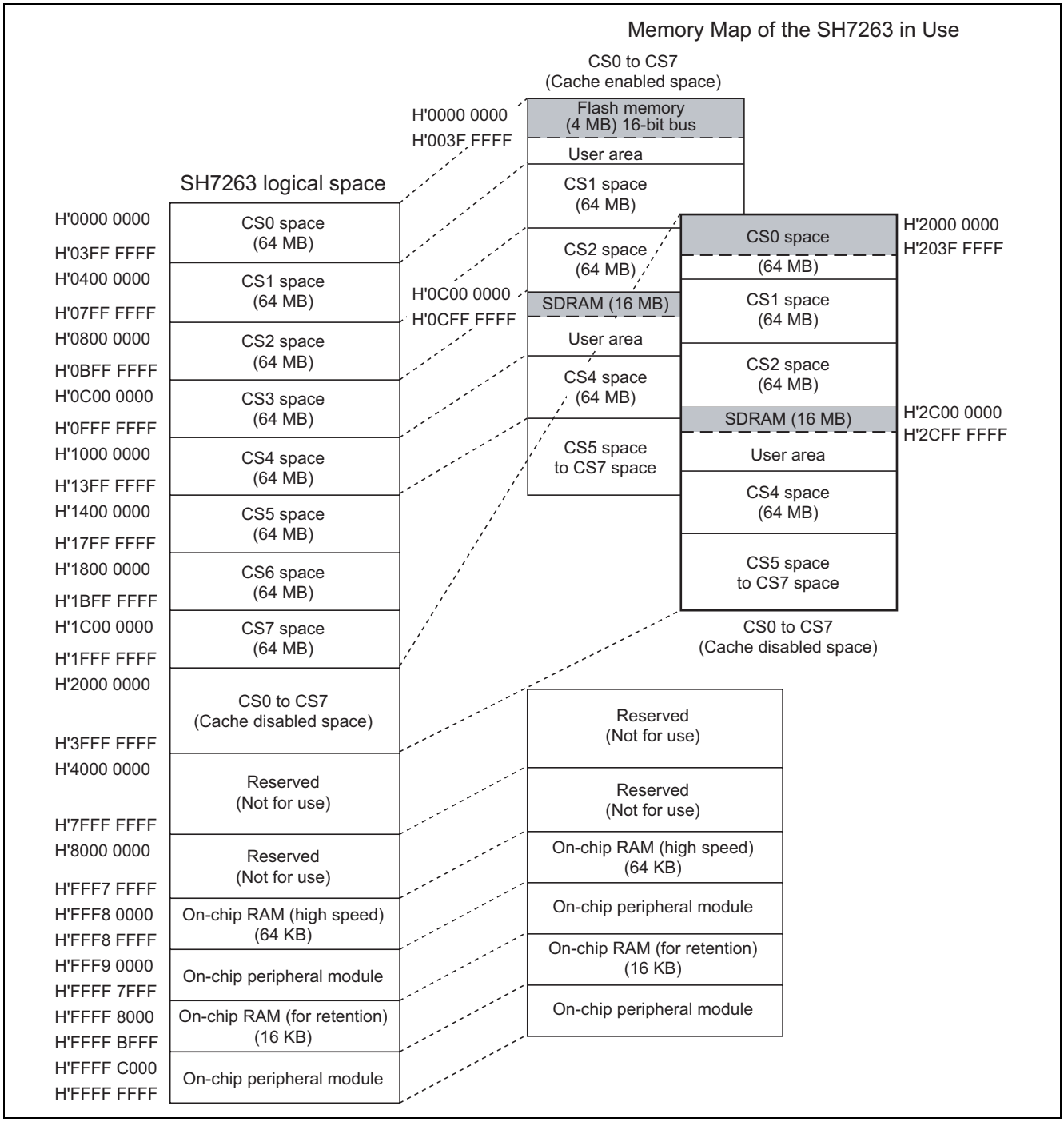


**Figure 5 Memory Map for the Sample Application**

## 2.4 Description of Operation

### 2.4.1 Bus Occupancy Ratio

This LCDC is capable of controlling displays with up to 1,024 × 1,024 dots and 16 bpp (bits per pixel). The image data for display is stored in VRAM, which is shared with the CPU. This LCDC should read the data from VRAM before display.

SH7263 has a maximum 32-burst memory read operation and a 2.4-Kbyte line buffer, so although a complete breakdown of the display is unlikely, there may be some problems with the display depending on the combination. A recommended size at the frame rate of 60 Hz is 320 × 240 dots in 16 bpp or 640 × 480 dots in 8 bpp.

As a rough standard, the bus occupancy ratio shown below should not exceed 40%.

$$\text{Bus occupancy ratio (\%)} = \frac{\text{Overhead coefficient} \times \text{Total number of display pixels ((HDCN + 1)} \times 8 \times \text{(VDLN + 1))} \times \text{Frame rate (Hz)} \times \text{Number of colors (bpp)}}{\text{CKIO (Hz)} \times \text{Bus width (bit)}} \times 100$$

The overhead coefficient becomes 1.375 when the CL2 SDRAM is connected to a 32-bit data bus and 1.188 when connected to a 16-bit data bus. The data bus width of the SDRAM used in this sample program is fixed at 16 bits. The overhead coefficient, therefore, is 1.118.

Table 5 gives bus occupancy ratio of the sample program and figure 6 shows the timing where the display is valid, retrace periods, and so on.

**Table 5 Bus Occupation Ratio of the Sample Program**

| | | |
|---|---|---|
| Overhead coefficient | CL2 16-bit bus | 1.118 |
| Number of horizontal characters for display | 240 dots = (HDCN + 1) × 8 dots | HDCN = 29 |
| Number of lines for display vertically | 320 lines = VDLN + 1 | VDLN = 319 |
| Frame rate | — | 60 Hz |
| Number of colors | R-G-B [5:6:5] | 16 bpp |
| CKIO | Bus clock | 66 MHz (Bϕ) |
| **Bus occupation ratio** | **7.80%** | |

Note: HDCN is specified by the number of characters for display (in 8-bit units) – 1.

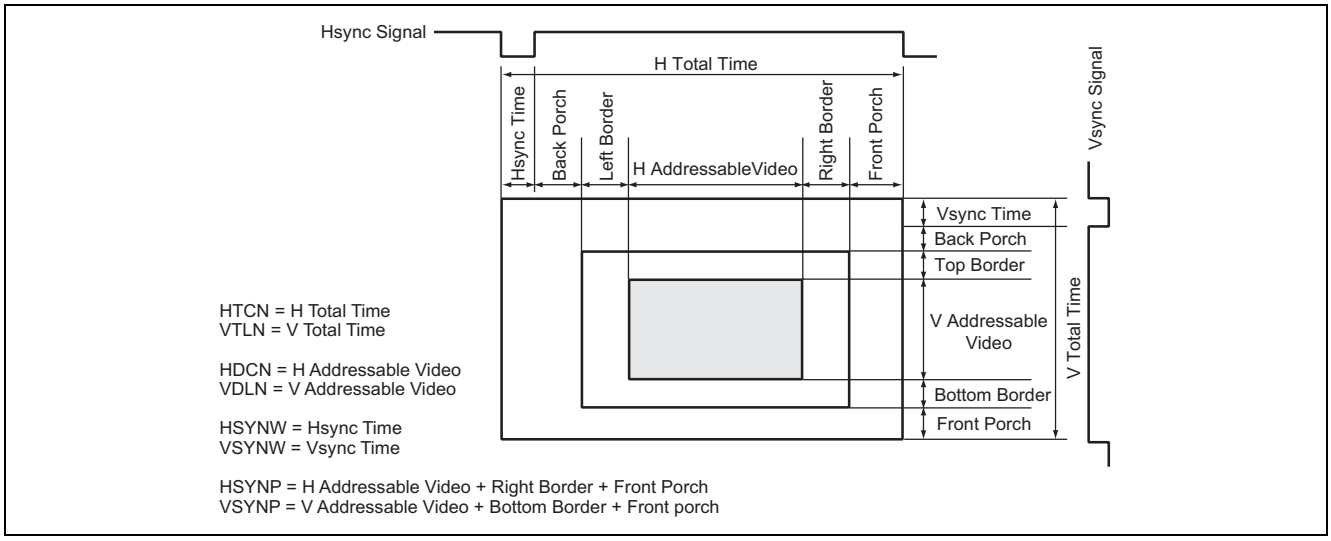


**Figure 6 Valid Display and Retrace Periods**

### 2.4.2 Color Palette Specification

Color palette registers are not set in the sample application. If a color palette is to be used, make settings with reference to the description below.

(1) Color Palette Register

This LCDC has a color palette which outputs 24 bits of data per entry and is able to simultaneously hold 256 entries. The color palette thus allows the simultaneous display of 256 colors chosen from among 16-M colors.

The procedure below may be used to set up color palettes at any time.

Figure 7 shows the data format for a color-palette entry and table 6 indicates the arrangement of settings in a color-palette register.

1. Set the PALEN bit in the LDPALCR to 0 (initial value); normal display operation.
2. Access LDPALCR and set the PALEN bit to 1; enter color-palette setting mode after three cycles of peripheral clock.
3. Access LDPALCR and confirm that the PALS bit is 1.
4. Access LDPR00 to LDPRFF and write the required values to the PALD00 to PALDFF bits.
5. Access LDPALCR and clear the PALEN bit to 0; return to normal display mode after a single cycle of peripheral clock.

A 0 is output on the LCDC display data output (LCD_DATA) while the PALS bit in LDPALCR is set to 1.

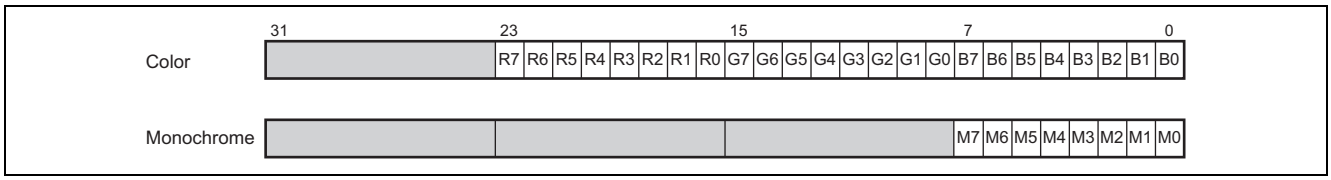


**Figure 7 Data Format for Color-Palette Entry**

**Table 6 Settings of a Color Palette Register (PALDnn Color/Gradation)**

| Bit | Bit Name | Color Data | Color | Monochrome |
|---|---|---|---|---|
| 31 to 24 | — | — | Read-only bits, so writing is not possible. | Read-only bits, so writing is not possible. |
| 23 | PALDnn23 | R data | Setting for R data | Don't care |
| 22 | PALDnn22 | | | |
| 21 | PALDnn21 | | | |
| 20 | PALDnn20 | | | |
| 19 | PALDnn19 | | | |
| 18 | PALDnn18 | | • When the setting is 0, write 0.<br>• When the setting is a value other than 0, write 1 or 0. | |
| 17 | PALDnn17 | | | |
| 16 | PALDnn16 | | | |
| 15 | PALDnn15 | G data | Setting for G data | |
| 14 | PALDnn14 | | | |
| 13 | PALDnn13 | | | |
| 12 | PALDnn12 | | | |
| 11 | PALDnn11 | | | |
| 10 | PALDnn10 | | | |
| 9 | PALDnn9 | | • When the setting is 0, write 0.<br>• When the setting is a value other than 0, write 1 or 0. | |
| 8 | PALDnn8 | | | |
| 7 | PALDnn7 | (Color)<br>B data | Setting for B data | Setting for M data |
| 6 | PALDnn6 | | | |
| 5 | PALDnn5 | | | |
| 4 | PALDnn4 | (Monochrome)<br>M data | | |
| 3 | PALDnn3 | | | |
| 2 | PALDnn2 | | • When the setting is 0, write 0.<br>• When the setting is a value other than 0, write 1 or 0. | • When the setting is 0, write 0.<br>• When the setting is a value other than 0, write 1 or 0. |
| 1 | PALDnn1 | | | |
| 0 | PALDnn0 | | | |

Note: Although ▒▒▒▒▒▒ indicates ineffective data, write values to these bits.
For details on the settings, see the description of color-palette specification in the *SH7263 Group Hardware Manual* (REJ09B0290).

### 2.4.3 Notes on Usage

- Follow the procedure below to halt access to VRAM for storing display data (synchronous DRAM in the CS3 space).

  1. Confirm that the LPS1 and LPS0 bits in LDPMMR are currently set to 1.
  2. Clear the DON bit in LDCNTR to 0 (display-off mode).
  3. Confirm that the LPS1 and LPS0 bits in LDPMMR have changed to 0.
  4. Wait for the display time for a single frame to elapse.

  This halting procedure is required before selecting self-refreshing for the display data storage VRAM (synchronous DRAM in area 3) or making a transition to standby mode or module standby mode.

- Do not access SDRAM before it is initialized.
  In the sample application, areas of the SDRAM are used after the bus state controller (BSC) has been initialized by the HardwareSetup function. Please note that if non-initialized SDRAM is used, errors in operation will occur.

- Do not locate the S section (i.e. the stack area) in SDRAM.
  The value set in the table for reset vectors (last address of the S section + 1) is set as the initial value of the stack pointer. Although there is no problem for the sample application since the S section is in on-chip RAM, if the S section had been placed in SDRAM, access to non-initialized SDRAM would be made when functions of the initialization program are called.

- Do not access the static variable area before execution of the INITSCT function.
  Execution of the INITSCT function initializes the static area for the C language. Please note that values are undefined for access before execution of the function.

- Do not place the image data area in a cache-enabled space.
  If the image data area (B_IMAGE_AREA section) is located in a cache-enabled space, data will not be correctly displayed on the LCD panel due to problems with coherence.

### 2.4.4 Sections

Table 7 gives allocation of sections which have been applied in the sample program.

**Table 7 Allocation of Sections**

| Section Name | Application of Section | Allocation Address | Address Space |
|---|---|---|---|
| DVECTTBL | Table for reset vector | H'0000 0000 | CS0 space (Cache-enabled) |
| DINTTBL | Table for interrupt vectors | | |
| PResetPRG | Reset program | H'0000 0800 | |
| PIntPRG | Interrupt function | | |
| P | Program area (in cases where no different specification is made) | H'0000 1000 | |
| C | Constant area | | |
| C$BSEC | Address structure for non-initialized data | | |
| C$DSEC | Address structure for initialized data | | |
| D | Initialized data (initial value) | H'203F F000 | CS0 space (Flash) (Cache-disabled) |
| PCACHE | Program area (cache disabled space) | | |
| B_IMAGE_AREA | Image data area (non-initialized data area) | H'2C00 0000 | CS3 space (SDRAM) (Cache-disabled) |
| B | Non-initialized data area | | |
| RINTTBL | Table for interrupt vector | H'FFF8 0000 | On-chip RAM |
| R | Initialized-data area | | |
| S | Stack area | H'FFF8 FC00 | |

Note: For details on the settings, see the *SuperH RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package V.9.01 User's Manual* (REJ10J1571)

## 2.5 Operation of the Sample Program

The initialization program consists of several source files, including resetprg.c, which includes the PowerON_Reset_PC function that is executed after power is supplied, and hwsetup.c, which includes hardware initialization functions. An overview of the configuration of the main source files follows.

Figure 8 shows the flow of processing by the reset program, figure 9 shows the flow of processing by hardware initialization functions, figure 10 shows the flow of processing by the “main” function, figures 11, 12 and 13 show the flow for initialization of the LCDC, and figure 14 shows the flow for the setting of color patterns. Furthermore, figures 15 and 16 show the flow for terminating and starting display control by the LCDC, respectively.

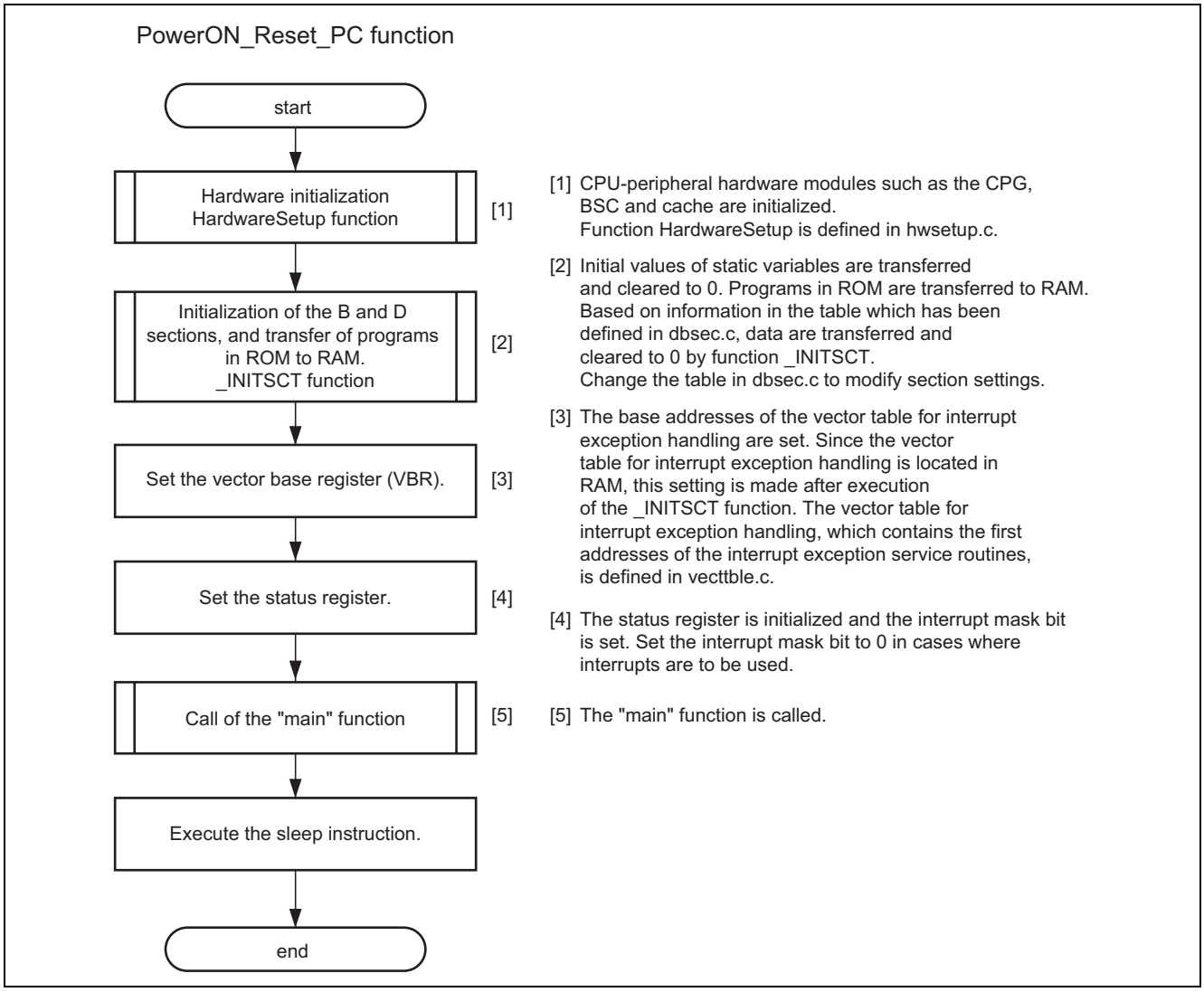


**Figure 8 Flow of Processing by the Reset Program**

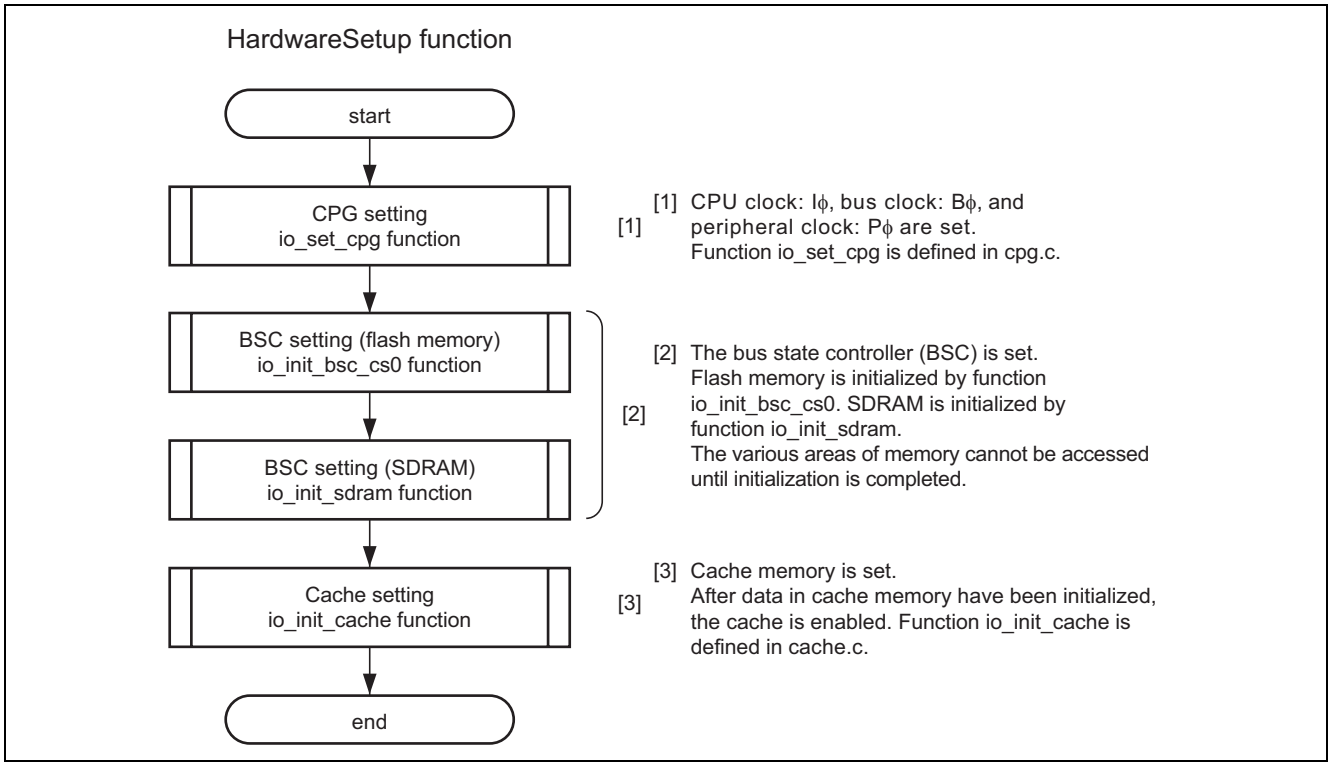


**Figure 9 Flow of Processing by Hardware Initialization Function**

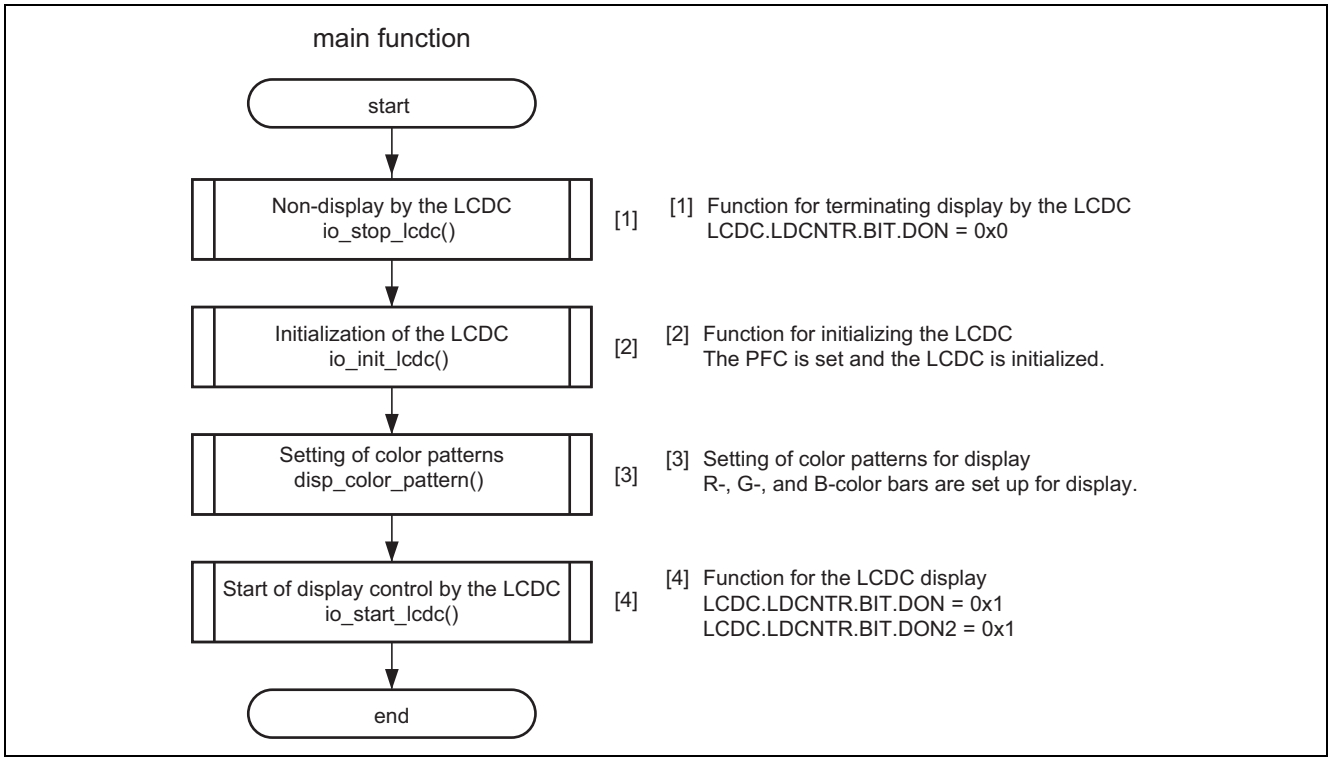


**Figure 10 Flow of Processing by the “main” Function**

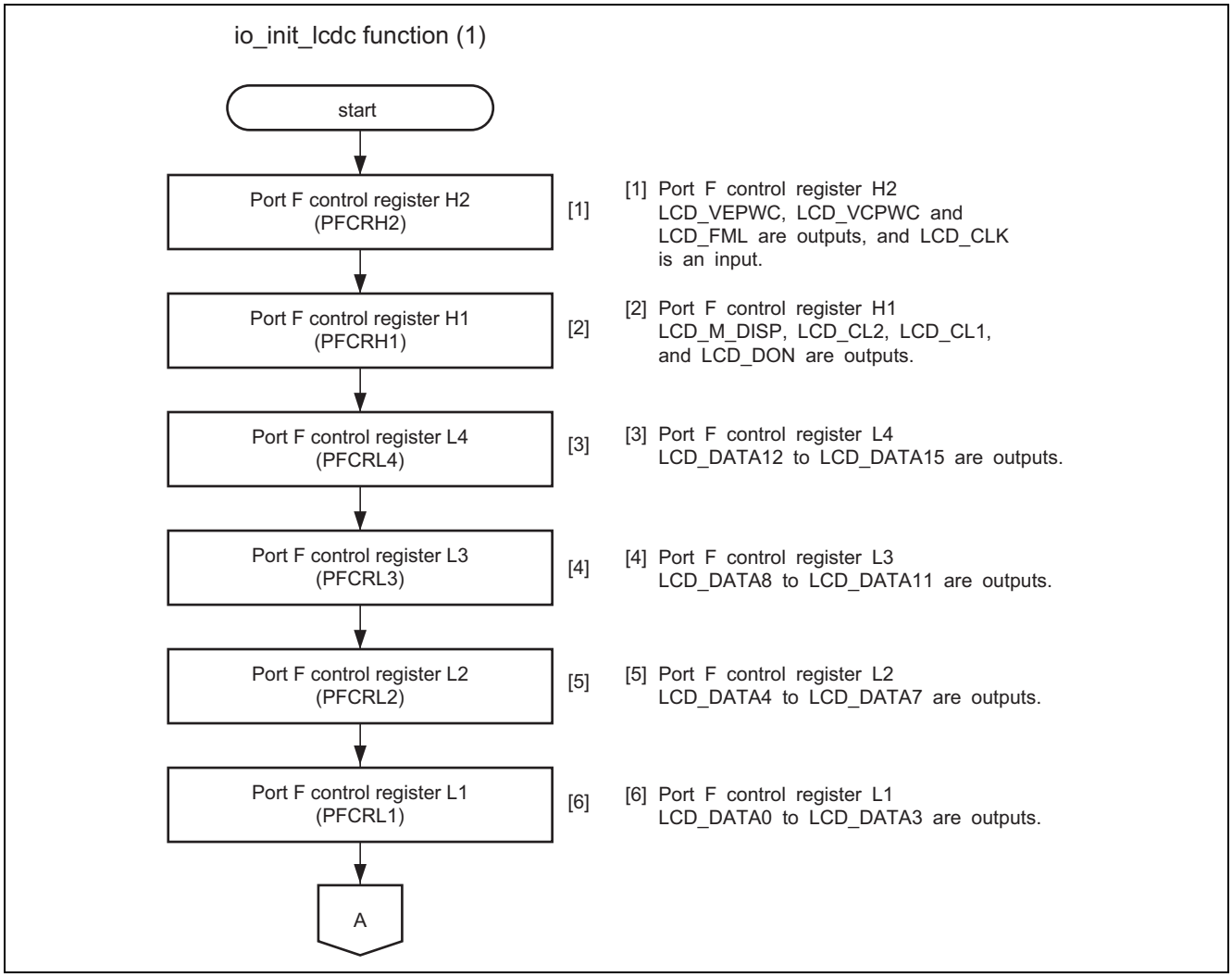


**Figure 11 Flow for Initialization of the LCDC (1)**

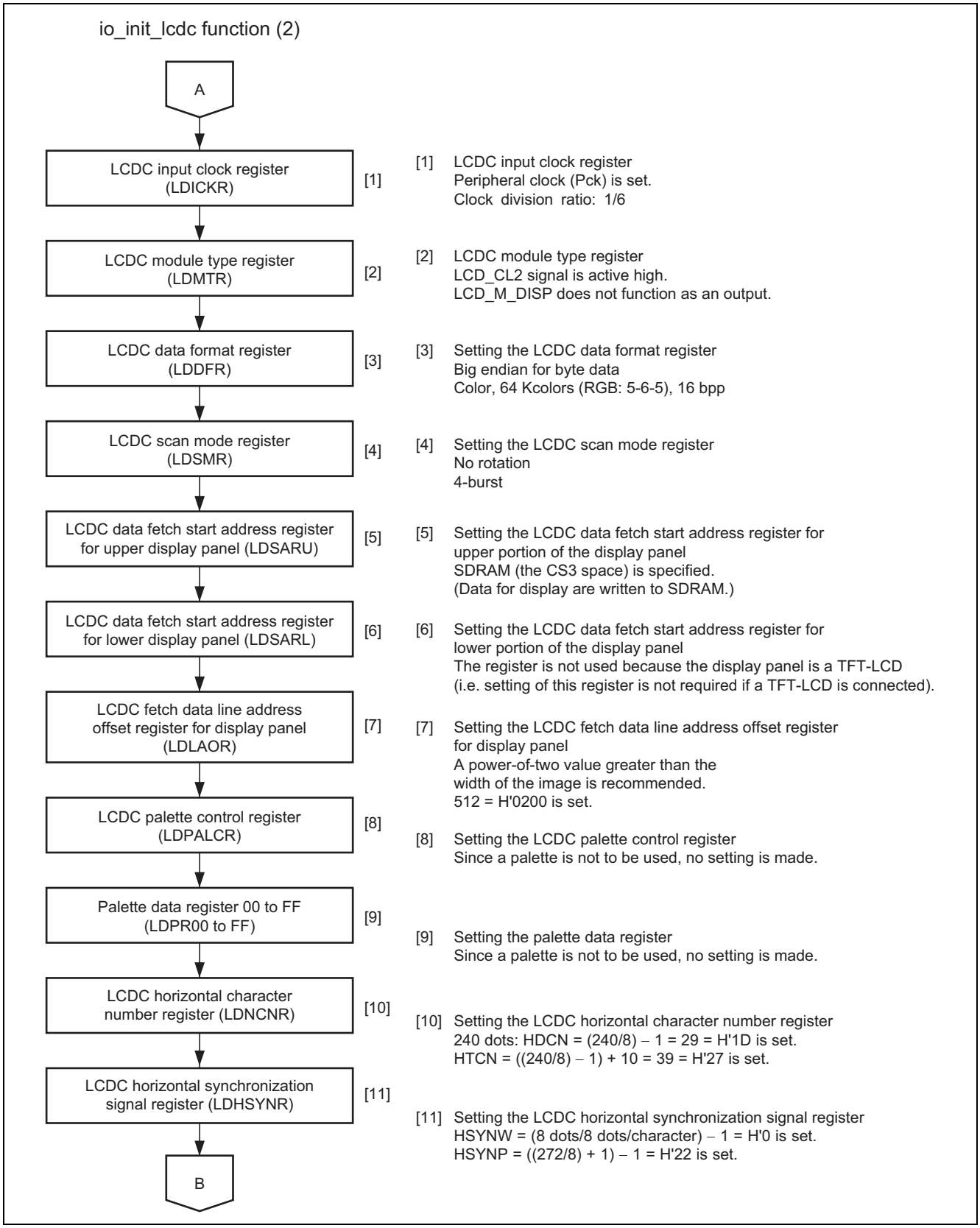


**Figure 12 Flow for Initialization of the LCDC (2)**

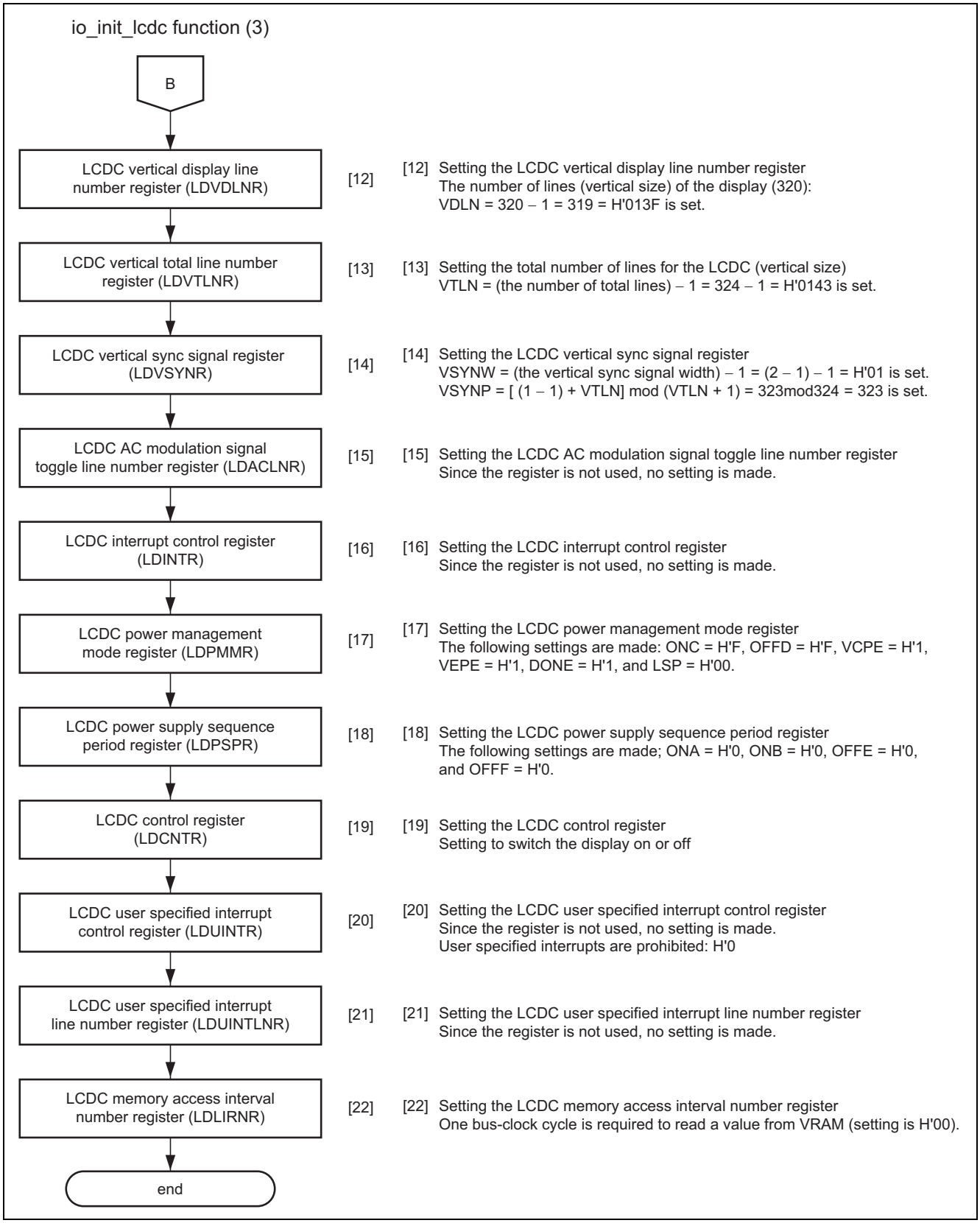


**Figure 13 Flow for Initialization of the LCDC (3)**

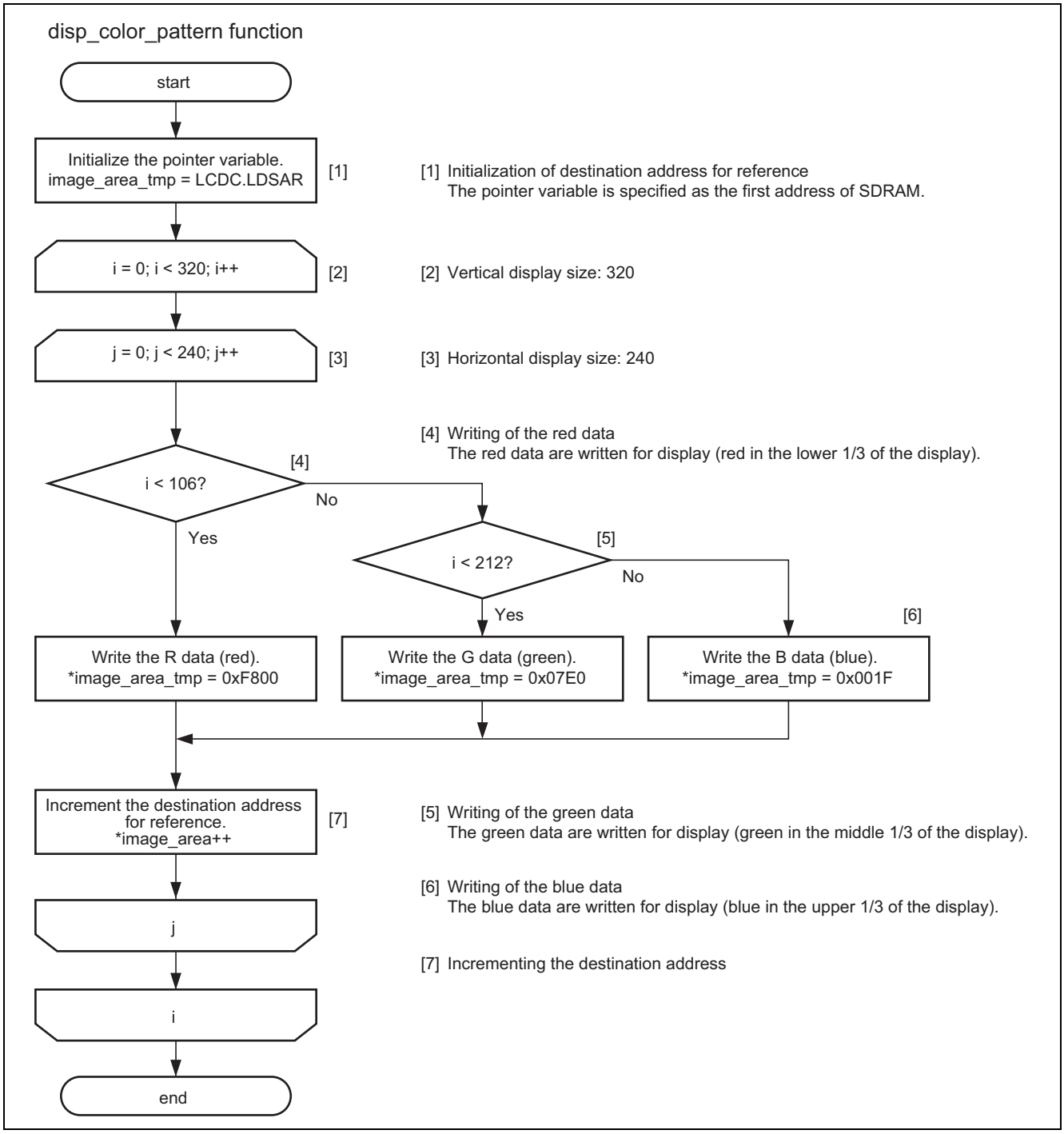


**Figure 14 Flow for the Setting the Color Patterns**

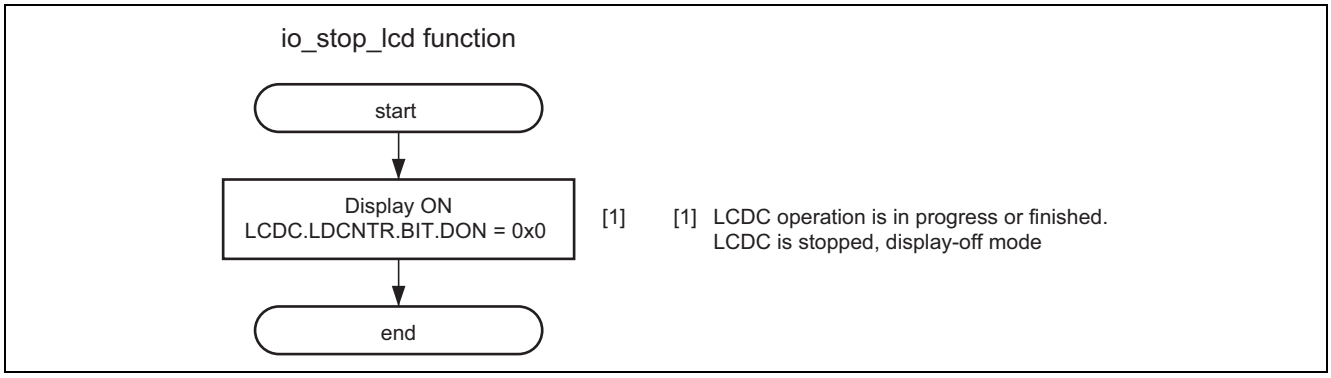


**Figure 15 Flow for Terminating Display Control by the LCDC**

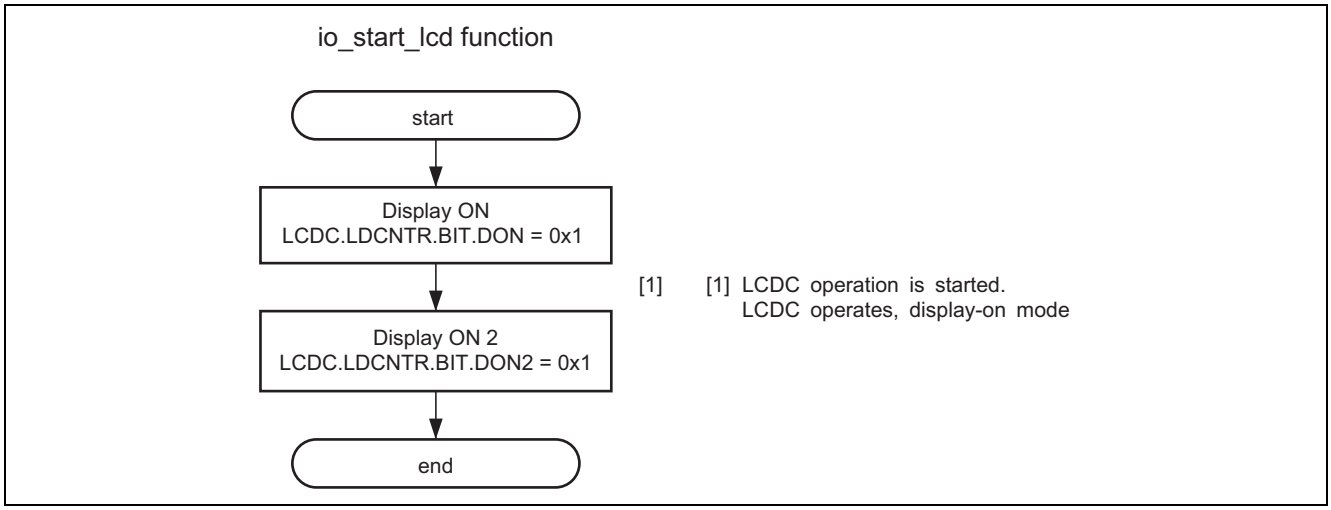


**Figure 16 Flow for Starting Display Control by the LCDC**

## 2.6 Register Settings Used in Sample Program

### 2.6.1 Modules (CPG, BSC, PFC)

Table 8 lists register settings for individual modules other than the LCDC.

**Table 8 Register Settings for Individual Modules**

| Module | Description | Setting Value |
|---|---|---|
| CPG | Internal clock: 200 MHz<br>Bus clock: 66 MHz<br>Peripheral clock: 33 MHz | FRQCR = H'1104 |
| BSC | CS0 space (flash memory) | |
| | • Specifies the idle period between writing and reading, and between writing and writing: 1 cycle<br>• Specifies the data bus width: 16 bits | CS0BCR = H'1000 0400 |
| | • Cycles of delay for assertion: 1.5<br>• Access wait cycles: 5<br>• Cycles of delay for negation: 1.5 | CS0WCR = H'0000 0AC1 |
| | CS3 space (SDRAM) | |
| | • Specifies memory: SDRAM<br>• Specifies the data bus width: 16 bits | CS3BCR = H'0000 4400 |
| | • Cycles of waiting for pre-charge: 1<br>• Wait cycles from the ACTV command to READ or Write command: 2<br>• CAS latency: 2 cycles<br>• Cycles of waiting for pre-charge activation: 2<br>• Cycles for the REF command or release from self-refresh: 5 | CS3WCR = H'0000 2892 |
| | • Refresh control (refreshing proceeds): Auto-refresh<br>• Bank active mode: Auto-precharge<br>• Number of row address bits for area 3: 12<br>• Number of column address bits for area 3: 9 | SDCR = H'0000 0809 |
| | • Clock select: Bϕ/16<br>• Refresh count: 1 time | RTCSR = H'A55A 0010 |
| | Refresh interval: 65 (0x41) cycles/refresh | RTCOR = H'A55A 0041 |
| | AC characteristics switching: Switching is performed and delay time is extended. | RTCSR = H'A55A 0010 |
| PFC | Settings for address bus, data bus, and LCD control pins for use in the CS0 to CS3 spaces | |
| | LCDC pins: LCD_DATA15 to LCD_DATA0 | PFCRH2 = H'2222 |
| | LCD_DON | PFCRH1 = H'2222 |
| | LCD_CLK, LCD_CK1, LCD_CK2 | PFCRL4 = H'2222 |
| | LCD_M_DISP | PFCRL3 = H'2222 |
| | LCD_FLM | PFCRL2 = H'2222 |
| | LCD_VCPWC, LCD_VEPWC | PFCRL1 = H'2222 |
| | External memory pins: $\overline{CS3}$ | PCCRL4 = H'0011 |
| | CKE | PCCRL3 = H'0011 |
| | RAS, CAS | PCCRL2 = H'0011 |
| | RD/$\overline{WR}$ | PCCRL1 = H'1010 |
| | $\overline{WE0}$, $\overline{WE1}$ | PECRL1 = H'0100 |

### 2.6.2 LCD Controller

Tables 9 to 14 list register settings for the LCDC.

**Table 9 Register Configuration (1)**

| Register Name | Bit Name | Address | Setting Value | Description |
|---|---|---|---|---|
| LDICKR | ICKSEL[1:0] | H'FFFF FC00 | H'1006 | Input clock select<br>B'01: Peripheral clock is selected |
| | DCDR[5:0] | | | Clock division ratio<br>B'000110: 1/6 (5.5 MHz) |
| LDMTR | FLMPOL | H'FFFF FC02 | H'C02B | FLM (vertical sync signal) polarity select<br>B'1: LCD_FLM pulse is low active |
| | CL1POL | | | CL1 (horizontal sync signal) polarity select<br>B'1: LCD_CL1 pulse is low active |
| | DISPPOL | | | DISP (display enable) polarity select<br>B'0: LCD_M_DISP is high active |
| | DPOL | | | Display data polarity select<br>B'0: LCD_DATA is high active, transparent-type LCD panel |
| | MCNT | | | M Signal control<br>B'0: M (AC line modulation) signal is output |
| | CL1CNT | | | CL1 (horizontal sync signal) control<br>B'0: CL1 is output during vertical retrace period |
| | CL2CNT | | | CL2 (dot clock of LCD module) control<br>B'0: CL2 is output during vertical and horizontal retrace periods |
| | MIFTYP[5:0] | | | Module interface type select<br>B'101011: Color TFT for a 16-bit data bus |
| LDDFR | PABD | H'FFFF FC04 | H'002D | Byte data pixel alignment<br>B'0: Big endian for byte data |
| | DSPCOLOR [6:0] | | | Display color select<br>B'0101101: Color, 64 Kcolors (R-G-B: 5-6-5), 16 bpp |
| LDSMR | ROT | H'FFFF FC06 | H'0000 | Rotation module select<br>B'0: Not rotated |
| | AU[1:0] | | | Access unit select<br>B'00: 4-burst |
| LDSARU | SAU25 to SAU4 | H'FFFF FC08 | H'0C00 0000 | Start address for upper display data fetch<br>H'0C00 0000:<br>The start address for data fetch of the display data must be set within the synchronous DRAM area of area 3. |
| LDSARL | SAL25 to SAL4 | H'FFFF FC0C | — | Start address for lower panel display data fetch<br>TFT: Cannot be used<br>The start address for data fetch of the display data must be set within the synchronous DRAM area of area 3. |
| LDLAOR | LAO15 to LAO0 | H'FFFF FC10 | H'0200 | Line address offset<br>256 × 2 = H'0200<br>A power-of-two greater than the width of the image (240 pixels in this sample application) is recommended. Since the recommended value is set, the setting is 512. |

**Table 10 Register Configuration (2)**

| Register Name | Bit Name | Address | Setting Value | Description |
|---|---|---|---|---|
| LDPALCR | PALS | H'FFFF FC12 | H'0000 | Palette state<br>B'0: Display mode: LCDC uses the palette |
| | PALEN | | | Palette read/write enable<br>B'0: Request for transition to normal display mode |
| LDPR00 to LDPRFF | PALDnn23 to PALDnn0 | H'FFFF F800 to H'FFFF FBFC | — | Palette data<br>Since a palette is not to be used, no setting is made. |
| LDHCNR | HDCN7<br>HDCN6<br>HDCN5<br>HDCN4<br>HDCN3<br>HDCN2<br>HDCN1<br>HDCN0 | H'FFFF FC14 | H'1D20 | Horizontal display character number<br>Setting for the number of horizontal display characters (unit: character = 8 dots)<br>Since the width of the panel in this sample application is 240 pixels, the setting is as follows:<br>HDCN = (the number of display characters) – 1<br>= (240/8) – 1 = 29 = H'1D. |
| | HTCN7<br>HTCN6<br>HTCN5<br>HTCN4<br>HTCN3<br>HTCN2<br>HTCN1<br>HTCN0 | | | Horizontal total character number<br>Setting for the number of total horizontal characters (unit: character = 8 dots)<br>The minimum horizontal retrace period is three characters (24 dots). In this sample program, the horizontal retrace period is set to 10 characters (80 dots).<br>Setting is made as follows;<br>HTCN = [ (240/8) – 1] + 3 = 32 = H'20. |
| LDHSYNR | HSYNW3<br>HSYNW2<br>HSYNW1<br>HSYNW0 | H'FFFF FC16 | H'0022 | Horizontal sync signal width<br>Setting for the width of the horizontal sync signals (CL1 and Hsync) (unit: character = 8 dots)<br>HSYNW = (horizontal sync signal width) – 1 = (8 dots/8 dots/character) – 1 = 0 |
| | HSYNP7<br>HSYNP6<br>HSYNP5<br>HSYNP4<br>HSYNP3<br>HSYNP2<br>HSYNP1<br>HSYNP0 | | | Horizontal sync signal output position<br>Setting for the output position of the horizontal sync signals (unit: character = 8 dots)<br>Specify the value of (horizontal sync signal output position) – 1.<br>HSYNP = [(272/8) + 1] – 1 = H'22 |
| LDVDLNR | VDLN10<br>VDLN9<br>VDLN8<br>VDLN7<br>VDLN6<br>VDLN5<br>VDLN4<br>VDLN3<br>VDLN2<br>VDLN1<br>VDLN0 | H'FFFF FC18 | H'013F | Vertical display line number<br>Setting for the number of vertical display lines (unit: line)<br>Specify the value of (line number for display) – 1.<br>VDLN = 320 – 1 = H'013F |

**Table 11 Register Configuration (3)**

| Register Name | Bit Name | Address | Setting Value | Description |
|---|---|---|---|---|
| LDVTLNR | VTLN10 | H'FFFF FC1A | H'0143 | Vertical total line number |
| | VTLN9 | | | Setting for the total number of vertical display lines (unit: line) |
| | VTLN8 | | | Specify the value of (the number of total line) – 1. |
| | VTLN7 | | | The minimum for the total number of vertical lines is 2 lines. The following conditions must be satisfied: VTLN ≥ VDLN, VTLN ≥ 1. |
| | VTLN6 | | | VDLN = 324 – 1 = H'0143 |
| | VTLN5 | | | |
| | VTLN4 | | | |
| | VTLN3 | | | |
| | VTLN2 | | | |
| | VTLN1 | | | |
| | VTLN0 | | | |
| LDVSYNR | VSYNW3 | H'FFFF FC1C | H'1143 | Vertical sync signal width |
| | VSYNW2 | | | Setting for the width of the vertical sync signals (FLM and Vsync) (unit: line) |
| | VSYNW1 | | | Specify the value of (the vertical sync signal width) – 1. |
| | VSYNW0 | | | Since the vertical sync signal width is two lines, the setting is as follows; VSYNW = (2 – 1) = H'01. |
| | VSYNP10 | | | Vertical sync signal output position |
| | VSYNP9 | | | Setting for the output position of the vertical sync signals (FLM and Vsync) (unit: line) |
| | VSYNP8 | | | Specify the value of (vertical sync signal output position) – 2. |
| | VSYNP7 | | | DSTN should be set to an odd number value. It is handled as (setting value + 1) / 2. |
| | VSYNP6 | | | For an 320-line LCD module and a vertical retrace period of 0 lines (in other words, VTLN = 323 and the vertical sync signal is active for the first line): |
| | VSYNP5 | | | Single display |
| | VSYNP4 | | | VSYNP = [ (1 – 1) + VTLN] mod (VTLN + 1) |
| | VSYNP3 | | | = [ (1 – 1) + 323] mod (324 + 1) |
| | VSYNP2 | | | = 323mod324 = 323 = H'143 |
| | VSYNP1 | | | |
| | VSYNP0 | | | |
| LDACLNR | ACLN4 | H'FFFF FC1E | — | AC line number |
| | ACLN3 | | | Settings for the numbers of lines where the LCD current alternating signal of the LCD module is toggled (unit: line). |
| | ACLN2 | | | Specify the value of (line number for toggling) – 1. |
| | ACLN1 | | | This is not used in the sample application. |
| | ACLN0 | | | |

**Table 12 Register Configuration (4)**

| Register Name | Bit Name | Address | Setting Value | Description |
|---|---|---|---|---|
| LDINTR | MINTEN | H'FFFF FC20 | H'0000 | Memory access interrupt enable<br>B'0: Disables an interrupt generation |
| | FINTEN | | | Frame end interrupt enable<br>B'0: Disables an interrupt generation |
| | VSINTEN | | | Vsync starting point interrupt enable<br>B'0: Disables an interrupt generation |
| | VEINTEN | | | Vsync ending point interrupt enable<br>B'0: Disables an interrupt generation |
| | MINTS | | | Memory access interrupt state<br>Indicates the memory access interrupt handling state. |
| | FINTS | | | Flame end interrupt state<br>Indicates the flame end interrupt handling state. |
| | VSINTS | | | Vsync start interrupt state<br>Indicates the LCDC's Vsync start interrupt handling state. |
| | VEINTS | | | Vsync end interrupt state<br>Indicates the LCDC's Vsync end interrupt handling state. |
| LDPMMR | ONC3<br>ONC2<br>ONC1<br>ONC0 | H'FFFF FC24 | H'FF70 | LCDC power-on sequence period<br>Set the period from LCD_VEPWC assertion to LCD_DON assertion in the power-on sequence of the LCD module in frame units.<br>Specify the value of (the period) – 1.<br>For details, see the figures “Power Supply Control Sequence and States of the LCD Module” in the *SH7263 Group Hardware Manual* (REJ09B0290). |
| | OFFD3<br>OFFD2<br>OFFD1<br>OFFD0 | | | LCDC power-off sequence period<br>Set the period from LCD_DON negation to LCD_VEPWC negation in the power-off sequence of the LCD module in frame units.<br>Specify the value of (the period) – 1.<br>For details, see the figures “Power Supply Control Sequence and States of the LCD Module” in the *SH7263 Group Hardware Manual* (REJ09B0290). |
| | VCPE | | | LCD_VCPWC pin enable<br>B'1: Sets whether or not to enable a power-supply control sequence using the LCD_VCPWC pin. |
| | VEPE | | | LCD_VEPWC pin enable<br>B'1: Sets whether or not to enable a power-supply control sequence using the LCD_VEPWC pin. |
| | DONE | | | LCD_DON pin enable<br>B'1: Sets whether or not to enable a power-supply control sequence using the LCD_DON pin. |
| | LPS[1:0] | | | LCD module power-supply input state<br>B'00: Indicates the power-supply input state of the LCD module when using the power-supply control function. |

**Table 13 Register Configuration (5)**

| Register Name | Bit Name | Address | Setting Value | Description |
|---|---|---|---|---|
| LDPSPR | ONA3<br>ONA2<br>ONA1<br>ONA0 | H'FFFF FC26 | H'0000 | LCDC power-on sequence period<br>Set the period from LCD_VCPWC assertion to starting output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) in the power-on sequence of the LCD module in frame units.<br>Specify the value of (the period) – 1. |
| | ONB3<br>ONB2<br>ONB1<br>ONB0 | | | LCDC power-on sequence period<br>Set the period from starting output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) to the LCD_VEPWC assertion in the power-on sequence of the LCD module in frame units. Specify the value of (the period) – 1. |
| | OFFE3<br>OFFE2<br>OFFE1<br>OFFE0 | | | LCDC power-off sequence period<br>Set the period from LCD_VEPWC negation to stopping output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) in the power-off sequence of the LCD module in frame units.<br>Specify the value of (the period) – 1. |
| | OFFF3<br>OFFF2<br>OFFF1<br>OFFF0 | | | LCDC power-off sequence period<br>Set the period from stopping output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) to LCD_VCPWC negation in the power-off sequence of the LCD module in frame units.<br>Specify the value of (the period) – 1. |
| LDCNTR | DON2 | H'FFFF FC28 | In operation: H'0011<br>Not in operation: H'0000 | Display on 2<br>Specifies the start of the LCDC display operation.<br>0: LCDC is being operated or stopped<br>1: LCDC starts operation<br>When this bit is read, it is always read as 0. Only write 1 to this bit to start display operation. Do not write any value to this bit other than to start display operation. |
| | DON | | | Display on<br>Specifies the start and stop of the LCDC display operation. The control sequence state can be checked by referencing the LPS[1:0] of LDPMMR.<br>0: Display-off mode: LCDC is stopped<br>1: Display-on mode: LCDC operates |

**Table 14 Register Configuration (6)**

| Register Name | Bit Name | Address | Setting Value | Description |
|---|---|---|---|---|
| LDUINTR | UINTEN | H'FFFF FC34 | H'0000 | User specified interrupt enable<br>B'0: LCDC user specified interrupt is not generated |
| | UINTS | | | User specified interrupt state<br>This bit is set to 1 at the time an LCDC user specified interrupt is generated (set state). During the user specified interrupt handling routine, this bit should be cleared by writing 0 to it. |
| LDUINTLNR | UINTLN10<br>UINTLN9<br>UINTLN8<br>UINTLN7<br>UINTLN6<br>UINTLN5<br>UINTLN4<br>UINTLN3<br>UINTLN2<br>UINTLN1<br>UINTLN0 | H'FFFF FC36 | — | User specified interrupt generation line number<br>Specifies the line in which the user specified interrupt is generated (line units). Set (line number for interrupt generation) – 1<br>When using the LCD module with STN/TFT display, the setting of this register should be equal to or lower than the vertical display line number (VDLN) in LDVDLNR. |
| LDLIRNR | LIRN7 to LIRN0 | H'FFFF FC40 | H'0000 | VRAM reading bus clock interval<br>Specify the number of bus-clock cycles for reading by the CPU/DMAC between burst bus cycles of reading of the VRAM for the LCDC.<br>H'00: One bus clock cycle |

## 3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual (REJ09B0051)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7263 Group Hardware Manual (REJ09B0290)
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