

# IGBT, FRD

How to use the PLECS model

## Introduction

This document describes the usage and precautions for the PLECS model using an our product combination of RJP6831JWS and RJU6832JWS as an example.

# Contents

How to use the model	2
Library Browser	. 2
Precautions for using the model	3
Combination of IGBT and FRD	. 3
Simulation Parameters	. 3
	How to use the model Library Browser Precautions for using the model Combination of IGBT and FRD Simulation Parameters



#### 1. How to use the model

# 1.1 Library Browser

After the PLECS model is installed, "Renesas Component - date" is added as a category to the library browser as shown in Figure 1-1, and product models can be selected from the subcategory "RJP6831\_RJU6832".

Library Browse		-		×
Q Search componen				
<ul> <li>&gt; System</li> <li>&gt; Assertions</li> <li>&gt; Control</li> <li>&gt; Electrical</li> <li>&gt; Thermal</li> <li>&gt; Magnetic</li> <li>&gt; Mechanical</li> <li>&gt; PI ECS RT Box</li> <li>&gt; Renesas Component</li> <li></li></ul>	1t - Jul5th2024 31_RJU6832			
Low Switching loss Easy paralleling by inte AEC Q101 (HTRB, HT [RJU6832JWS Feature Fast Recovery Diode t Low Forward voltage VF = 1.5 V typ. (at IF = AEC Q101 (HTRB) qua (Applications) Hybrid and electric vel	BB) qualified Is] echnology : 300 A, Tj = 25 ° C) lified	aturation vo	Itage	. Tj = 25

Figure 1-1 Renesas Component Library



# 2. Precautions for using the model

## 2.1 Combination of IGBT and FRD

Be sure to use RJP6831JWS and RJU6832JWS in combination as shown in Figure 2-1

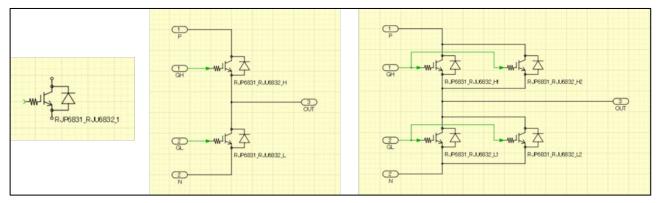


Figure 2-1 The example of model Combinations

#### 2.2 Simulation Parameters

For simulation parameters, the setting of voltage, current, and other simulation conditions, please refer to the datasheet for ratings and recommended values.

The simulation parameters for this device are as follows (Fig. 2-2)

Gate resistance (on)					
Gate resistance (off)					
Initial Temperature					

RJP6831_RJU	16832 (mask	) (link)		
[RJP6831 JM3 750 V Tren Low collect VCE(sat) = Low Switch Easy paralle AEC Q101 ( [RJU6832 JM3 Fast Recove Low Forwar	S Features] ch & field st or to emitte = 1.4 V typ. ing loss ling by intern HTRB, HTC S Features] ery Diode te d voltage ( typ. (at IF HTRB) quai	op high AE4 tech r saturation volta; (at IC = 300 A, Vi nal Rg (B) qualified chnology = 300 A, Tj = 25 ified	ge GE = 15 V, Tj = 25	• c)
Parameters Gate resistan	Assertion ce (on):	ns		
Gate resistan 5.6	ce (on):	าร		
Gate resistan 5.6 Gate resistan	ce (on):	ns		
Gate resistan 5.6 Gate resistan 5.6	ce (on): ce (off):	ns		
Gate resistan 5.6 Gate resistan	ce (on): ce (off):	ns		
Gate resistan 5.6 Gate resistan 5.6 Initial tempera	ce (on): ce (off):	ns		

**Figure 2-2 Simulation Parameters** 



#### **Revision History**

		Description		
Rev.	Date	Page	Summary	
1.00	Jul.17.24	-	First edition	



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