Application Note

Industrial Ethernet PHY

Layout recommendations and design rules

Dual PHY ASSP

uPD60620,
uPD60620A,
uPD60621A

Renesas Electronics
www.renesas.com

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(1) List of Abbreviations and Acronyms

Abbreviation	Full Form
AGND	Analogue Ground
ASSP	Application Specific Standard Product
DGND	Digital Ground
FGND	Frame Ground
GND	Ground
IO	Input - Output
LED-MUX	LED Multiplexing
MAC	Media Access Control
MDI	Media Dependent Interface
MII	Media Independent Interface
PD	Pull-Down
PHY	Physical Layer
PU	Pull-Up
RMS	Root Mean Square
UM	User's Manual

Table of Contents

Chapter 1 General Information

UPD60620/21 is a dual port Ethernet physical layer device for 10Base-T100Base-TX and 100Base-FX operation.

This application note is complementary material to the following documents. Please read these documents for further information.

- Industrial Ethernet PHY - Dual PHY ASSP User Manual
  R19UH0083EDxxxx
- Industrial Ethernet PHY – Programming Guide
  R19AN0010EDxxxx

Note:
xxxx – version number

Chapter 2 Strap Options

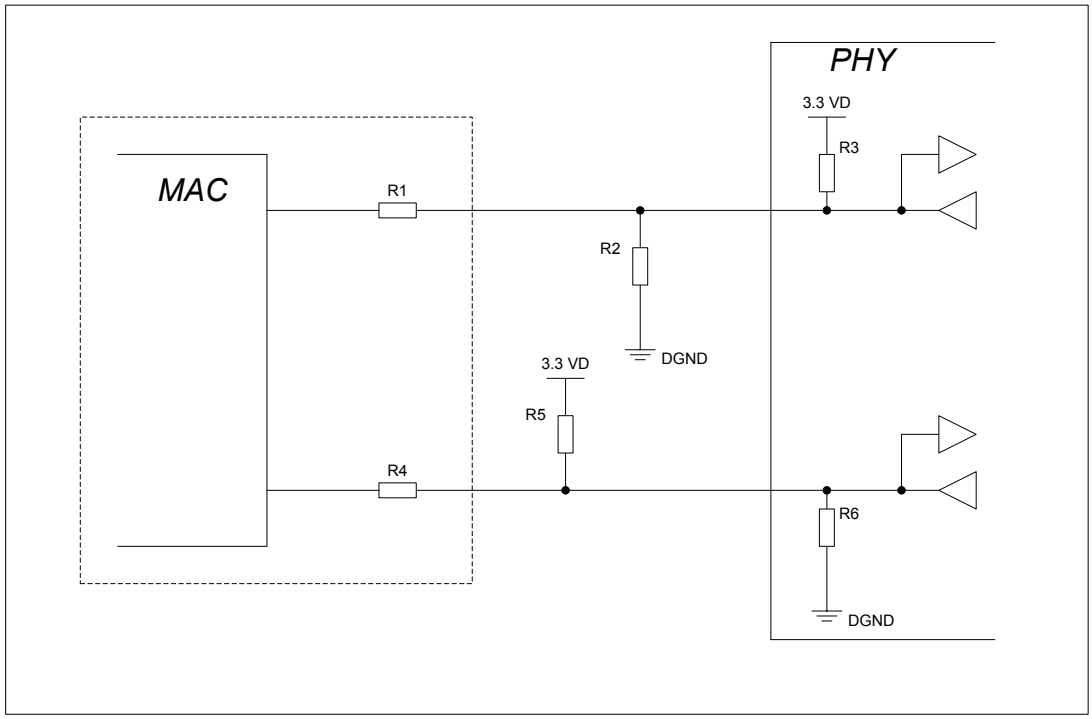
The Ethernet PHY ASSP provides the opportunity to set initial start-up configurations by external strap pin configuration. These strap options are read during power-up or hardware reset (resetb).

The strap pins are normal port pins that have only during the start-up phase the strap option functionality. The strap configuration is realized by a pull-up or pull-down resistance. Every strap pin has a default setting that is set by an internal 40kΩ resistance. To set an external strap-pin configuration a resistor of about 4kΩ should be used. In a noisy environment it is recommended to connect every strap-pin to an external pull-up/-down irrespective to its internal configuration.

An example of a schematic for two different strap-pin ports is shown in figure 2-1 with the related parts in table 2-1.

Table 2-2 lists all strap-pins and its functions. In Table 2-3 additional strap modes are described.

Figure 2-1 Schematic example for pull-up and pull-down configuration at a strap pin



Note: The dashed box includes the MII related circuit parts. See also chapter 4.

Table 2-1 Part list – strap option example

Part	Type	Characteristics	Recommended components
R1, R4	Resistor	10Ω	
R2, R5	Resistor	~ 3.9 kΩ	
R3, R6	Internal resistance	~ 40 kΩ	

Table 2-2 Strap options

Pin Name	Function	Default value
P1RXD1	0: Autonegotiation disabled, 100BaseT 1: Autonegotiation enabled, 100BaseT	1, PU
P1RXD0	If Autonegotiation disabled: 0: Half Duplex 1: Full Duplex If Autonegotiation enabled: 0: Parallel detect ends in half duplex mode 1: Forced Full Duplex in parallel detect *See also special strap modes in table 2-3*	1, PU
P1RXCLK	0: Disable Quick Autonegotiation 1: Quick Autonegotiation, shortest times (Autonegotiation required) *See also special strap modes in table 2-3*	1, PU
P0RXERR	0: Configure RMII Interface 1: Configure MII Interface	1, PU
P1RXERR	0: Standard Mode, “JK” required for Start of Frame detection 1: Fast Mode, Only “J” required for Start of Frame detection	1, PU
P0RXCLK	0: AUTOMDI-X disabled. 1: AUTOMDI-X enabled	1, PU
P0RXDV	0: FX Mode for PHY0, in this case the values of Autonegotiation, Duplex are ignored for this PHY. 1: TX Mode for PHY0	1, PU
P1RXDV	0: FX Mode for PHY1, in this case the values of Autonegotiation, Duplex are ignored for this PHY. 1: TX Mode for PHY1	1, PU
P0RXD0 / P0RXD1	Configures the upper two bits N and M of the PHY addresses 00: device uses address 00xxx for SMI 01: device uses address 01xxx for SMI 10: device uses address 10xxx for SMI 11: device uses address 11xxx for SMI	00, PD
P1TXCLK*	0: Synchronous mode for TXCLK. TXCLK is synchronous to XCLK0. This must be used for MACs that supply the MII TX data synchronously to the XCLK0 signal. 1: Asynchronous mode for TXCLK. This mode reduces the TX Latency, but requires a MAC that handles the TXCLK signal to supply the MII TX data. This is the typical bahaviour.	1, PU

To configure the PHY via strap pins to special modes unusual combinations of the strap pins are used. The PHY modes are shown and described in table 2-3.

Table 2-3 Special strap modes

Mode	Description	Strap combination
Special Isolate Mode	In this mode the PHYs will not set up a link unless programmed and enabled through the SMI	Autonegotiation OFF ➔ PD at P1RXD1 Quick Autonegotiation ON ➔ PU at P1RXCLK (default) Full Duplex ➔ PU at P1RXD0 (default)
Repeater* Mode	In this mode a channel to channel loopback is enabled. The data from the RX ports is forwarded to the TX port of the other channel. PHY configuration in repeater mode is 100BT FD.	Autonegotiation OFF ➔ PD at P1RXD1 Quick Autonegotiation ON ➔ PU at P1RXCLK (default) Full Duplex ➔ PD at P1RXD0

*This pin/function is available at uPD60620A and uPD60621A only

Chapter 3 Media Dependent Interface

This PHY device supports to two kinds of media interfaces:

- IEEE802.3 compliant twisted pair interface for 100Base-TX and 10Base-T operation.
- IEEE802.3 compliant optical media interface.

The start-up mode of the PHY can be set via strap pin configuration.

3.1 Differential Pair Routing

This chapter describes how to design the differential pairs between PHY and connector. Some general design rules for differential pair routing are given here. Furthermore some recommendations of the specific realization for the Ethernet PHY are described.

- Long wires should be avoided. The PHY, the transformer, and the connector should be placed together as close as possible.
- Crossing of differential traces with other lines and among each other should be avoided. The components should be placed that way that crossing of differential pairs of TxP/N and RxP/N is not necessary.
- Differential lines should be routed straight and as short as possible.
- Lines should bend with a 45 degree angle or less. (figure 3-1)
- Traces between PHY device, transformer and RJ45 connector should be designed with a differential impedance of 100Ω±10% and with an impedance of 50Ω related to GND.
- The traces of a differential pair should match in length. 0.5mm is the maximum deviation. Adjustments of the length should be done at the connector, device or transformer.
- Additional to the length the single traces should be designed symmetrical. They should be parallel and routed in the same layer with continuous width and a preferable fixed spacing. Components, vias and connections should also be symmetrical.
- Stubs should be avoided.
- Preferable is a large edge gap at differential pairs (‘g’ in figure 3-2). An empty space of five times of the trace width between differential pair and other signals, planes or components is recommended.
- Differential lines should not cross edges of the GND/supply plane, other planes or voids in the layer below. For continuous impedance a GND plane in the layer below is preferable.
- Beneath the magnetics no lines or planes should be routed.
- Preferable differential pairs should be routed via as little vias as possible. If vias are necessary please note the following:

- Vias of the related plane (e.g. AGND) should be placed near the signal vias. The distance between signal via and GND via should be equal to the distance between the layers to avoid a discontinuity of the impedance. (See ‘a’ in figure 3-3)
- Void and no planes between and around the signal vias (see figure 3-3). Metal of planes close to the differential vias could influence the impedance.
- The diameter of the vias should be almost equal to the trace width. (See ‘w’ in figure 3-3)

Figure 3-1 Trace corner of differential pairs

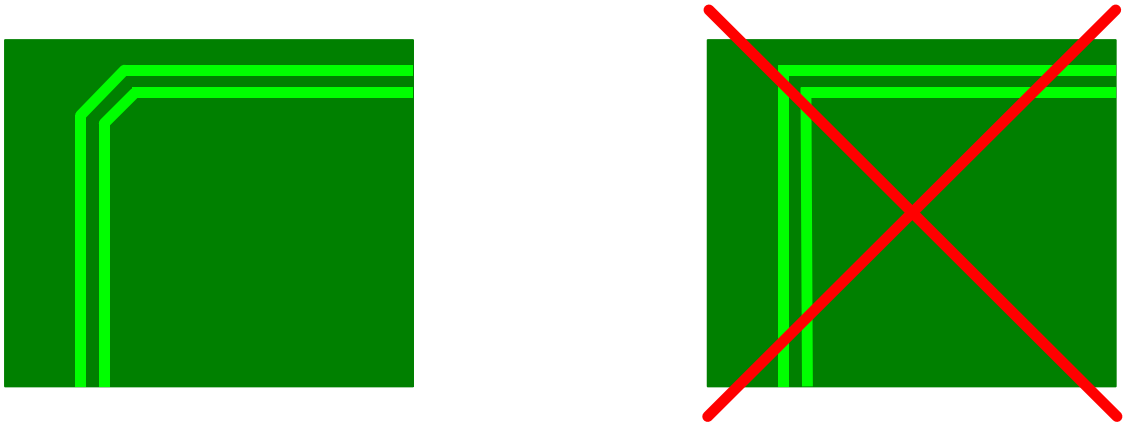


Figure 3-2 Differential pair traces

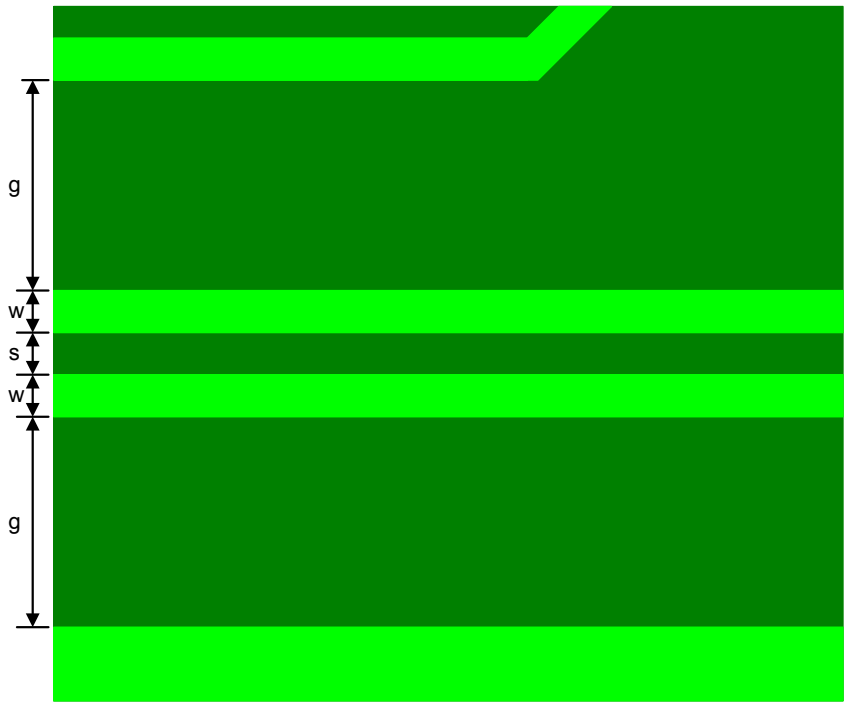
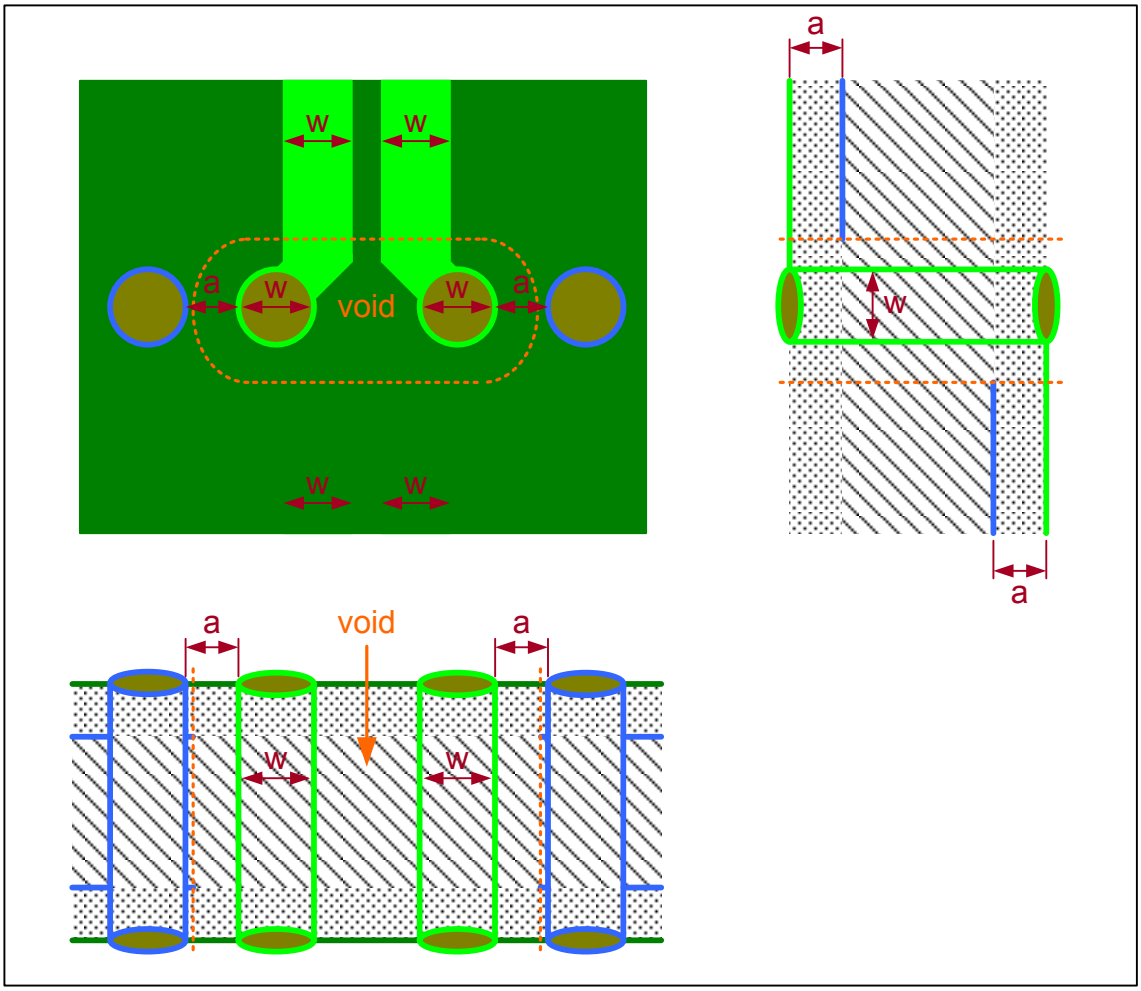


Figure 3-3 Vias for differential pairs



3.2 Twisted Pair Interface

Figure 3-4 and figure 3-5 show examples of twisted pair interface circuits with external and integrated magnetics. The following table 3-1 gives recommendations for values and parts. Additionally a layout example is given in figure 3-6 (Dimensions not true to scale).

Figure 3-4 Schematics for twisted pair interface circuit with external magnetics

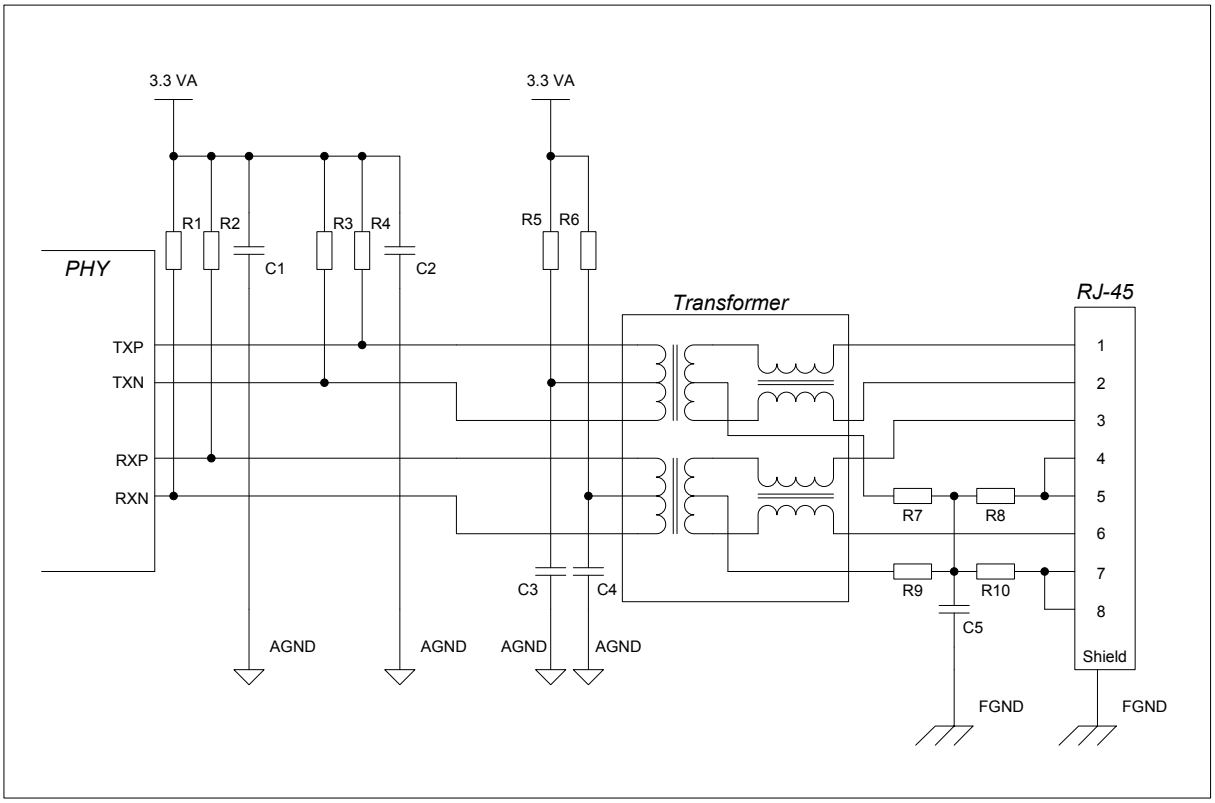


Figure 3-5 Schematics for twisted pair interface circuit with integrated magnetics

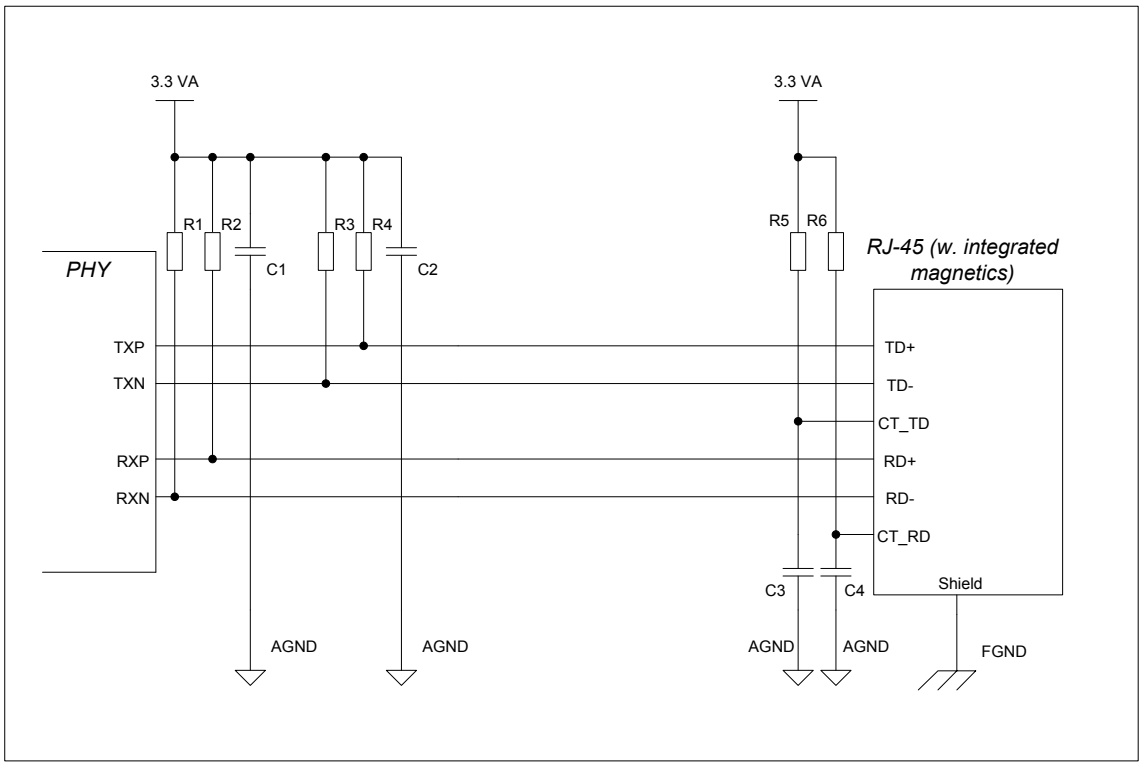


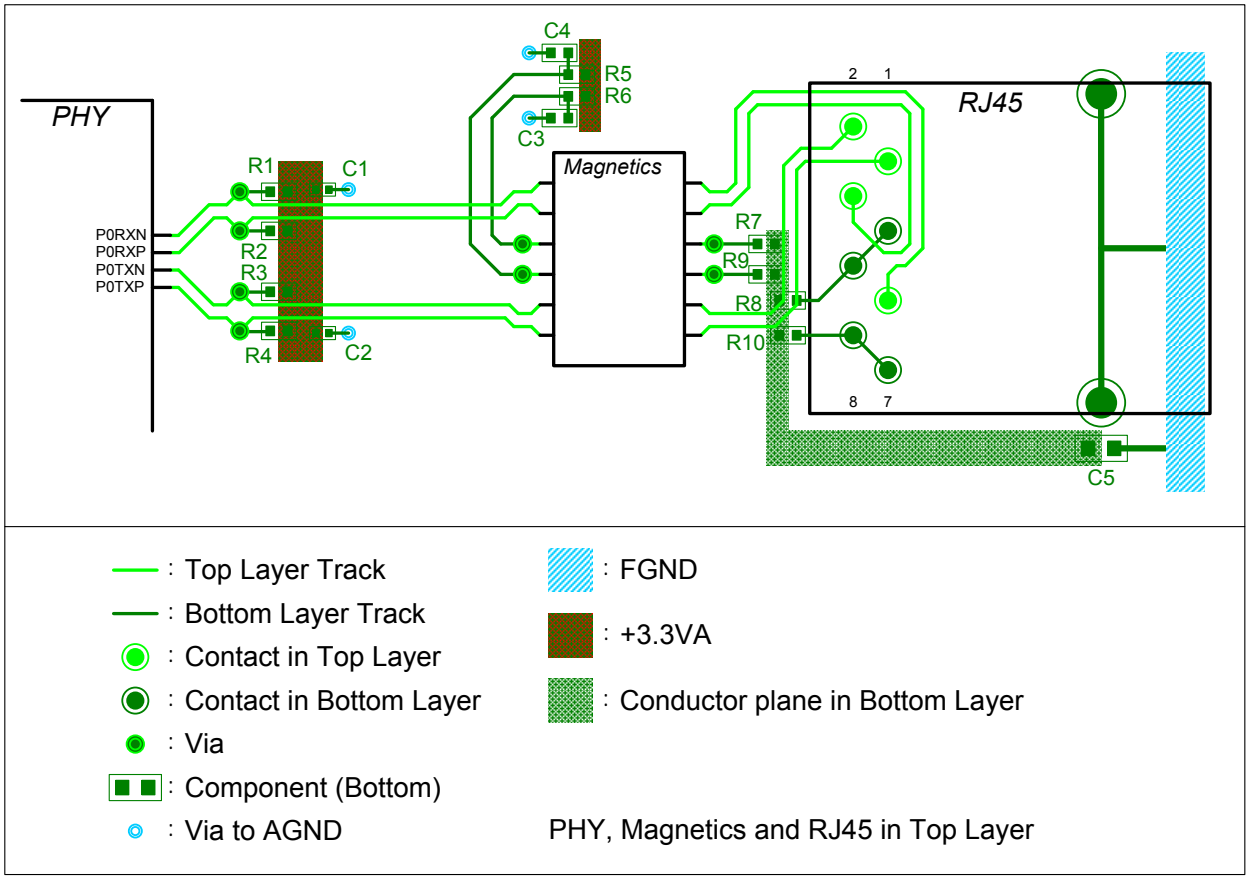
Table 3-1 Part list – TX Interface

Part	Type	Characteristics	Recommended components
R1, R2, R3, R4	Resistor	49.9Ω±1% 1/16W	
R5, R6	Resistor	10Ω±1% 1/16W	
R7, R8, R9, R10	Resistor	75Ω±1% 1/16W	
C1	Capacitor	10nF – 100nF	
C2	Capacitor	10nF – 100nF	
C3	Capacitor	10nF - 22nF	
C4	Capacitor	10nF - 22nF	
C5	Capacitor	4.7nF±10%	
Transformer		One channel	Pulse Engineering H1012NL, H1102NL
		Two channel	Pulse Engineering H1270NL, HX1294
RJ45 with integrated magnetics		One channel	Pulse Engineering J0011D21BNL

Notes:

- R1, R2, R3, R4, C1, C2 should be placed close to the PHY device
- R5, R6, C3, C4 should be placed close to the magnetics
- If an external transformer is used R8 and R10 should be placed next to the RJ45 connector
- The turns ratio of the transformer must be 1:1.
- The transformer should support AutoMDIX / MDIX if this function will be used by application

Figure 3-6 Example of twisted pair interface layout with external magnetics



3.3 Optical Interface

Figure 3-7 shows an example schematic for a connection between an optical interface and one channel of the Ethernet PHY. Component details are shown in table 3-2 below.

Figure 3-7 Schematics for optical interface circuit

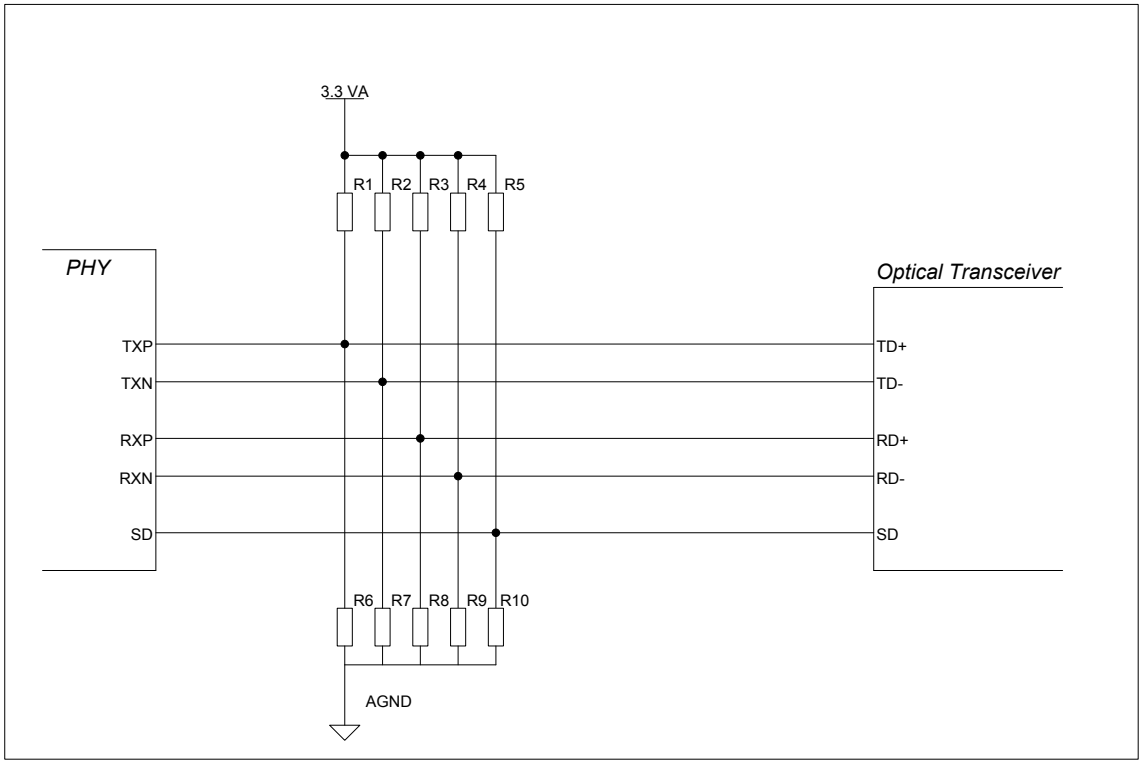


Table 3-2 Part list – optical interface

Part	Type	Characteristics	Recommended components
R1, R2	Resistor	51Ω±1%	
R3, R4, R5	Resistor	130Ω±1%	
R6, R7	Resistor	750Ω±1%	
R8, R9, R10	Resistor	82Ω±1%	
Optical Transceiver		One channel 1300nm	Avago Technologies AFBR-5803

Notes:

- All resistors should be placed as close as possible to the optical transceiver.

3.4 Optical Signal Specification

The behaviour of the optical interfaces is described here.

The min and max values for these signals are shown in table 3-3.

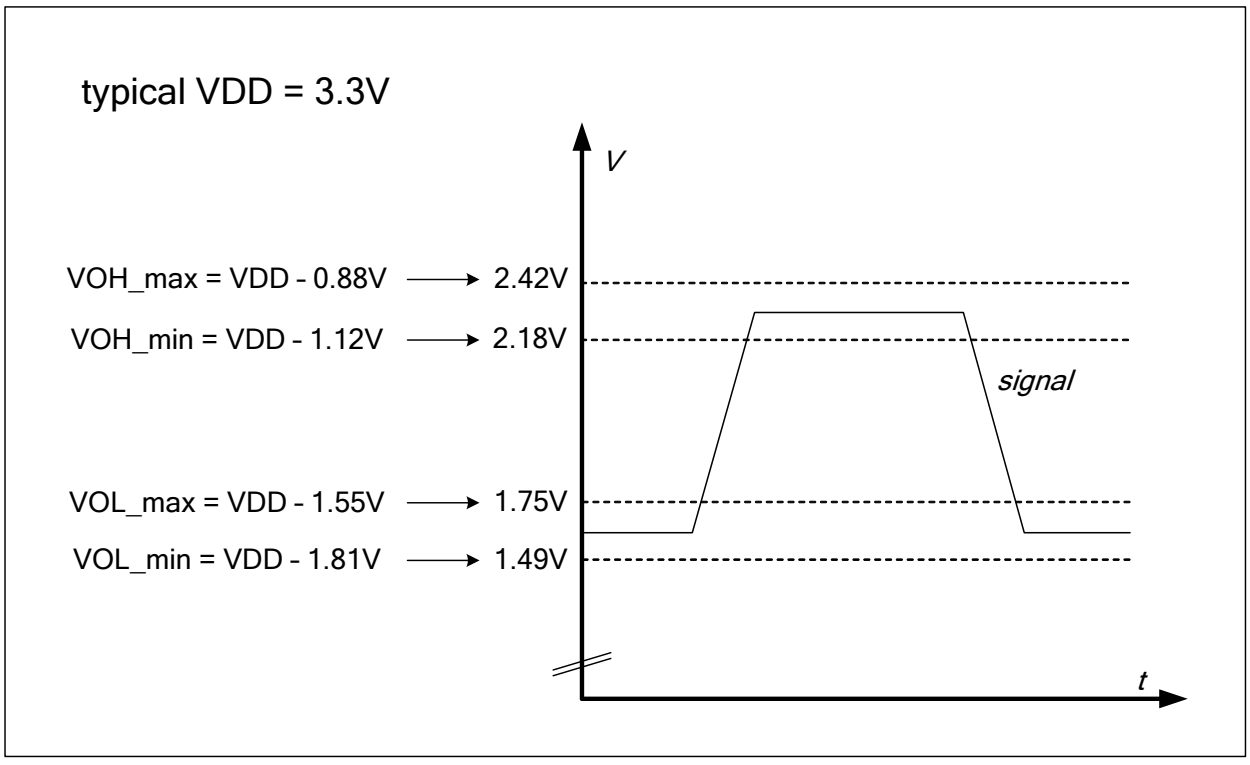
The ranges for the optical signalling are dependent from the 3.3V supply voltage. 3.0V – 3.6V is the allowed range for this voltage supply. An example for the typical 3.3V is shown in figure 3-8.

The nominal 3.3 V is shown as VDD.

Table 3-3 Optical Interface Specification Table

	Specification	
	Min	Max
Output Voltage Low - VOL [V]	VDD - 1.81	VDD - 1.55
Output Voltage High - VOH [V]	VDD - 1.12	VDD - 0.88

Figure 3-8 Optical output signal for typical supply voltage



3.5 Configurable Twisted Pair or Optical Interface

As described at the beginning of this chapter and in chapter 2 the PHY mode of the connected MDI interface should be set via strap pin configuration. Thus a PHY channel can be used in Twisted Pair or optical configuration – not both at the same time. It is possible to use the dual channel PHY ASSP with different media at the two channels.

In some cases (e.g. for evaluation) it could be necessary to develop a board with the possibility to change the used medium of the Ethernet PHY. This chapter describes shortly how to arrange such a flexible board design. Please note that such a configuration is not an optimized design for differential pair routing and should be avoided if possible.

To create a flexible board design connection options for 0Ω resistors should be placed in the differential pair traces. An example circuit design is shown in figure 3-9. For the related operation mode the resistors R1-R4 (optical) or R5-R8 Twisted Pair) have to be soldered on the PCB. The unused traces must be open.

Figure 3-10 shows a layout example. It has to be considered that the splitting connections are placed very close to the device, as some of the following components in the twisted pair circuitry should also be very close at the PHY. To avoid crossing lines these connections should be vias to route both circuitry in different layers. To avoid large stubs the 0Ω resistors footprints should be closest to the via.

Figure 3-9 Schematic for parallel twisted pair and optical preparation

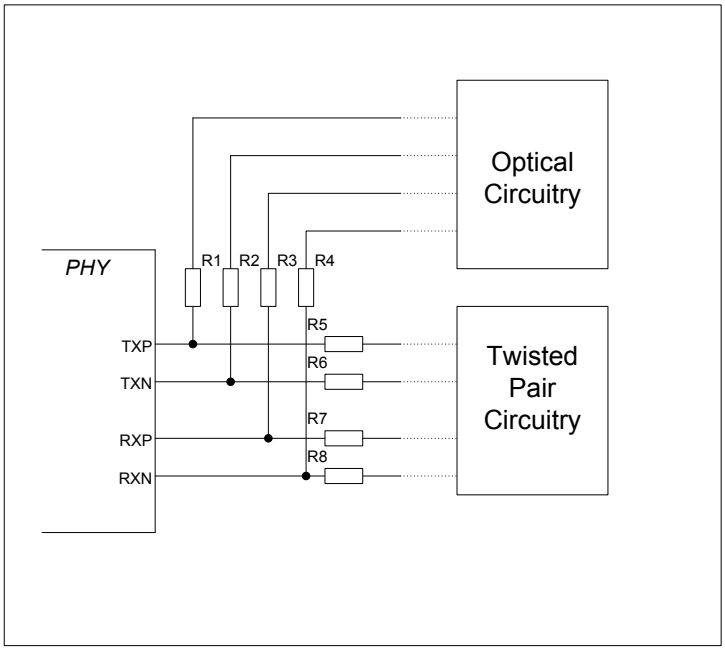
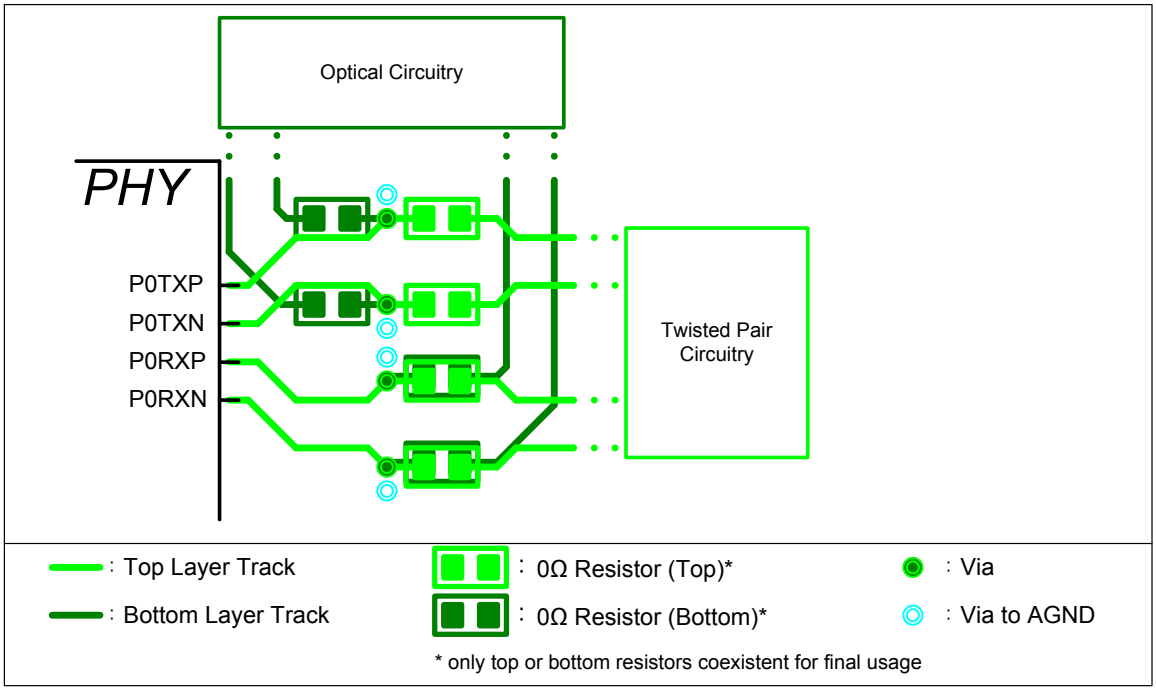


Figure 3-10 Layout Example parallel twisted pair and optical preparation



Chapter 4 MAC Interfaces – MII and RMII

The Ethernet PHY ASSP supports MII and RMII configuration to be connected to a MAC. Both modes need special hardware configuration and only one of these modes can exclusively operate at one time. The mode can be set via strap-pin configuration.

The tables below give an overview of all MII or RMII related pins. Table 4-1 shows all pins for PHY 0, table 4-2 all pins of PHY1 and table 4-3 the two SMI pins for the PHY control.

In figure 4-1 and 4-2 example schematics for MII and RMII are given.

Table 4-1 PHY0 ports: MII – RMII

Port name	I/O	Pin	MII function	RMII function
P0COL	O	21	Collision detect	Not used Wiring: OPEN
P0TXD0	I	43	Transmission data	Transmission data
P0TXD1	I	44		
P0TXD2	I	45		Not used Wiring: Pull-down
P0TXD3	I	46		Not used Wiring: Pull-down
P0TXERR	I	47	Send error	Not used Wiring: Pull-down
P0TXEN	I	48	Transmission enable	Transmission enable
P0TXCLK	O	49	Transmission clock 10BASE-T: 2.5MHz 100BASE-TX: 25MHz	Not used Wiring: OPEN
P0RXD0	O	53	Receive data	Receive data
P0RXD1	O	54		
P0RXD2	O	55		Not used Wiring: OPEN
P0RXD3	O	56		Not used Wiring: OPEN
P0RXDV	O	57	Receive data valid	P0CRS_DV
P0RXERR	O	58	Receive error	Receive error
P0RXCLK	O	59	Receive clock 10BASE-T: 2.5MHz 100BASE-TX: 25MHz	Not used Wiring: OPEN
P0CRS	O	60	Carrier sense	Not used Wiring: OPEN

Table 4-2 PHY1 ports: MII – RMII

Port name	I/O	Pin	MII function	RMII function
P1COL	O	22	Collision detect	Not used Wiring: OPEN
P1TXD0	I	23	Transmission data	Transmission data
P1TXD1	I	24		
P1TXD2	I	25		Not used Wiring: Pull-down
P1TXD3	I	26		Not used Wiring: Pull-down
P1TXERR	I	27	Send error	Not used Wiring: Pull-down
P1TXEN	I	28	Transmission enable	Transmission enable
P1TXCLK	O	29	Transmission clock 10BASE-T: 2.5MHz 100BASE-TX: 25MHz	Not used Wiring: OPEN
P1RXD0	O	35	Receive data	Receive data
P1RXD1	O	36		
P1RXD2	O	37		Not used Wiring: OPEN
P1RXD3	O	38		Not used Wiring: OPEN
P1RXDV	O	39	Receive data valid	P1CRS_DV
P1RXERR	O	40	Receive error	Receive error
P1RXCLK	O	41	Receive clock 10BASE-T: 2.5MHz 100BASE-TX: 25MHz	Not used Wiring: OPEN
P1CRS	O	42	Carrier sense	Not used Wiring: OPEN

Table 4-3 SMI signals

Port name	I/O	Pin	Function
MDC	I	62	Data clock for PHY control Timing clock of MDIO
MDIO	I/O	63	Data I/O for PHY control

Figure 4.1 and 4.2 show schematics for an MII and an RMII interface. The schematics are examples for one PHY channel. The direction of the signaling is shown with blue arrows. The component values are displayed in table 4-4 below.

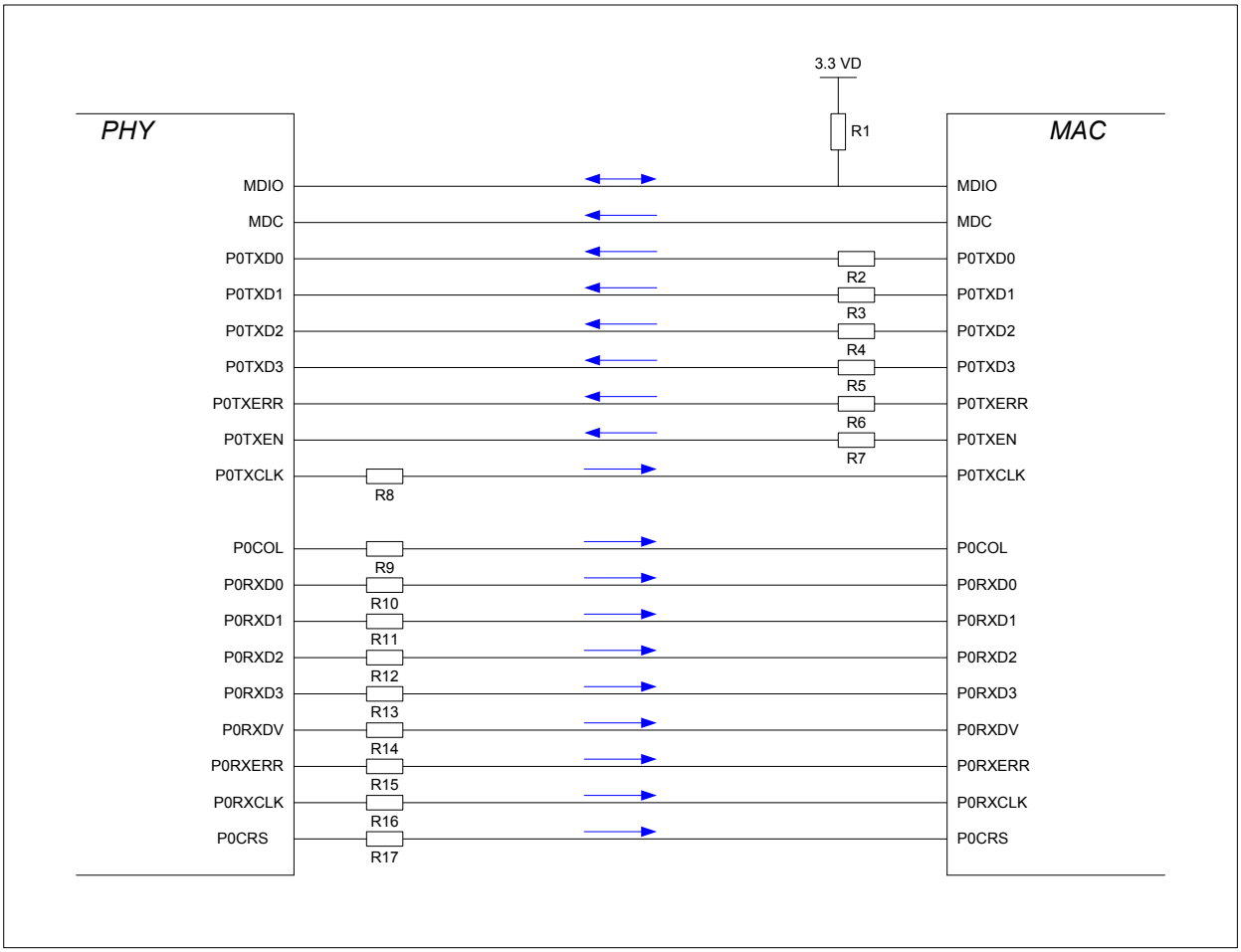
Some layout recommendations are described by the following notes. For further information the documentation of the used MAC and standardization notes (IEEE) should be considered.

General Notes:

- The MDIO signal line should be connected to a 1.5kΩ resistor.
- 10Ω resistors at the outputs reduce reflections on the signal lines
- Some the MII/RMII ports provide a strap pin configuration. This additional wiring is described in chapter 2.
- The recommended impedance for all MII signal lines to GND is 50Ω±10%.

- The Data Signals (TXD3:0 and RXD3:0) and the related clock (TXCLK, RXCLK) are handled as bus communication lines. Thus the four data lines and the related clock line should match in length (deviation within 10mm). Also the other related signals (TXEN/RXDV, ERR) should have this length. Same length match is also important in RMII mode.
- All MII/RMII lines should be wired as short as possible.
- The signals should be routed in one layer, vias should be avoided
- Similar to all other signal lines the routing should be as straight as possible. Lines should bend with a 45 degree angle or less.
- For clock lines it can be useful to shield them by GND lines especially if longer traces are necessary.

Figure 4-1 MII interface

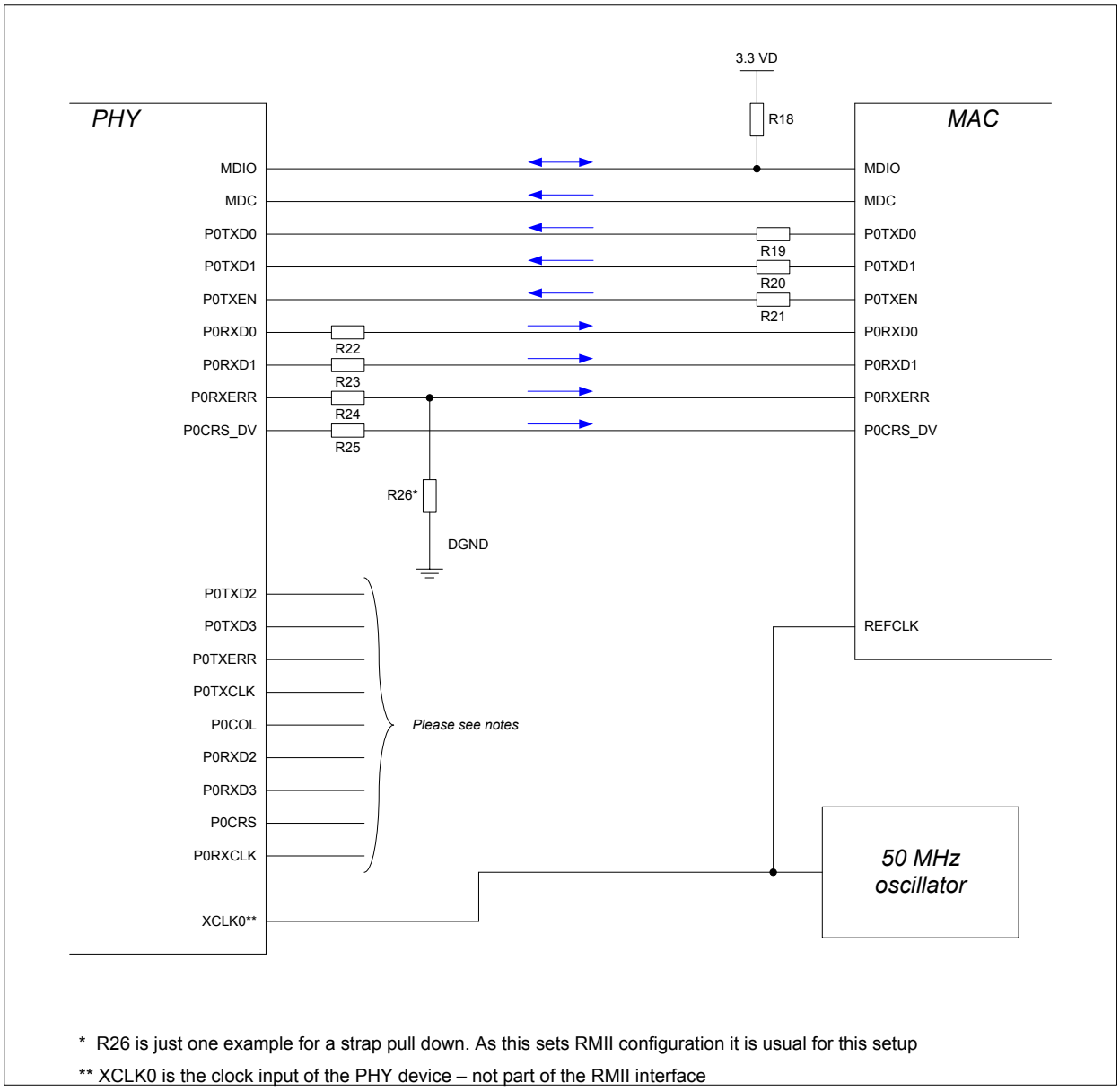


RMII specific notes:

- In RMII mode no clock is provided from the interface itself. Reference clock for the MAC is the same 50 MHz clock used for the whole PHY device (see also chapter 7).
- R26 is simply one example for a strap pin pull-down resistor. This one configures the PHY to RMII mode (see also chapter 2)
- Not used port pins can be used as additional GPIOs.

- If they are not used as GPIO please handle as follows:
  - Consider if there is needed a strap-pin option which needs a resistor
  - If a not used pin is programmed as input please pull it to GND
  - If a not used pin is programmed as output please leave it open
  - Best solution is to leave all unused pins open and program these GPIOs to an output function (e.g. 0x0011). If you need a strap resistance program the port as input (0x1111).

Figure 4-2 RMII interface



* R26 is just one example for a strap pull down. As this sets RMII configuration it is usual for this setup

** XCLK0 is the clock input of the PHY device – not part of the RMII interface

Table 4-4 Part list – MII and RMII interfaces

Part	Type	Characteristics	Recommended components
R1, R18	Resistor	1.5kΩ	
R2 – R17 R19 – R25	Resistor	10Ω	
R26	Resistor	~ 3.9kΩ	

Chapter 5 Power Supply

This chapter describes the power supply of the dual channel PHY ASSP. It gives some important recommendations and shows examples for schematic and layout design. The PHY needs 3.3V and 1.5V power supplies. The 1.5V can be supplied via the system power supply or by internal voltage regulator. In this case the PHY can be supplied with 3.3V only.

Note:
In the following schematics of the power supply a lot of filtering components are used (Capacitors, ferrites, etc.). The given values of these parts are simply examples of running designs. The choice of these values depends on the quality of the supplied system power and the PCB design itself.

5.1 Power Supply Related Port Pins

Table 5-1 shows all power supply and GND pins of the PHY device. For the following explanations the pin names are used.

Table 5-1 Power supply and GND related ports

Power Supply	Pins	Comment
REGBVDD	70, 71	3.3V voltage regulator input
REGBGND	74, 75	GND for voltage regulator
VDDIO	32, 50, 66	3.3V/2.5V IO power supply
VDD33ESD	20	3.3V input
P1AGND, P0AGND	8, 14	Analog GND for PHY
REGAGND	76	Analog GND for regulator
REGAVDD	77	Analog 3.3V power supply for regulator
GNDIO	31	GND for IO
GND15	51	GND for digital core
VDD15	30, 52	1.5V Digital VDD
VSSAPLL	9	Analog GND for PLL
VDDAPLL	11	Analog 1.5V power supply for PLL
VDDACB	10	Analog 3.3V power supply (common for both channels)
P1VDDMEDIA, P0VDDMEDIA	3, 19	Analog 1.5V power supply for PHY
REGLX	72, 73	Output voltage regulator, connect to external coil
REGFB	78	Feedback to voltage regulator, connect to external capacitor
REGOFF	80	Regulator disable: Hi: Regulator disabled Low: Regulator enabled

5.2 3.3 V Power Supply

A schematic for the 3.3 V Power supply is shown in figure 5-1. The related part list is shown in table 5-2.

Note:

- The capacitors C3, C4, C7, C8, C9 should be placed closest to the PHY. The other components could be arranged with some little space to the PHY.

Figure 5-1 3.3V power supply

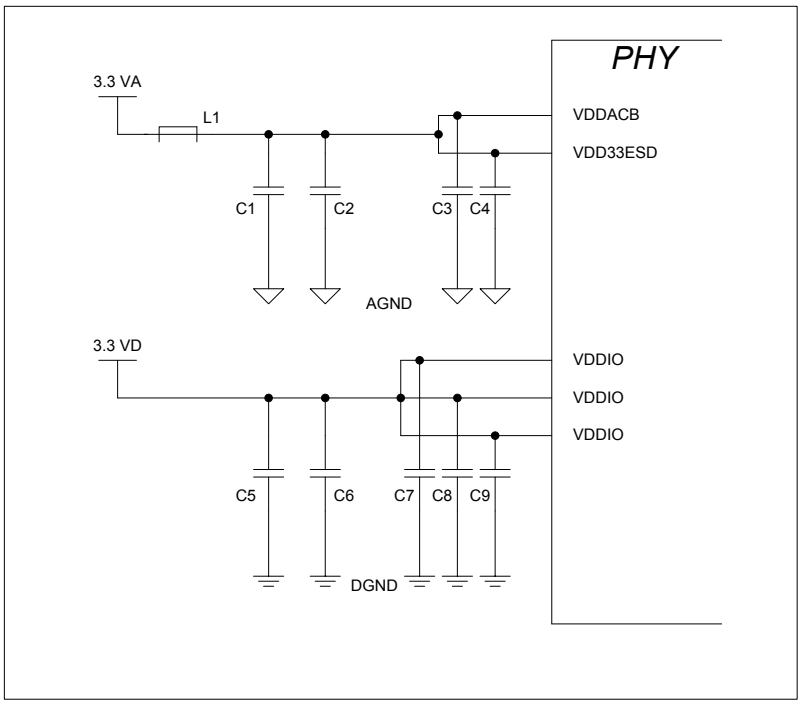


Table 5-2 Part list – 3.3V power supply

Part	Type	Characteristics	Recommended components
C1, C5	Capacitor	10uF±10%	
C2, C3, C4, C6, C7, C8, C9	Capacitor	100nF±10%	
L1	Ferrite Bead	120Ω @ 100MHz	Murata BLM21AG121SH1

5.3 1.5V Power Supply

A schematic for the 1.5 V Power supply is shown in figure 5-2. The related part list is shown in table 5-3.

Note:

- Similar to the 3.3V supply circuits the capacitors C11, C12, C13, C14, C16, C17 should be placed closest to the PHY and the other components could be arranged some centimetres away.

Figure 5-2 1.5V power supply

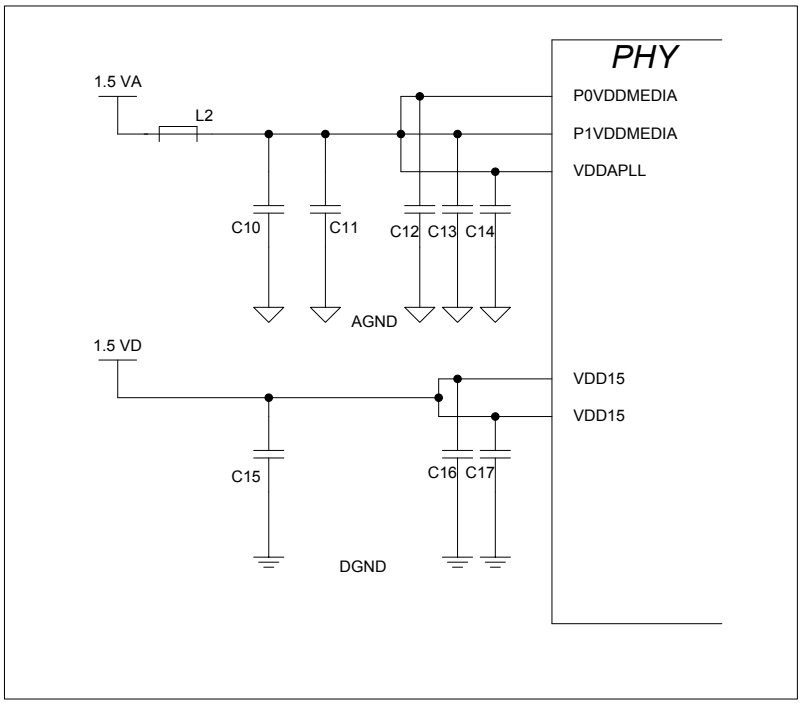


Table 5-3 Part list – 1.5V power supply

Part	Type	Characteristics	Recommended components
C10, C15	Capacitor	10uF±10%	
C11, C12, C13, C14, C16, C17	Capacitor	100nF±10%	
L2	Ferrite Bead	120Ω @ 100MHz	Murata BLM21AG121SH1

5.4 Integrated Voltage Regulator

As outlined above the PHY ASSP has an integrated voltage regulator to generate the needed 1.5V itself. Thus a 3.3V only operation is possible. The regulator is a switching regulator. This chapter describes the external wiring for both cases: regulator operation and regulator disabled.

5.4.1 Regulator Operation – 1.5V Generation

Figure 5-3 shows the wiring for the external regulator circuit if the regulator is used to generate the 1.5V for the PHY. Table 5-4 shows the recommended components. In Figure 5-4 a layout example is given.

Notes:

- All components except the pull-down resistor R1 should be placed as close as possible to the related PHY pins.
- Preferable the connections at REGBVDD, REGAVDD, REGBGND, REGAGND, REGLX, and REGFB should be planes instead of small tracks. At least 1mm track width is mandatory.
- If possible REGAVDD and REGBVDD should be supplied via separated tracks. The connection point between these lines should be 20mm or more distant from the PHY. A connection directly at the regulator input could cause noise transfer between REGBVDD and REGAVDD.
- *Important:* The characteristic of C19 is mandatory. A lower ESR will cause problems for the regulator oscillation!

Figure 5-3 Regulator circuit – regulator used

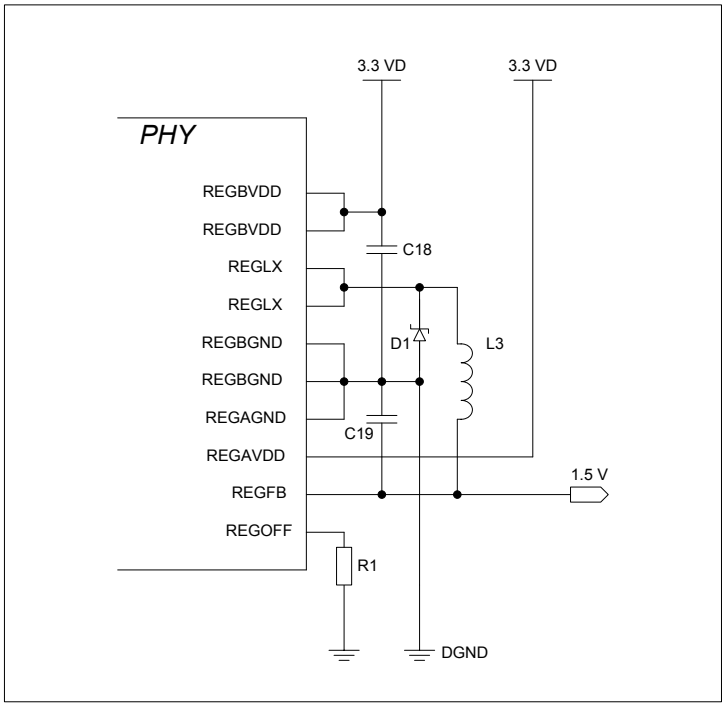


Table 5-4 Part list – regulator circuit – regulator used

Part	Type	Characteristics	Recommended components
C18	Capacitor	22uF ±20%	
C19*	Tantalum Capacitor	22uF ±20% ESR: 150-350mΩ	PSLB21A226M (NEC TOKIN) TCJB226M010R0300 (AVX) T494C226K016AT (KEMET)
D1	Schottky Rectifier Diode	30V,1A	SBS005 (SANYO) STPS1L30UPBF (ST)
L3	Inductor	10uH	VLCF5028T (TDK)
R1	Resistor	~ 4.7kΩ	
C19a*	Ceramic Capacitor	22uF ±10%	Evaluated with: GRM32ER71A226KE20L
R19a*	Resistor	100mΩ ±1%	Evaluated with: MCR18EZHFLR100

*Note:

- To avoid the recommended tantalum capacitor it is possible to compose the needed characteristics with a series connection of a resistor and ceramic capacitor.

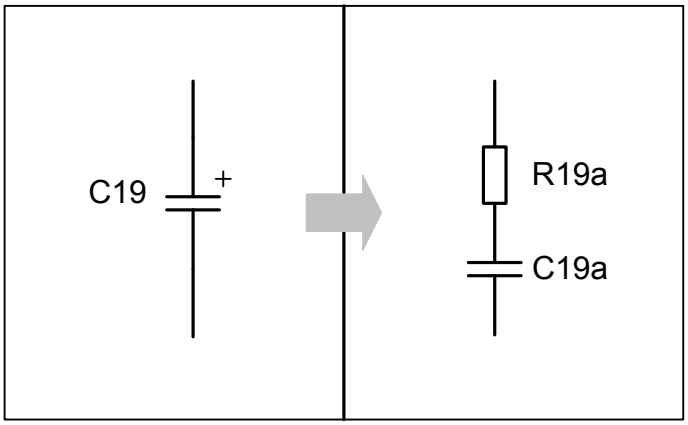
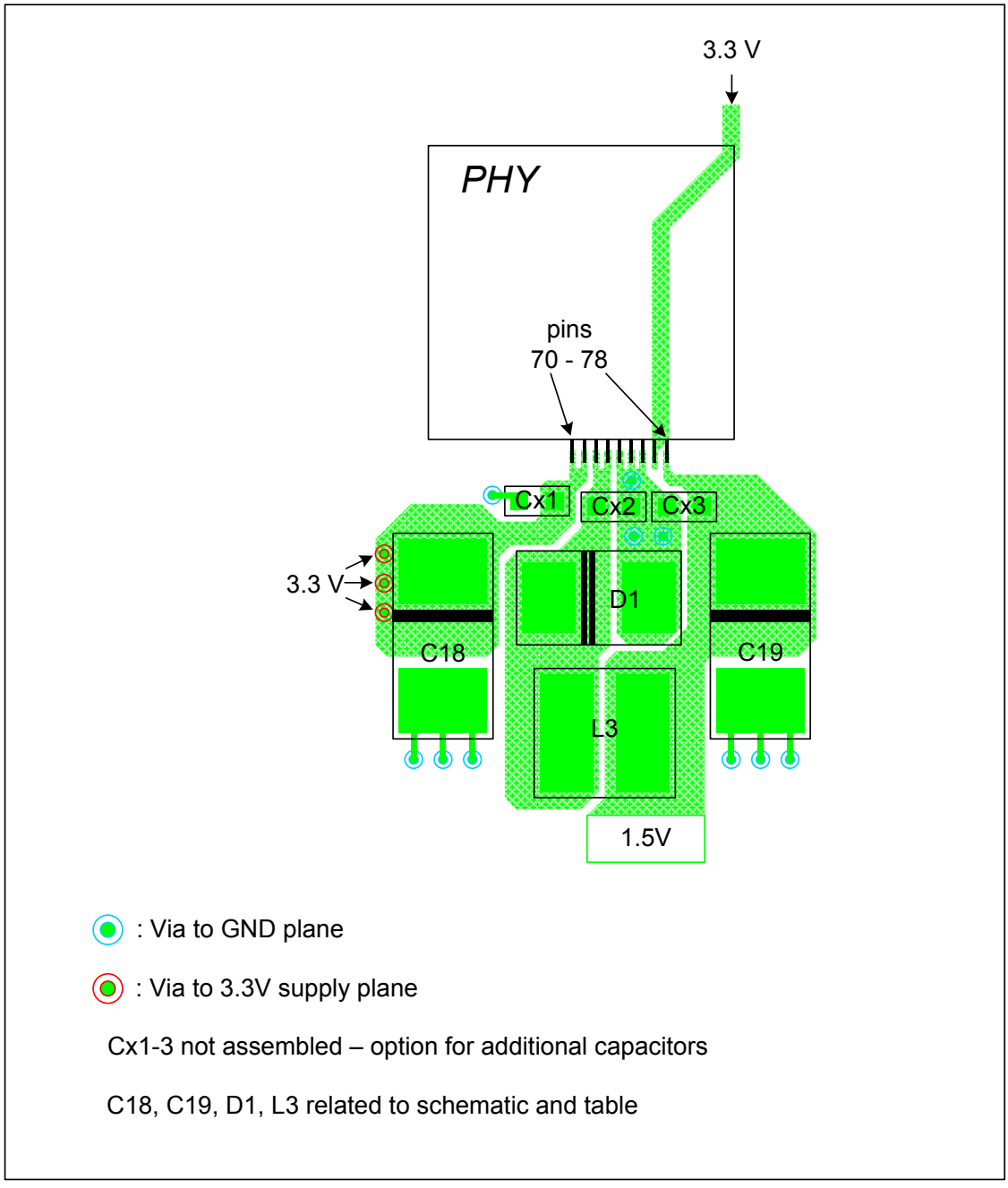


Figure 5-4 PCB layout example for regulator usage



Note: *The option for additional capacitors has been designed to add further filter opportunities. This is usually not necessary.*

5.4.2 Regulator Disabled – External 1.5V Supply

The wiring for a disabled internal regulator is shown in figure 5-5. The part list is shown in table 5-5.

Notes:

- A supply for the 3.3V is still necessary but without any rules.
- REGLX ports should be open and not connected to anything.
- REGFB should be connected to GND via a pull-down resistor
- To disable the regulator REGOFF has to be connected to 3.3V via a pull-up resistor.

Figure 5-5 Regulator circuit – regulator not used

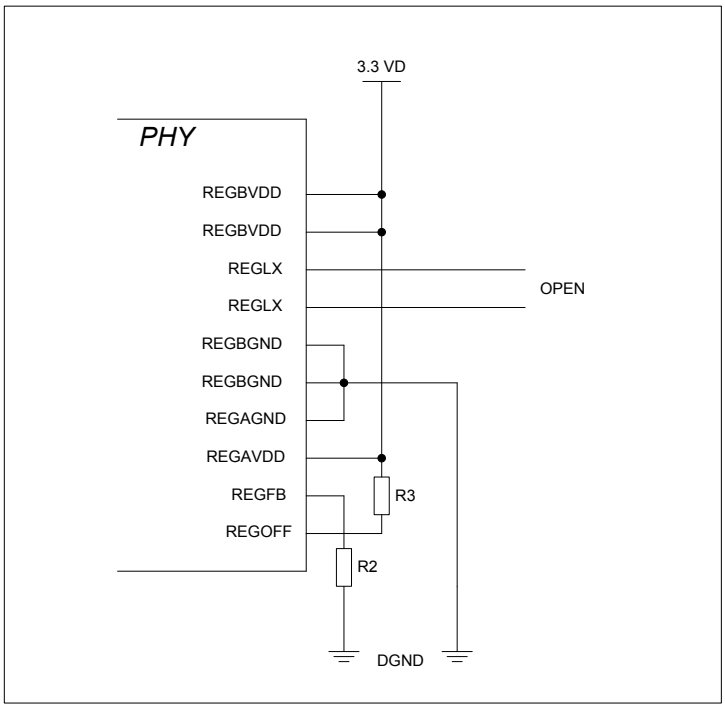


Table 5-5 Part list - regulator circuit – regulator not used

Part	Type	Characteristics	Recommended components
R2	Resistor	~ 4.7kΩ	
R3	Resistor	~ 4.7kΩ	

Chapter 6 Layout of Power Supply and GND Planes

This chapter gives some recommendations how to design supply and GND areas.

Table 6-1 shows the three kinds of supply and GND and the related sections.

Table 6-1 Power supplies and GNDs

Category	Name	Detail
3.3V	3.3V	3.3V system power – board supply
	3.3VD	+3.3V for digital
	3.3VA	+3.3V for analog
1.5V (if supplied externally)	1.5V	1.5V system power – board supply
	1.5VD	+1.5V for digital
	1.5VA	+1.5V for analog
Ground	DGND	Digital Ground
	AGND	Analog Ground
	FGND	Frame Ground

6.1.1 3.3V supply

The 3.3V supply includes 3.3V board supply and the PHY related analogue and digital supplies 3.3VA and 3.3VD.

Note:

- These supplies should be connected at one point via a filter structure.

6.1.2 External 1.5V supply

External 1.5V supply is needed if the built-in regulator is not used.

Similar to the 3.3V supply the 1.5V includes a board supply and the PHY related analogue and digital supplies 1.5VA and 1.5VD.

Note:

- These supplies should be connected at one point via a filter structure.

6.1.3 GNDs

For a PHY board three separated GNDs are recommended: Digital ground (DGND), analogue ground (AGND) and frame ground (FGND).

Notes:

- DGND and AGND should be connected at one point via a 0Ω resistor.
- The components connected to DGND and AGND should be placed beneath or above the related GND plane.
- The FGND should surround the PCB at its edge.
- The FGND should be at the top and the bottom layer of the PCB.
- The FGND should also be connected to the other GNDs. This can be done via low impedance path or any special circuit, e.g. ESD protection.
- The FGND can be connected to chassis grounding
- Ground wires and areas especially at shields or close to differential pairs should have enough vias to the GND plane (e.g. every 5-10mm).

6.1.4 Layout example

Figure 6.1 – 6.4 show a layout example for a four layer PCB. This layout is an idealized and simplified illustration.

Figure 6-1 Power and GND layout – Layer 1

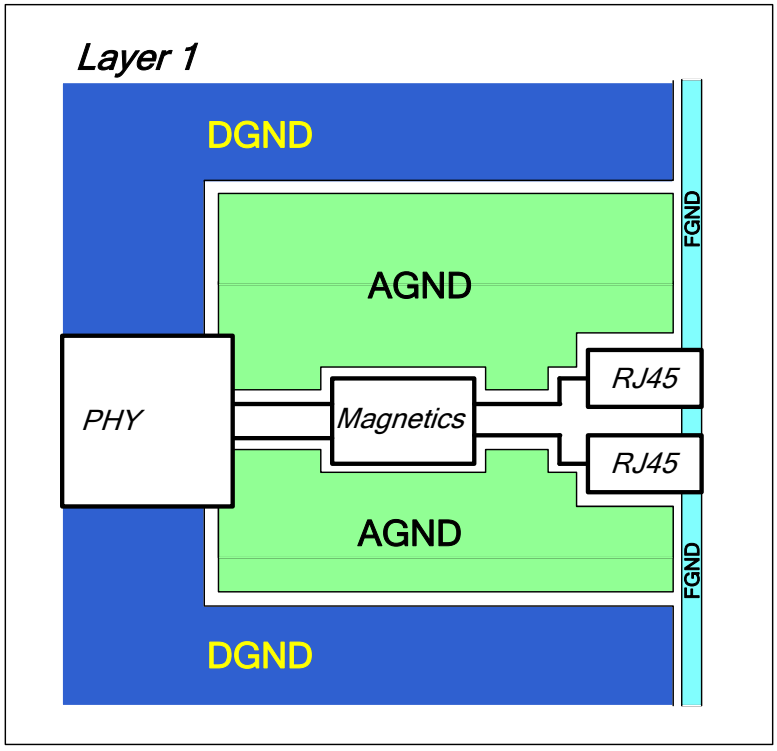


Figure 6-2 Power and GND layout – Layer 2

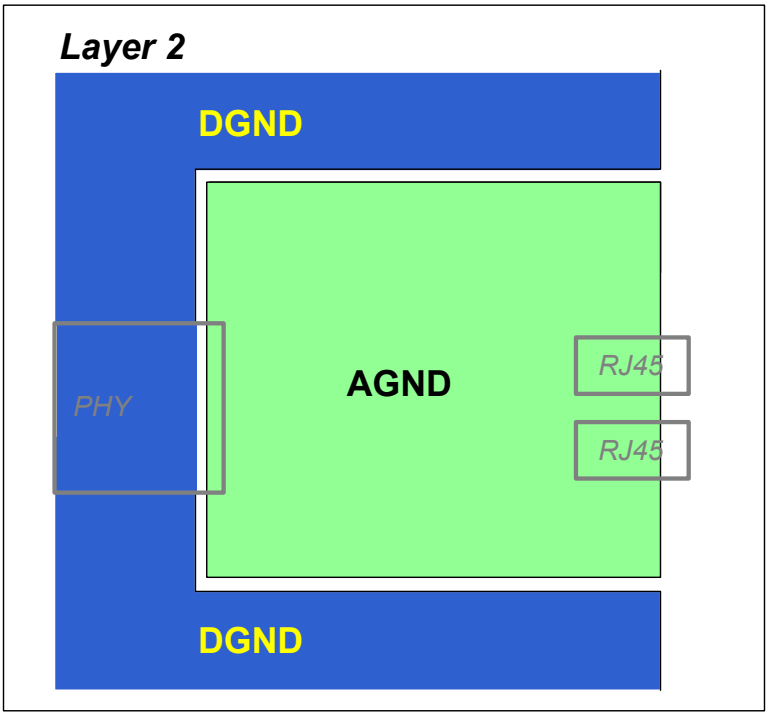


Figure 6-3 Power and GND layout – Layer 3

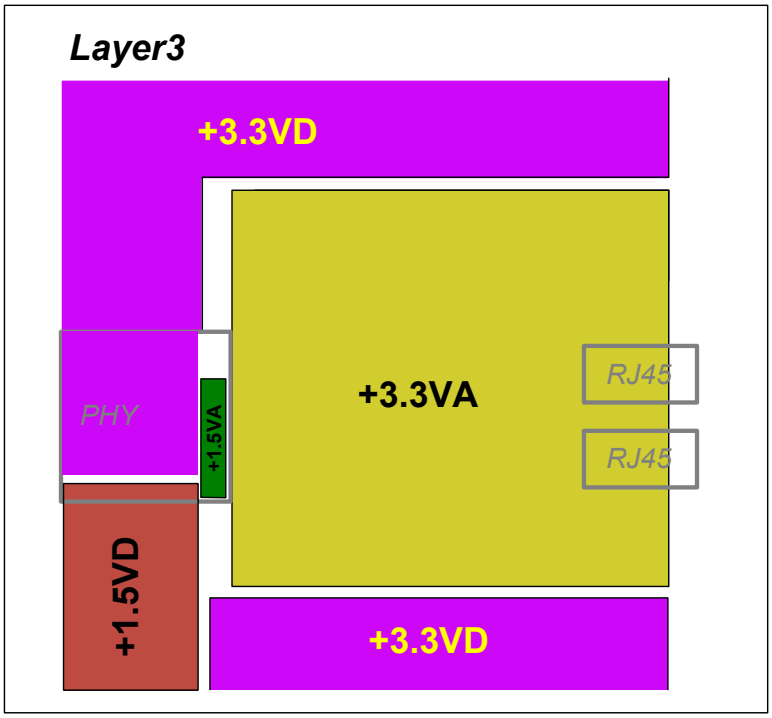
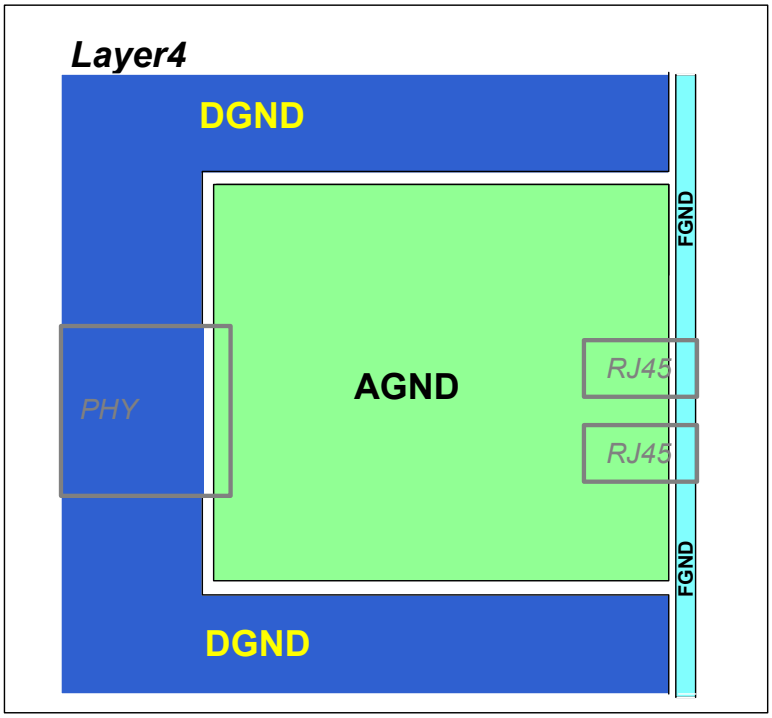


Figure 6-4 Power and GND layout – Layer 4



Chapter 7 External Reference Clock

7.1 Reference Clock

For operation of the Ethernet PHY ASSP an external clock is needed. For MII operation a 25MHz clock has to be applied to the PHY device. For RMII operation the frequency of the clock has to be 50MHz.

The external clock can be provided by a quartz crystal or any other oscillator.

In case of 50MHz usage for RMII configuration an oscillator should be used because the signal is also used as clock for data transfer (see chapter 4).

The requirements of an oscillator that can be used are shown in table 7-1.

Table 7-1 Reference clock requirements

Item	Min	Typ	Max	Unit	Comment
Reference Clock frequency		25		MHz	For MII mode
		50		MHz	For RMII mode
Allowed error margin	-100		100	ppm	
Duty cycle	40	50	60	%	
Allowed Jitter		20		ps	RMS value

7.2 Circuit and layout for clock input

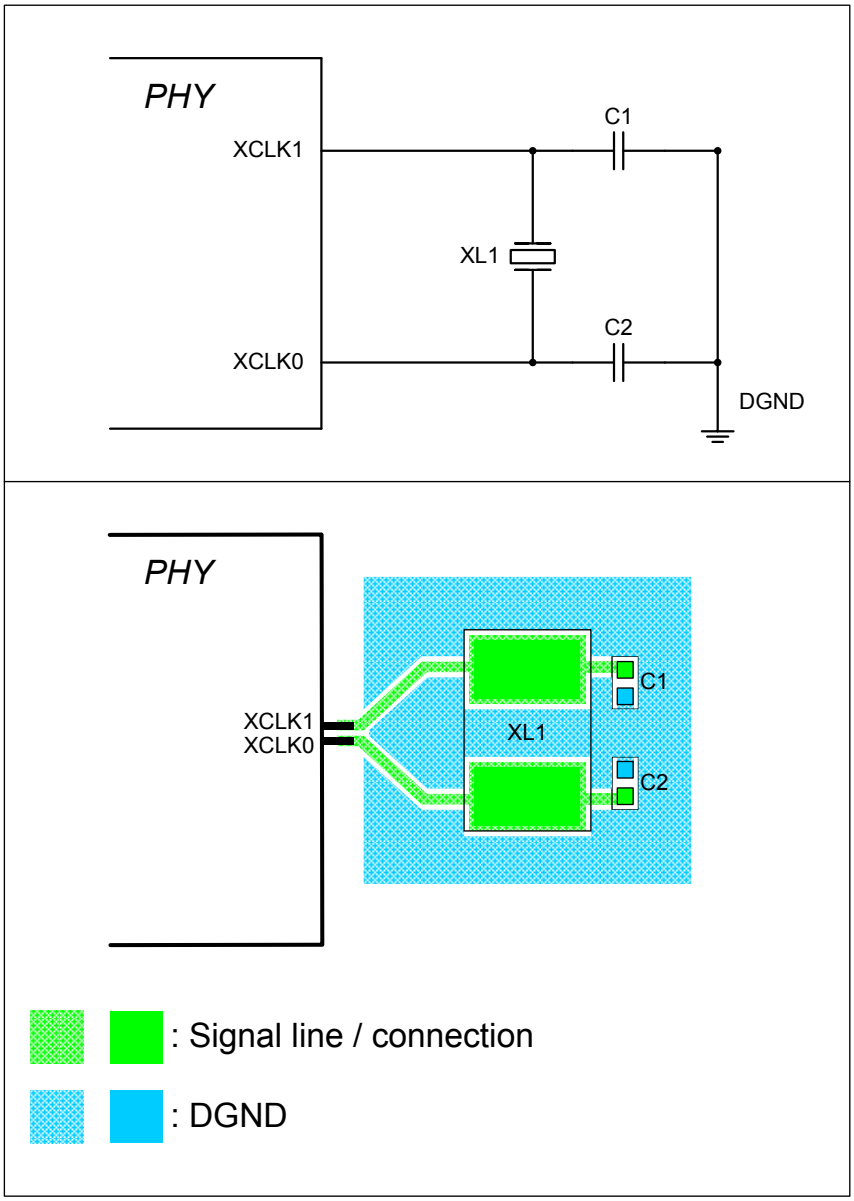
As described different clock sources are possible.

Two examples for schematic and layout are given here. Figure 7-1 shows a schematic and layout example for a quartz crystal use. Similar examples for an oscillator are shown in figure 7-2.

General notes:

- The clock supply circuit should be placed near to the clock input pins (XCLK0, XCLK1).
- The clock supply circuit should be separated from other signal and communication lines.
- Preferable the clock supply circuit is surrounded with DGND.
- The used devices for the external clock may have their own design recommendations. They should also be considered.

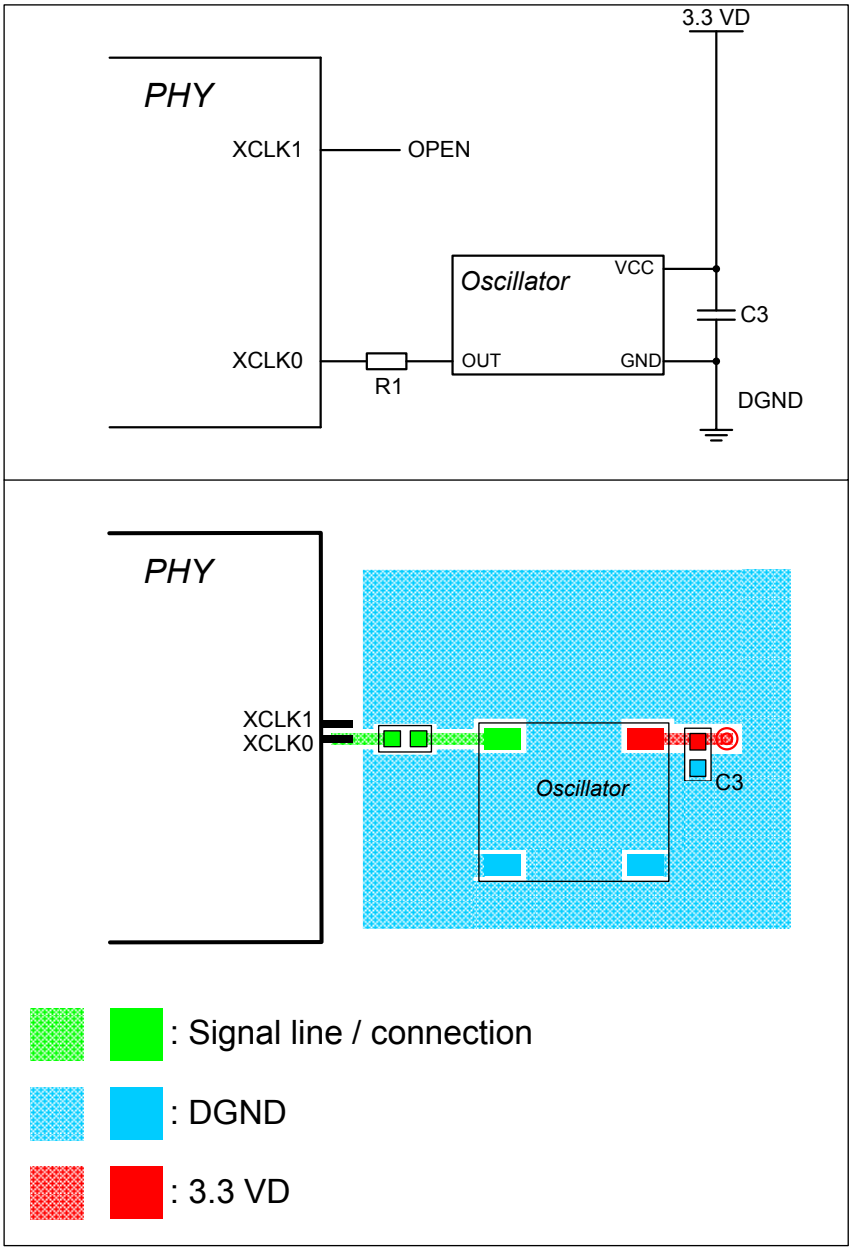
Figure 7-1 Schematic and layout example for quartz crystal usage



Notes related to quartz crystal usage:

- A quartz crystal has to be connected to XCLK0 and XCLK1.
- C1 and C2 are load capacitors for the quartz crystal. For the capacity values of C1 and C2 the data sheet of the used quartz should be considered.
- It is preferable to shield the clock signals with a surrounding DGND plane as shown in the layout Example.
- As mentioned before a quartz crystal is applicable for 25MHz only.

Figure 7-2 Schematic and layout example for oscillator usage



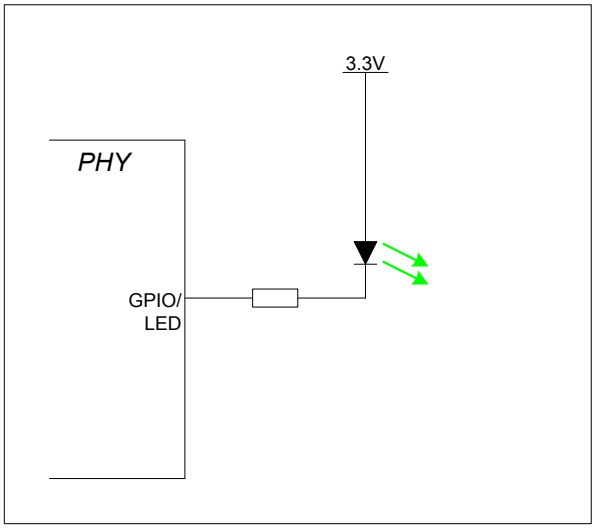
Notes related to oscillator usage:

- If the clock is applied by an oscillator this has to be connected to XCLK0.
- XCLK1 port should be open and not connected to anything
- R1 is a damping resistance. Its value depends on the used oscillator.
- C3 is a decoupling capacitor. For its value the oscillator data sheet should be considered.
- It is preferable to shield the oscillator and the signal with a surrounding DGND plane as shown in the layout Example.

Chapter 8 LED Control

The dual channel PHY originally provides 3 different LED output signals per channel. Every GPIO pin can be configured to output one of these LED signals. In contrast to all other GPIOs signals the LEDs are active low. Thus a LED has to be connected between 3.3V and LED output. A schematic is shown in figure 8-1.

Figure 8-1 Circuit for LED operation



Note:

- No component recommendations are given because their values interdepend. The strength of the used output port should also be considered (refer UM).

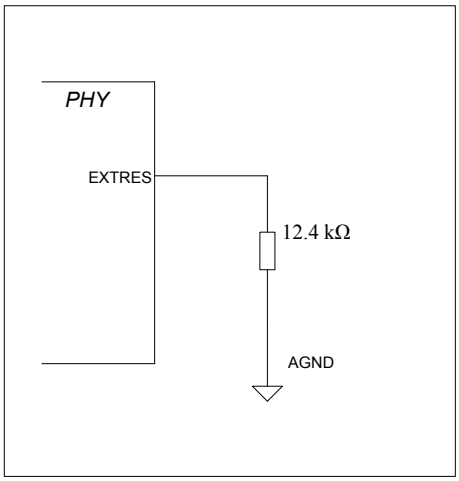
Chapter 9 EXTRES

The EXTRES port defines the bias current of the PHY. It should be connected to DGND via 12.4kΩ as shown in figure 9-1.

Notes:

- The 12.4kΩ resistor should be placed near the PHY.
- It is recommended to use a 12.4kΩ resistance with maximum 1% range and 1/16W.
- Do not compose the 12.4kΩ resistance from two resistors (e.g. 12kΩ and 390Ω).

Figure 9-1 Wiring of EXTRES



Chapter 10 Unused pins

Table 10-1 shows the unused ports of the Dual Channel PHY ASSP and gives a recommendation how to terminate them in a design.

Table 10-1 Unused port pins

Port name	Pin	Termination
TEST	2	pull-down with ~4.7kΩ
ATP	13	pull-down with ~4.7kΩ

Chapter 11 Mount Pad Dimensions

Figure 11-1 and table 11-1 shows the recommended dimensions for the mount pads for the PHY ASSP. The related device dimensions are shown in table 11-2. For complete device dimensions refer the UM.

Figure 11-1 Mount Pad Dimensions

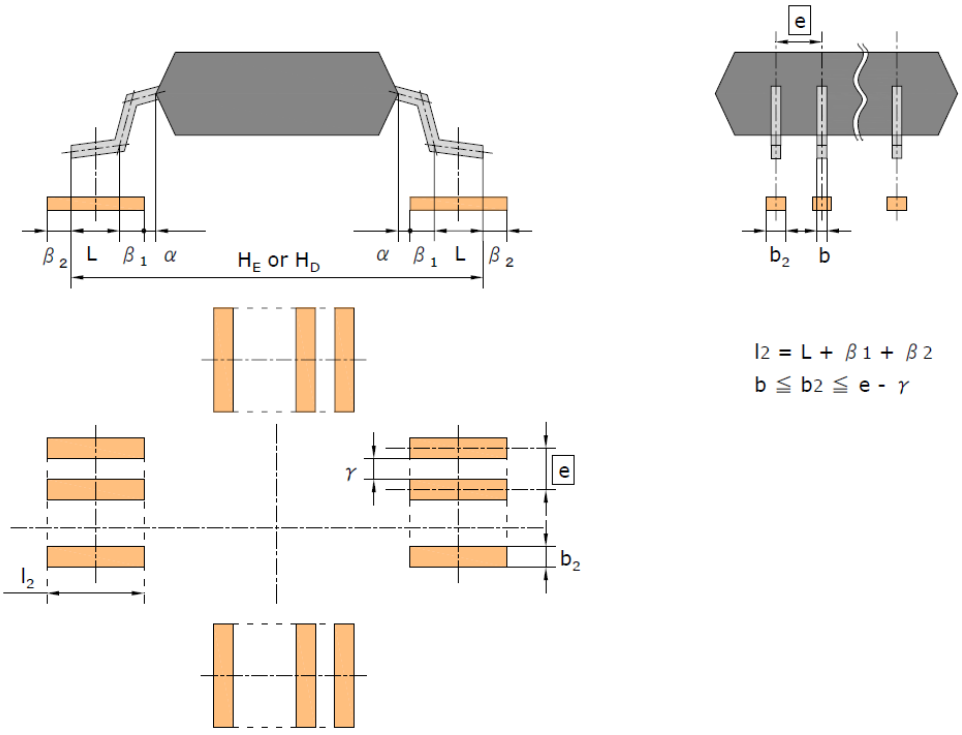


Table 11-1 Mount Pad Dimensions

Variable	Value in mm
α	0.10 – 0.30
β_1	0.20 – 0.40
β_2	0.20 – 0.40
γ	0.25

Table 11-2 Related Device Dimensions

Variable	Value in mm
L	0.50
e	0.50
b	0.2 + 0.07 - 0.03

Revision History

Revision	Date	Changes
1.0	December 17, 2012	
1.1	March 19, 2013	Minor changes
1.2	July 1, 2013	Optical Transceiver specs changed, other minor changes

General Precautions in the Handling of ASSP Products

The following usage notes are applicable to all ASSP products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of ASSP products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   The characteristics of ASSP in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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