Output Data Formats for Renesas Rad Hard Precision SAR ADCs

This application note discusses the output data formats available on the ISL73141SEH and ISL73148SEH rad hard precision SAR ADC products and details the configuration through the evaluation software iRADAnalyzer on their respective evaluation boards. There are a variety of formats that can be used to encode the digital output data from an ADC; therefore, it is important to understand how this is applied to the ISL73141SEH and ISL73148SEH. The purpose of this application note is to provide information on the available output data formats, explain their relationships, detail the configurations, and define the impact on the operation of these ADC products.

Throughout this application note, the data formats are presented primarily as 14 bits. Figures and tables are provided to aid the reader in understanding these different data formats and how the device mode of operation impacts these data formats for these ADC products. In all cases, the analog input voltage (A_{IN}) is limited to a maximum value equal to the input reference voltage (V_{REF}) because the V_{REF} voltage defines the full-scale input range of the ADC.

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1. Unsigned (Unipolar) Data Format

In an unsigned (unipolar) data format, the full-scale analog input voltage range of the ADC is straight coded to a binary code with a range from zero to the maximum binary value for a given resolution, such as fourteen 1s = 11 1111 1111 1111 (decimal value = +16383) for a 14-bit resolution. This is probably the simplest data format to understand as it is all positive values and is not specially encoded but rather is more straightforward. Table 1 provides information on the relationship between the ADC input scale, digital code in decimal and binary, and the input voltage to the ADC. At the lowest input voltage of 0V, the ADC input is considered zero-scale and the digital code is 0 in decimal and fourteen 0s in binary. As the input voltage increases, the digital code increases until the maximum input voltage of 4.096V is reached and the ADC input is at full-scale. The VREF voltage for this case is 4.096V for the ISL73141SEHF7 device. For the case of the ISL73141SEHFN, the VREF voltage is 3.0V and the values in Table 1 would scale accordingly. When at full scale, the digital output code is 16383 in decimal and fourteen 1s in binary. For the case of the ISL73141SEH, this data format is fixed and cannot be changed.

Table 1. Unsigned (Unipolar) Data Format for ISL73141SEH[1]

ADC Input Scale	Digital Code (Decimal)	Binary Digital Code Unsigned (Unipolar)	Input Voltage (V)
Zero-scale	0	00 0000 0000 0000	0
1/8 full-scale range	2048	00 1000 0000 0000	0.512
1/4 full-scale range	4096	01 0000 0000 0000	1.024
3/8 full-scale range	6144	01 1000 0000 0000	1.536
1/2 full-scale range	8192	10 0000 0000 0000	2.048
5/8 full-scale range	10240	10 1000 0000 0000	2.56
3/4 full-scale range	12888	11 0010 0101 1000	3.072
7/8 full-scale range	14336	11 1000 0000 0000	3.584
Full-scale	16383	11 1111 1111 1111	4.096

1. Voltage values based on the reference voltage of the ISL73141SEH being set to 4.096V.

The ISL73148SEH can also operate with an unsigned (unipolar) data format. When the ISL73148SEH is operated in this manner, only half of the available input range of the ADC is available, which means the total resolution is 13 bits instead of 14 bits. The ISL73148SEH contains an ADC core with a differential input but has single-ended analog inputs. The analog signal is applied to the positive input of each of the eight channels. The negative input for all eight channels is connected to the COM pin of the ISL73148SEH. When operating the ISL73148SEH in unsigned (unipolar) data format, the COM pin is connected externally to ground. The negative input to the internal ADC core of the ISL73148SEH is at ground potential (0V) when the COM pin is connected to ground. This only allows the input signal range to the ADC core to swing from 0 to 2.5V, therefore, allowing for operation only on the positive side of the ADC differential input voltage scale. For the case of the ISL73148SEH, the VREF voltage should be 2.5V. Table 2 provides information on the relationship between the ADC input scale, digital code in decimal and binary, and the input voltage to the ADC. The ADC input voltage values shown in the table are given for the case where the internal PGA (Programmable Gain Amplifier) gain is set to a value of one or is bypassed. The ADC input voltage scales based on the gain setting of the PGA. The common mode voltage on the analog input also scales with the PGA gain setting. For further details, refer to the *ISL73148SEH datasheet.*

Table 2. Unsigned (Unipolar) Data Format for ISL73148SEH[1]

ADC Input Scale	Digital Code (Decimal)	Binary Digital Code Unsigned (Unipolar)	Input Voltage (V)	ADC Input Voltage (V)
Zero-scale	0	0 0000 0000 0000	0	0
1/8 full-scale range	1024	1 0000 0000 0000	0.3125	0.3125

Table 2. Unsigned (Unipolar) Data Format for ISL73148SEH[1] (Cont.)

ADC Input Scale	Digital Code (Decimal)	Binary Digital Code Unsigned (Unipolar)	Input Voltage (V)	ADC Input Voltage (V)
1/4 full-scale range	2048	0 1000 0000 0000	0.625	0.625
3/8 full-scale range	3072	1 1000 0000 0000	0.9375	0.9375
1/2 full-scale range	4096	1 0000 0000 0000	1.25	1.25
5/8 full-scale range	5120	1 0100 0000 0000	1.5625	1.5625
3/4 full-scale range	6444	1 1000 0000 0000	1.875	1.875
7/8 full-scale range	7168	1 1100 0000 0000	2.1875	2.1875
Full-scale	8191	1 1111 1111 1111	2.5	2.5

1. Voltage values based on the reference voltage of the ISL73148SEH being set to 2.5V.

The iRADAnalyzer software tool makes it simple to configure the ISL73148SEH evaluation board into unsigned (unipolar) mode operation. Hardware is on the evaluation board that makes the appropriate circuit connections to place the ISL73148SEH into unsigned data format mode. Figure 1 provides the software selection settings in iRADAnalyzer to select unsigned data format and also provides a diagram of the hardware connections that are made on the evaluation board to enable this mode. The internal connections and voltage potentials are also given.

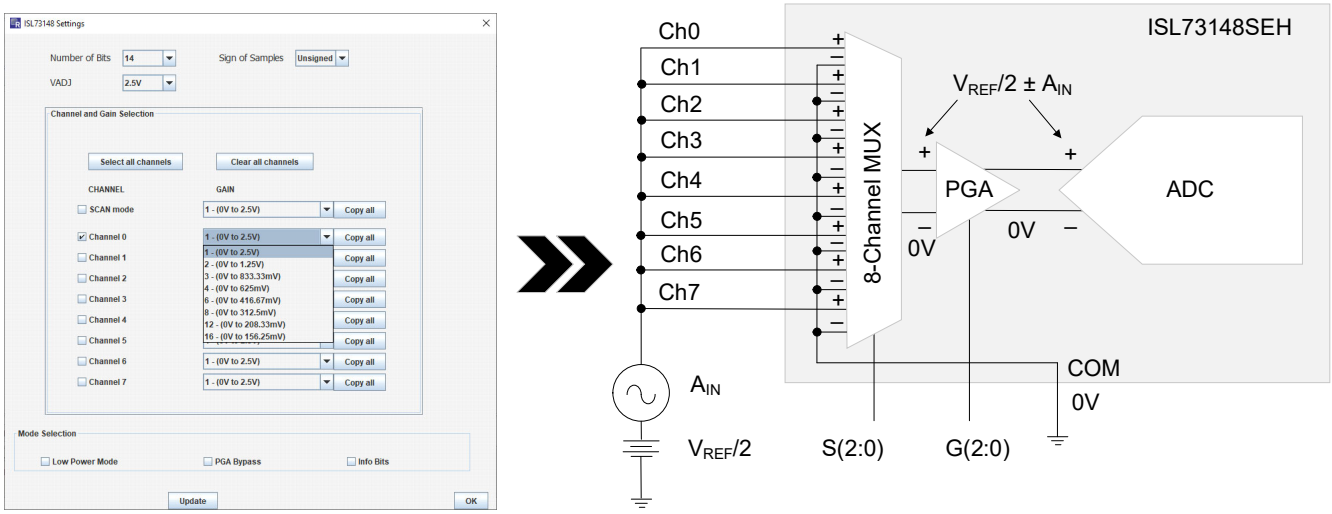

Figure 1. Unsigned (Unipolar) Data Format Software and Hardware Configuration for ISL73148SEHEV1Z

The user selections in the iRADAnalyzer software tool determine the ISL73148SEHEV1Z evaluation board hardware configuration. In the example in Figure 1, Channel 0 is selected and a gain of one is selected in iRADAnalyzer. All eight channels on the ISL73148SEHEV1Z board are connected together using headers by default, but only one channel at a time can be selected by the ISL73148SEH for conversion. The iRADAnalyzer software tool can however be configured to collect samples on more than one channel, just consecutively and not simultaneously. The evaluation hardware connects the COM pin of the ISL73148SEH to ground, sets the gain selection pins [G(2:0) = 000], and the channel selection pins [S(2:0) = 000], and adjusts the common mode value (V_{CM} = 1.25V) on the analog input to the selected channel. *Note:* For the conditions where the PGA is bypassed or the PGA gain is set to one, the same V_{CM} voltage is required on the analog input. If the gain ≥ 2 is selected, the evaluation hardware automatically adjusts the V_{CM} voltage appropriately based on the gain selection [$V_{CM} = (V_{REF}/2)/Gain$, where V_{REF} = ADC reference voltage]. It is up to you to adjust the analog input signal amplitude based on the PGA gain selection.

2. Signed (Bipolar) Data Format

The ISL73148SEH can also operate with a signed (bipolar) data format. In signed data format, the output data of the ADC is two's complement encoded. When the input voltage to the ISL73148SEH is at 0V, the digital output value from the ADC is a negative full scale, and when the input voltage is at 2.5V, the digital output value is a positive full scale. Therefore, when the differential input voltage is 0V, the digital output value is zero-scale. To enable the signed data format, the COM pin of the ISL73148SEH is bypassed to ground with a 0.1µF capacitor. For the ISL73148SEH, there are two digital output code ranges when operating with the signed data format. One range uses only the positive half of the ADC differential input range (PGA bypassed and PGA gain = 1), and the other range uses the full differential input range of the ADC (PGA gain ≥ 2).

When the PGA is bypassed or the gain is set to a value of one, the ADC can only operate on the positive side of its range. This feature makes the ISL73148SEH effectively operate as a 13-bit ADC in this condition with an output code range of -4096 to +4095. Table 3 provides information on the relationship between the ADC input scale, digital code in decimal and binary, and the input voltage to the ADC for this mode of operation. This mode uses the same analog input range of the ADC in the ISL73148SEH as used in the unsigned data format mode of operation. The difference in this mode is that the digital data is encoded as two's complement. Seeing that the input voltage can only be from 0V to 2.5V, the input voltages (A_{IN}) at each of the positive and negative inputs to the ADC can only swing from 0V to 1.25V providing for a differential input voltage range of 2.5V because there is no gain in the PGA (or the PGA is bypassed). Again, for the case of the ISL73148SEH, the VREF voltage should be 2.5V.

Table 3. Signed (Bipolar) Data Format for ISL73148SEH with PGA Gain = 1 or Bypassed

ADC Input Scale	Digital Code (Decimal)	Binary Digital Code Signed (Bipolar)	Input Voltage (V)	ADC Input Voltage (V)
Negative full scale	-4096	1 0000 0000 0000	0	0
1/8 full-scale range	-3072	1 0100 0000 0000	0.3125	0.3125
1/4 full-scale range	-2048	1 1000 0000 0000	0.625	0.625
3/8 full-scale range	-1024	1 1100 0000 0000	0.9375	0.9375
Zero-scale - 1 LSB	-1	1 1111 1111 1111	1.25 - V_{LSB}	1.25 - V_{LSB}
Zero-scale	0	0 0000 0000 0000	1.25	1.25
Zero-scale + 1 LSB	1	0 0000 0000 0001	1.25 + V_{LSB}	1.25 + V_{LSB}
5/8 full-scale range	1024	0 0100 0000 0000	1.5625	1.5625
3/4 full-scale range	2048	0 1000 0000 0000	1.875	1.875
7/8 full-scale range	3072	0 1100 0000 0000	2.1875	2.1875
Positive Full-scale	4095	0 1111 1111 1111	2.5	2.5

Figure 2 shows the software configuration in iRADAnalyzer to place the ISL73148SEH into signed (bipolar) data format with Channel 0 selected for the data capture. The major differences between signed and unsigned modes are the connection of the COM pin and the V_{CM} voltage on the analog input. Regardless of the gain setting, the common mode voltage (V_{CM}) is constant at $V_{REF}/2$ when operating the ISL73148SEH in signed (bipolar) mode. When the selections are made in iRADAnalyzer, the hardware configuration is automatically updated on the ISL73148SEHEV1Z evaluation board except for the input amplitude, which you must adjust based on the PGA gain selection.

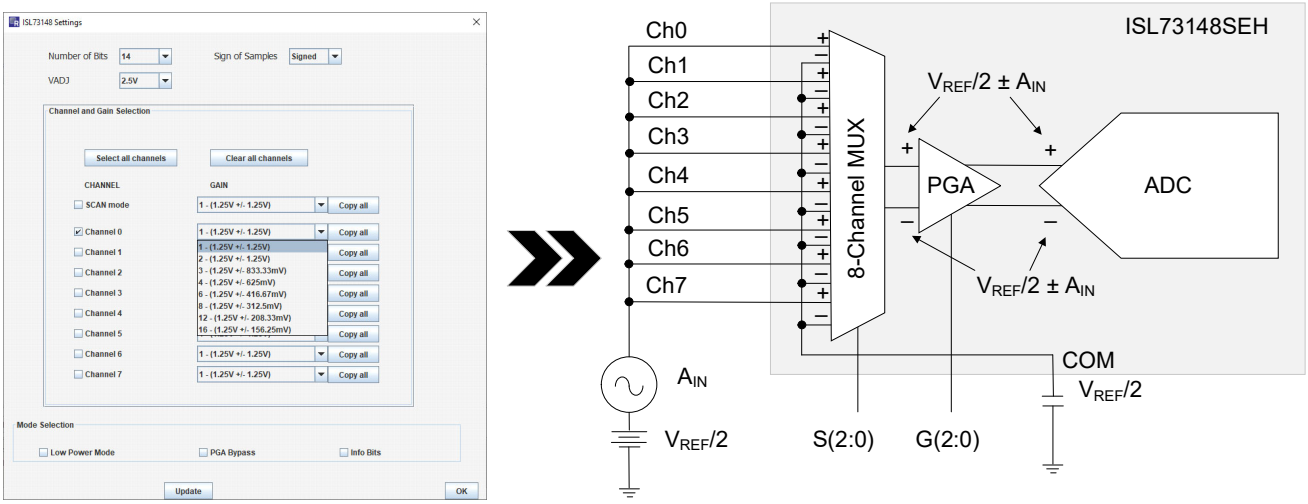

Figure 2. Signed (Bipolar) Data Format Software and Hardware Configuration for ISL73148SEHEV1Z

When operating the ISL73148SEH with a signed (bipolar) data format with a PGA gain ≥ 2, the full differential input range of the ADC core can be exercised. This is in contrast to operating the ISL73148SEH with signed data format with a PGA gain of 1 or with the PGA bypassed. As stated previously, when in signed data mode, the COM pin is decoupled to ground with a 0.1µF capacitor and the ISL73148SEH internal circuitry sets the voltage at the COM pin to $V_{REF}/2$. Recall that the negative analog inputs are all tied internally to the COM pin. Having the COM pin voltage at $V_{REF}/2$ allows the PGA to have a common mode voltage of $V_{REF}/2$ at both its positive and negative outputs. When the PGA gain is ≥ 2, the full differential input swing can be applied to the internal ADC core. In this case, the input voltages (A_{IN}) at each of the positive and negative inputs to the ADC can swing from 0V to 2.5V because the PGA gain is enabled to a value ≥ 2 providing for a differential input voltage range of 5V. This makes the full 14-bit range of the ADC available with an output code range of -8192 to +8191. Table 4 provides information on the relationship between the ADC input scale, digital code in decimal and binary, and the input voltage to the ADC for this mode of operation.

Table 4. Signed (Bipolar) Data Format for ISL73148SEH with PGA Gain ≥2

ADC Input Scale	Digital Code (Decimal)	Binary Digital Code Signed (Bipolar)	Input Voltage (V)	ADC Input Voltage (V-)	ADC Input Voltage (V+)
Negative full scale	-8192	10 0000 0000 0000	0	2.5	0
1/8 full-scale range	-6144	10 1000 0000 0000	0.3125	2.1875	0.3125
1/4 full-scale range	-4096	11 0000 0000 0000	0.625	1.875	0.625
3/8 full-scale range	-2048	11 1000 0000 0000	0.9375	1.5625	0.9375
Zero-scale - 1 LSB	-1	11 1111 1111 1111	1.25 - V_{LSB}	1.25 + V_{LSB}	1.25 - V_{LSB}
Zero-scale	0	00 0000 0000 0000	1.25	1.25	1.25
Zero-scale + 1 LSB	1	00 0000 0000 0001	1.25 + V_{LSB}	1.25 - V_{LSB}	1.25 + V_{LSB}
5/8 full-scale range	2048	00 0100 0000 0000	1.5625	0.9375	1.5625
3/4 full-scale range	4096	00 1000 0000 0000	1.875	0.625	1.875
7/8 full-scale range	6144	00 1100 0000 0000	2.1875	0.3125	2.1875
Positive Full-scale	8191	01 1111 1111 1111	2.5	0	2.5

3. Summary

The rad hard precision SAR ADCs from Renesas provide configurations that allows you to tailor the operation of the ADC to the requirements of the end application. In cases where an unsigned (unipolar) signal range is required, the rad hard ADC products provide the availability to perform the signal conversion to the digital domain in such a manner. For the case of the ISL73148SEH, the digital output format defaults to a signed data format to allow for maximum use of the ADC input range but also offers the flexibility of an unsigned data format in applications that require this type of data. The evaluation software and hardware make it simple for users to configure and evaluate these rad hard precision SAR ADCs in the required mode for the end application.

3.1 Next Steps

- Visit the Rad Hard Data Converters web page.

4. Revision History

Revision	Date	Description
1.00	Dec 5, 2022	Initial release.

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