Application Note

Power Solutions for Xilinx® Zynq Ultrascale+ ZU9EG

AN-PM-095

Abstract

This application note provides information on powering a Xilinx Zynq Ultrascale+ ZU9EG device with a power solution from Dialog Semiconductor.

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1 Terms and Definitions

GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
DA906x	Dialog DA9061, DA9062, DA9063, and DA9063L
DVC	Dynamic Voltage Control
DVS	Dynamic Voltage Scaling, analogous to DVC
MPSoC	Multiprocessor System-on-Chip
OTP	One-Time Programmable (memory)
RTC	Real-Time Clock
SoC	System-on-Chip

2 References

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[11] DA9063 Evaluation Boards Ordering Information, Dialog Semiconductor, Dialog Website Link

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[13] 176-20-B Power Board, schematic and BOM, Dialog Semiconductor Dialog Website Link

3 Introduction

The Xilinx Zynq Ultrascale+ MPSoC family of FPGA devices combine a powerful 64 processor system with programmable logic to meet the requirements of a wide range of applications. Fully realizing the performance of a Zync Ultrascale+ MPSoC device requires an optimized power management solution. Dialog Semiconductor have a range of flexible power management devices that can meet the requirements of the most demanding systems. The Dialog DA9063 PMIC, combined with one or more of the DA921x range of sub-PMICs, provides flexibility and control to match the requirements of most FPGA designs while maximizing performance and integration, and minimizing the PCB footprint.

4 Getting Started

This section introduces the basic power rail requirements of the Zynq Ultrascale+ ZU9EG devices along with the capabilities of the Dialog DA9063 PMIC and the DA9213 sub-PMIC, and shows why they are the perfect partners.

4.1 Power Supply Consolidation

The Xilinx Zync Ultrascale+ MPSoC devices require a range of power rails to release the full range of flexibility these devices offer. Depending on the configuration they may require between 5 and 16 different rails.

The Xilinx document, UG583 Ultrascale Architecture PCB design [12], defines four options for power supply consolidation, these are:

1. Always On: Optimized for cost
2. Always On: Optimized for Power and/or Efficiency
3. Always On: Optimized for PL Performance
4. Full Power Management Flexibility

Due to the available number of supply rails available with the DA9063/DA9213 combination, this document focuses on option 4, Full Power Management Flexibility, as this meets the widest number of use cases. Further consolidation may be possible, but would only be of value if the freed resources could be re-allocated within the end application.

4.2 The Zynq Ultrascale+ ZU9EG

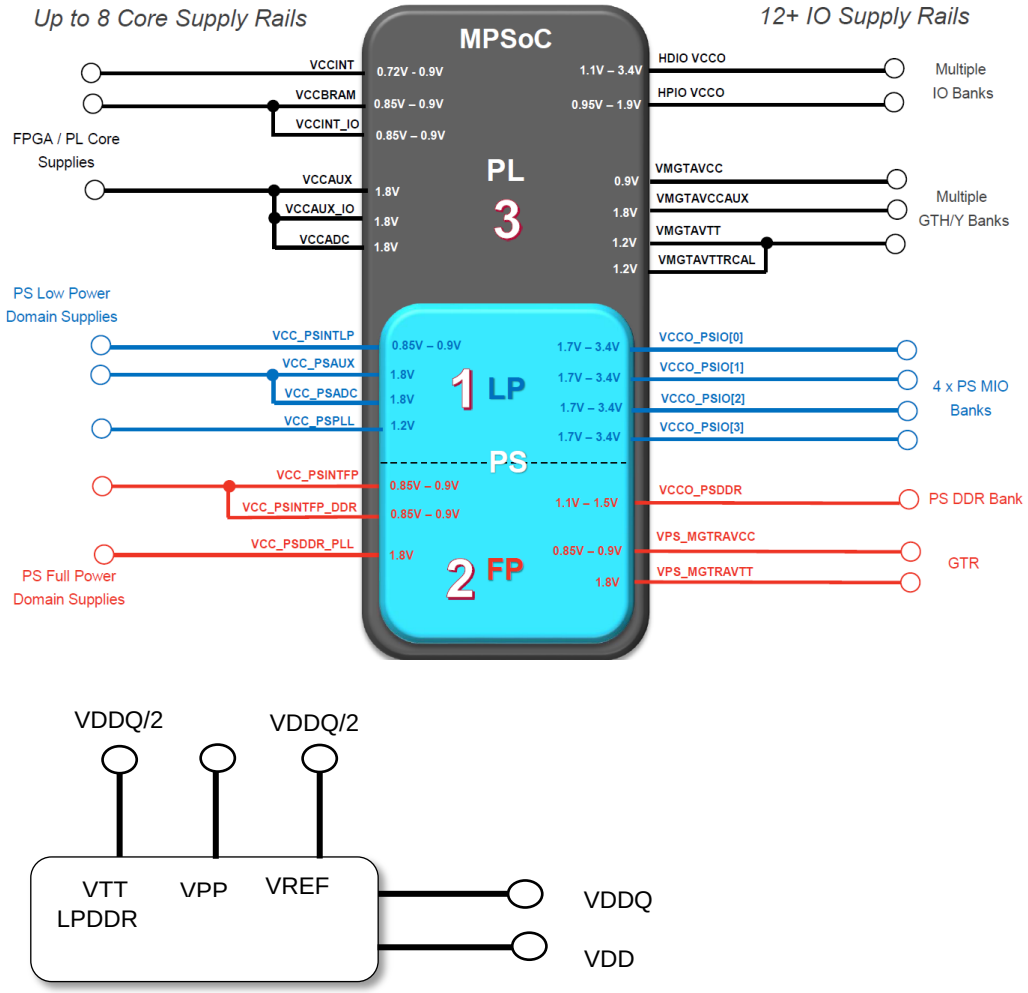

Figure 1: The Zynq Ultrascale+ ZU9EG Power Rail Requirements

Table 1: Zynq Ultrascale+ ZU9EG Power Rail Requirements

Power Rail	Voltage (V)	Current (A)
VCC_PSINTLP	0.85 to 0.9	0.4
VCC_PSAUX, VCC_PSADC	1.8	0.12
VCC_PSPLL	1.2	0.1
VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	User defined, 1.7 to 3.4	0.3
VCC_PSINTFP, VCC_PSINTFP_DDR	0.85	2.75
VCC_PSDDR_PLL	1.8	0.1
VCCO_PSDDR	User defined, 1.1 to 1.5	0.5
VCCINT, VCCINT_IO, VCCBRAM	0.85 to 0.9	20.8
VCCAUX, VCCAUX_IO, and VCCADC	1.8	1.12
VPS_MGTRAVCC	0.85 to 0.9	0.3

Power Rail	Voltage (V)	Current (A)
VPS_MGTRAVTT	1.8	0.1
VMGTAVTT (GTH), VMGTAVTT (GTY), VCC_VCU_PLL	1.2	2
VMGTAVCC (GTH), VMGTAVCC (GTY)	0.9	2
VMGTVCCAUX (GTH), VMGTVCCAUX (GTY)	1.8	0.1
VCCO (optional PL, PS I/O voltages)	User defined, 1.1 to 3.4	1.5

4.3 The Dialog DA9063

The Dialog DA9063 flexible PMIC integrates 6 bucks and 11 LDOs capable of supplying individual rails of up to 2.5 A. This device ideally matches many of the requirements of the Zynq family of devices.

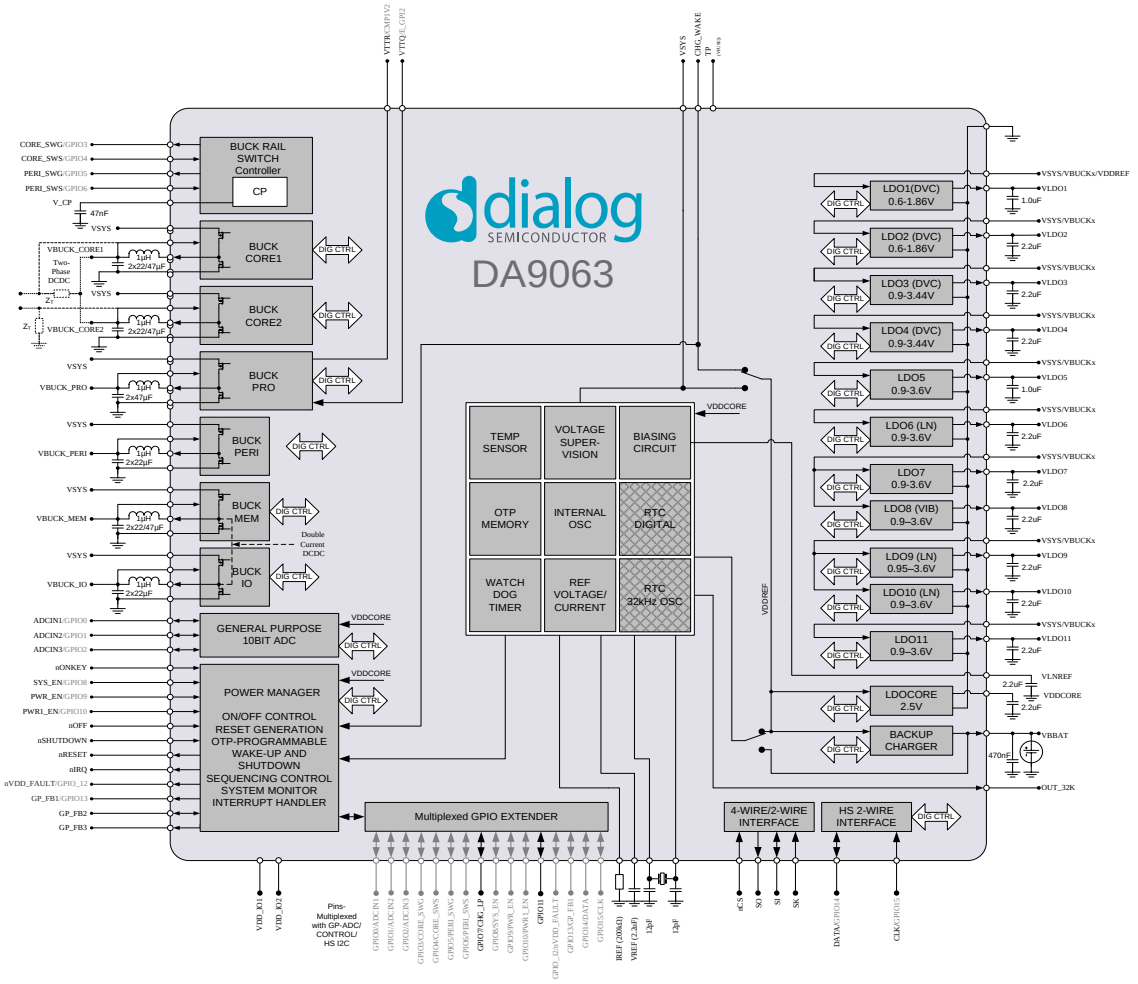

Figure 2: DA9063 Block Diagram

4.3.1 DA9063 Regulators

Table 2: DA9063 Regulator Summary

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max. Current (mA)	External Component	Notes
BUCKCORE1	VBUCKCORE1	0.3 to 1.57	1250/2500 (full-current mode)	1.0 µH/ 44 µF/ 88 µF	• DVC • 10 mV steps • < 0.7 V PFM mode only • 5 A dual-phase buck when combined with BUCKCORE2
BUCKCORE2	VBUCKCORE2	0.3 to 1.57	1250/2500 (full-current mode)	1.0 µH/ 44 µF/ 88 µF	• DVC • 10 mV steps • < 0.7 V PFM mode only • 5 A dual-phase buck when combined with BUCKCORE1
BUCKPRO	VBUCKPRO	0.53 to 1.80	1250/2500 (full-current mode)	1.0 µH/ 44 µF/ 88 µF	• DVC • 10 mV steps and VTT regulator mode • < 0.7 V PFM mode only
BUCKMEM	VBUCKMEM	0.8 to 3.34	1500	1.0 µH/ 44 µF	• DVC • 20 mV steps • 3 A (merge mode with BUCKIO)
BUCKIO	VBUCKIO	0.8 to 3.34	1500	1.0 µH/ 44 µF	• DVC • 20 mV steps • 3 A (merge mode with BUCKMEM)
BUCKPERI	VBUCKPERI	0.8 to 3.34	1500	1.0 µH/ 44 µF	• DVC • 20 mV steps
LDO1	VLDO1	0.6 to 1.86	100	1.0 µF	• DVC • 20 mV steps • Optional voltage tracking of BUCKCORE or BUCKPRO
LDO2	VLDO2	0.6 to 1.86	200	2.2 µF	• DVC • 20 mV steps
LDO3	VLDO3	0.9 to 3.44	200	2.2 µF	• Bypass mode • DVC • 20 mV steps
LDO4	VLDO4	0.9 to 3.44	200	2.2 µF	• Bypass mode • DVC • 20 mV steps
LDO5	VLDO5	0.9 to 3.6	100	1.0 µF	• 50 mV steps
LDO6	VLDO6	0.9 to 3.6	200	2.2 µF	• 50 mV steps, Low noise

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max. Current (mA)	External Component	Notes
LDO7	VLDO7	0.9 to 3.6	200	2.2 µF	• Bypass mode • 50 mV steps • Common supply with LDO8
LDO8	VLDO8	0.9 to 3.6	200	2.2 µF	• Bypass and switching vibration motor driver mode • 50 mV steps • Common supply with LDO7
LDO9	VLDO9	0.95 to 3.6	200	2.2 µF	• Low noise • 50 mV steps • OTP trimmed • Common supply with LDO10
LDO10	VLDO10	0.9 to 3.6	300	2.2 µF	• Low noise LDO • 50 mV steps • Common supply with LDO9
LDO11	VLDO11	0.9 to 3.6	300	2.2 µF	• Bypass mode • 50 mV steps
BACKUP	VBBAT	1.1 to 3.1	6	470 nF	• 100 mV/200 mV steps • Configurable charge current between 100 µA and 6000 µA • Reverse current protection (RCP)
LDOCORE	Internal PMIC supply	2.5 ±2 % accuracy	4	2.2 µF	• Internal LDO

4.4 The Dialog DA9213

The DA9213 is a member of the Dialog family of sub-PMICs. The sub-PMICs offer single or dual high-current outputs that are designed to complement the DA906x system PMICs. Utilizing a 3 MHz switching frequency (to allow the use of small 0.22 µH inductors) and a multi-phase architecture, the sub-PMICs offer impressive levels of current density in a small PCB footprint. The DA9213 can supply over 20 A from 0.3 V to 1.57 V in its quad phase configuration.

To maximize the voltage accuracy at the point of load, where it is needed, the DA9213 supports remote sensing capability.

The DA9213-88 variant is pre-configured with the 0.85 V target voltage required for the VCCINT rail. An optional output voltage of 0.9 V is selectable by tying a GPI high.

The DA9213 provides a power-good signal that indicates when the output is within 50 mV of its programmed voltage.

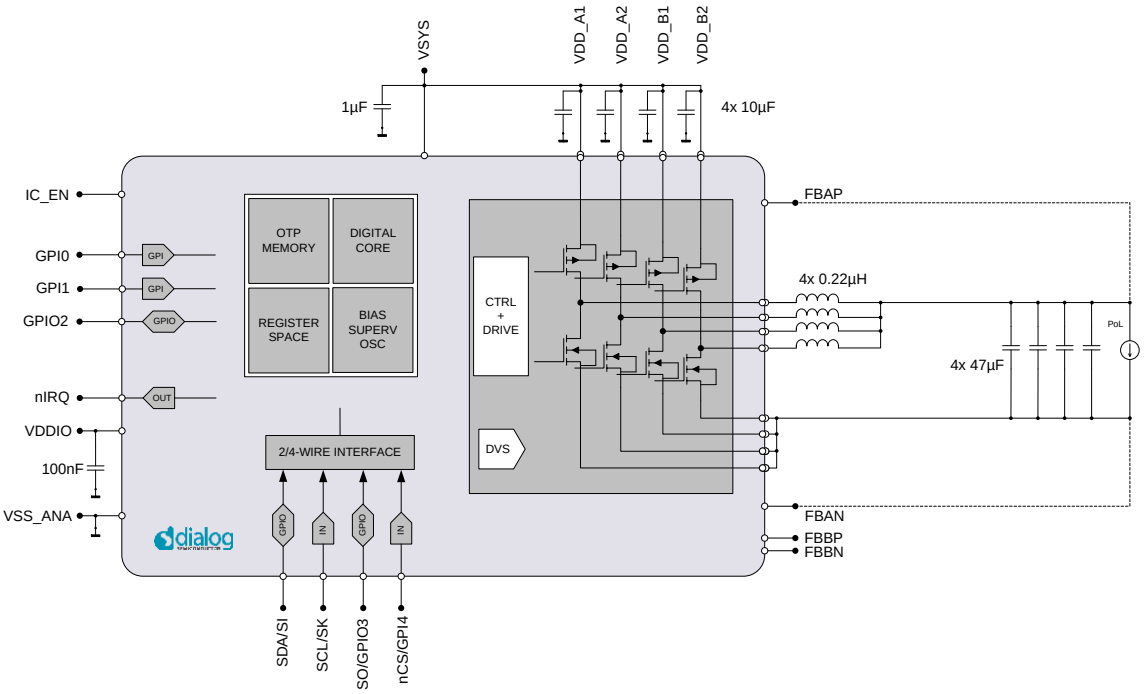

Figure 3: The DA9213 Sub-PMIC

For further information about the Dialog range of sub-PMICs, see the Dialog Semiconductor website.

4.5 Mapping to the DA9063 and DA9213

Comparing the ZU9EG power rail requirements from Table 1 with the DA9063 available regulators in Table 2 with the addition of the high current rail provided by the DA9213, it is clear to see that the DA9063 is a good match for designs using the ZU9EG.

The one rail that has not been included in this mapping is the always-on supply VCC_PSINTLP. Depending on the power functionality required, this should be supplied by a low I_Q regulator to optimize the low power performance of the system. Alternatively it may be possible to combine this with one of the existing 0.85 V rails, if low power performance is not required.

The flexible power sequencer at the heart of the DA9063 includes five GPIOs designed to enable additional regulators such as the DA9213. This feature allows the DA9063 to be the key device for a wide range of power solutions.

Mapping the ZU9EG on to the DA9063 and DA9213 is shown in Table 3.

Table 3: DA9063 and DA9213 Mapping for ZU9EG

Full Power Management Flexibility					DA9063/DA9213 Mapping	
	Power Regulator	**Possible Power Rail Consolidation**	**Voltage (V)**	**Current (A)**	**Resource**	**Current**
Required	1	VCC_PSINTLP	0.85	0.4	External	
	2	VCC_PSAUX, VCC_PSADC(1)	1.8	0.12	LDO3	0.2
	3	VCC_PSPLL,	1.2	0.1	LDO4	0.2
	4	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
	5	VCC_PSINTFP, VCC_PSINTFP_DDR	0.85	2.75	Core1	2.5
	6	VCC_PSDDR_PLL(2)	1.8	0.1	LDO5	0.1
	7	VCCO_PSDDR	USER	0.5	Mem	1.5
	8	VCCINT, VCCINT_IO, VCCBRAM	0.85	20.8	DA9213	20
User-Defined	9	VCCAUX, VCCAUX_IO, and VCCADC(1)	1.8	1.12	Peri	1.5
	10	VPS_MGTRAVCC	0.85	0.3	LDO1 and 2	0.1+0.2
	11	VPS_MGTRAVTT	1.8	0.1	LDO6	0.2
	12	VMGTAVTT (GTH), VMGTAVTT (GTY), and VCC_VCU_PLL	1.2	2	Core2	2.5
	13	VMGTAVCC (GTH) and VMGTAVCC (GTY)	0.9	2	Pro	2.5
	14	VMGTVCCAUX (GTH), and VMGTVCCAUX (GTY)	1.8	0.1	LDO7	0.2
Optional	15	Optional PL and PS I/O voltages(VCCO)	USER	1.5	IO	1.5

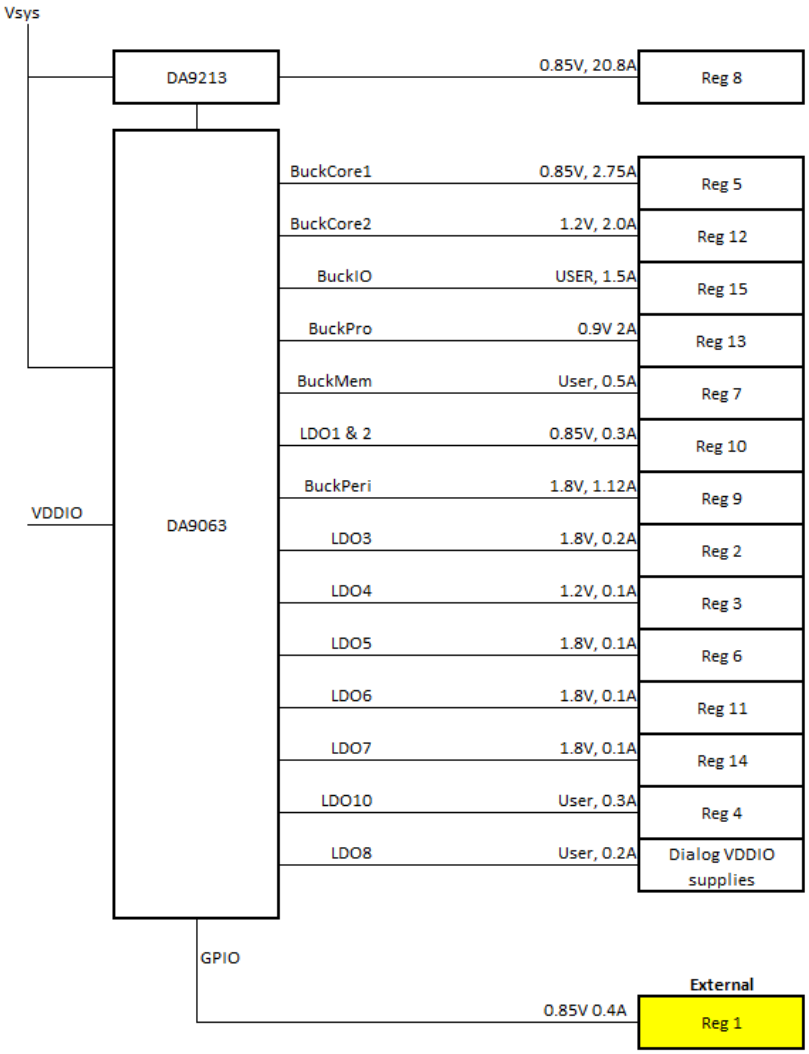

Figure 4: DA9063 and DA9213 Graphical Mapping

4.5.1 DA9063 and DA9213 PCB Footprint

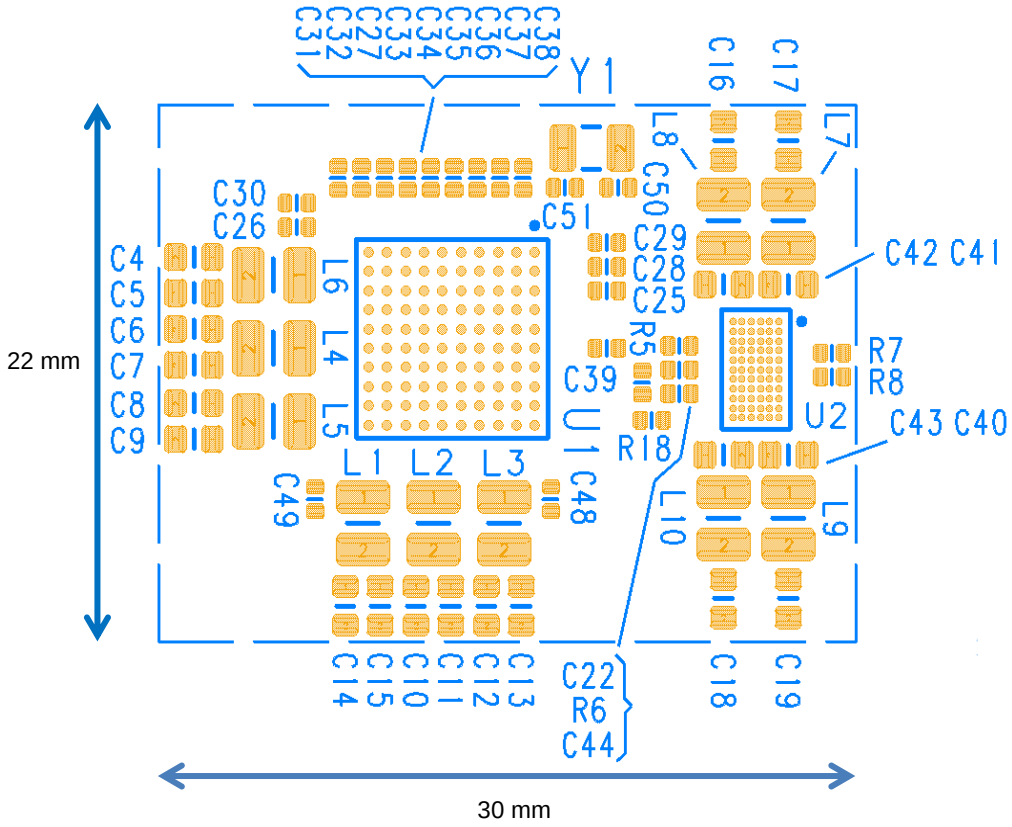

Figure 5: DA9063 and DA9213 Solution Footprint

The high level of integration, along with the 3 MHz switching frequency, results in a compact footprint. Figure 5 is an example footprint including all of the required passive components. The total area is less than 660 mm^2. This is achieved with nearly all of the components on the top side of the PCB, only a few input decoupling capacitors are located on the reverse side of the board, and without the use of over-aggressive placement. This area could be further reduced by more aggressive spacing rules. As shown, there is unused space in the calculated area. See the 176-20-B board data pack,[13], for more details. Table 4 has the full BOM for this design. Contact Dialog for example layout files.

4.5.2 Dialog 176-20-B Power Board

The Dialog power board was designed to demonstrate the small footprint possible with this design. As with all designs, there are trade-offs to be made. One good example would be the inductors selected. The TFM252010 inductors chosen have a very good current rating for the size of the device but, as with all smaller inductors, there is a cost in terms of the DCR. In this case, the 1 µH inductor has a typical DCR of 38 mΩ which impacts the efficiency of the buck. In systems where area is less critical, it is possible to select larger components with a DCR as low as 10 mΩ. This will have a noticeable impact on the regulator efficiency.

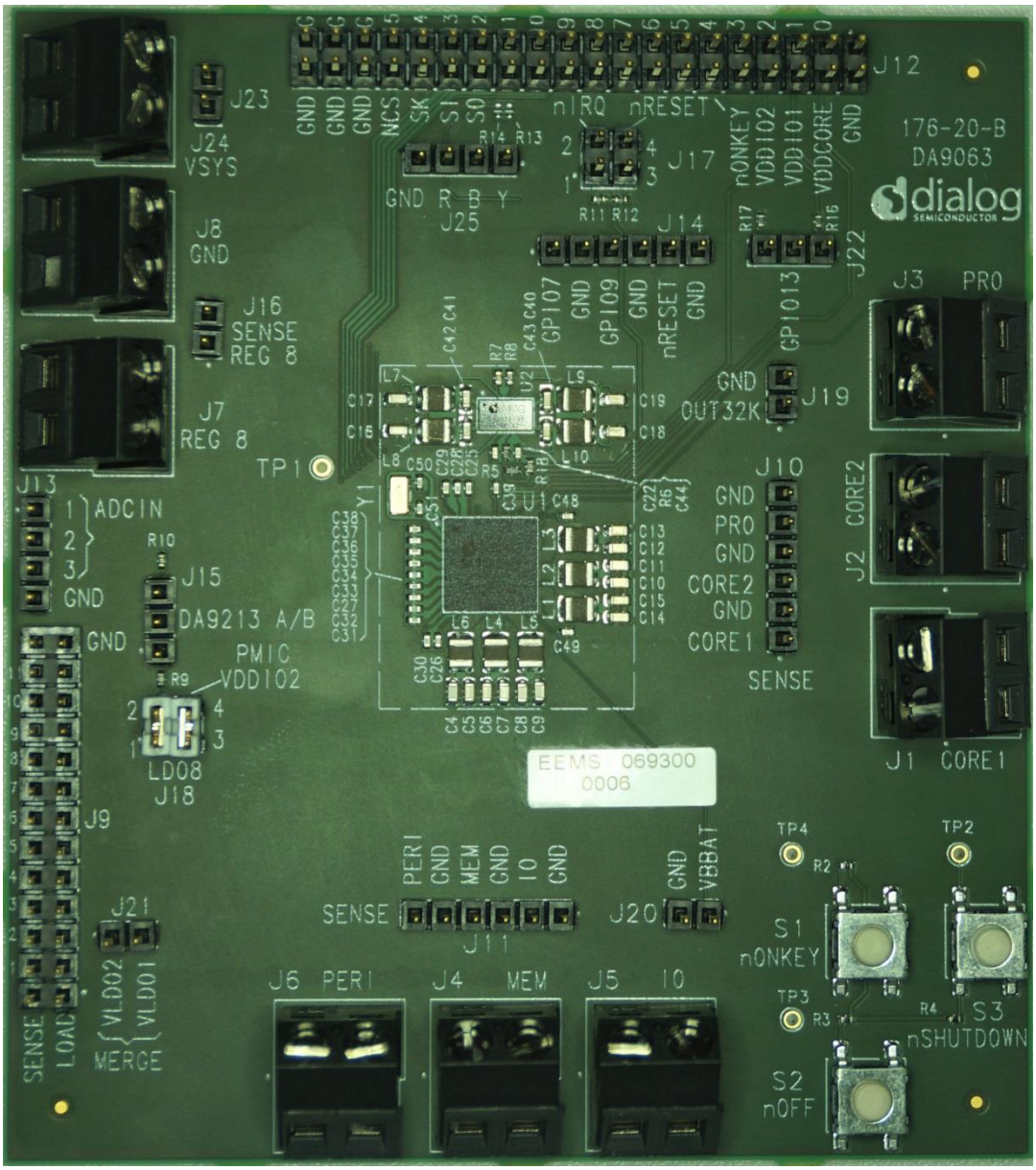

Figure 6: The Dialog 176-20-B Power Board

4.5.3 Typical Bill of Materials

Table 4: ZU9EG Example Bill of Materials

Qty	Ref Des.	Description	Footprint (EIA)	Value	Tolerance	Rating	Dielectric	Manufacturer	Manufacturer Part Number
1	C47	Capacitor	1005 (0402)	150 nF	10 %	10 V	X5R	Murata	GRM155 R61A154KE19
10	C10 to C19	Capacitor	1608 (0603)	47 uF	20 %	6.3 V	X5R	Murata	GRM188 R60J476ME15
6	L1 to L6	Inductor	2520 (1008)	1 uH	20 %	I_{SAT} = 3.5 A		TDK	TFM252010A-1R0M
1	U1	DA9063	BGA100					Dialog	DA9063
1	U2	DA9213	WLCSP 66					Dialog	DA9213
2	C50, C51	Capacitor	1005 (0402)	10 pF	5 %	50 V	COG /NPO	Murata	GRM155 5C1H100JA01D
1	C48	Capacitor	1005 (0402)	47 nF	10 %	10 V	X5R	Murata	GRM155 R61A473KA01D
3	C44 to C46	Capacitor	1005 (0402)	100 nF	10 %	10 V	X5R	Murata	GRM155 R61A104KA01D
1	C49	Capacitor	1005 (0402)	470 nF	10 %	10 V	X5R	Murata	GRM155 R61A474KE15D
6	C22 to C27	Capacitor	1005 (0402)	1 uF	10 %	10 V	X5R	Murata	GRM155 R61A105KE15D
6	C20, C21, C40 to C43	Capacitor	1608 (0603)	10 uF	20 %	6.3 V	X5R	Murata	GRM188 R60J106ME47D
9	C1 to C9	Capacitor	1608 (0603)	22 uF	20 %	6.3 V	X5R	Murata	GRM188 R60J226MEA0J
12	C28 to C39	Capacitor	1005 (0402)	2.2 uF	20 %	6.3 V	X5R	Murata	GRM155 R60J225ME15
2	R5, R6	Capacitor	1005 (0402)	10 kF	1 %	63 mW		Yageo	RC0402 FR-0710KL
2	R11, R12	Capacitor	1005 (0402)	20 kF	1 %	63 mW		Yageo	RC0402 FR-0720KL
9	R2 to R4, R9, R10, R15 to R18	Resistor	1005 (0402)	100 kΩ	1 %	63 mW		Yageo	RC0402 FR-07100KL
1	R1	Resistor	1005 (0402)	200 kΩ	1 %	63 mW		Yageo	RC0402 FR-07200KL
2	R7, R8	Resistor	1005 (0402)	0R		63 mW		Vishay	CRCW0402-0000Z0ED
4	L7 to L10	Inductor	2520 (1008)	220 nH	20 %	I_{SAT} = 8 A		TDK	TFM252010 ALMAR22MTAA
1	Y1	XTAL 12.5 pF		32768 Hz	±20 PPM			Micro Crystal	CM7V-T1A 32.768KHZ 12.5PF

4.5.4 Flexibility

The DA9063 has 11 LDO regulators, so there are two spare regulators that can be used to provide power to additional parts of the system, or to supply additional voltage IO domains.

The voltage required to supply the VCCINT rail is either 0.85 V or 0.9 V, this can be configured by pulling a GPIO high or low to select the required voltage.

For more demanding designs, Dialog has a range of system and sub-PMICs that can be used to build a power tree that will meet your needs, see http://www.dialog-semiconductor.com/power-management for more information.

4.5.5 DA9063 Additional Features

Along with the buck and LDO regulators, the DA9063 includes a range of additional features that are vital to most systems.

- Supply rail qualification: The DA9063 can monitor the incoming supply to prevent the system starting if a suitable supply is not available. A warning is generated if the supply falls below a programmed level.
- Low power RTC with alarm function and 32 kHz output.
- System RESET control: The DA9063 provides a system RESET signal that is used to hold the system in RESET until all supply rails are available.
- System Watchdog: The watchdog can be used to reset the system if it becomes unresponsive.
- Voltage monitoring via the onboard ADC.
- Up to 16 configurable GPIOs.
- For automotive designs, both the DA9063 and the DA9213 are available in automotive variants.

4.5.6 Working with the DA9063

There are multiple options available for working with the DA9063. The 176-20-B board provides the configuration described in this section and is ideal for evaluating the capabilities of the DA9063 along with the DA9213. This board can be controlled via a supplied USB to I^2C interface and the DA9063 GUI.

For full custom development activities, it is recommended to use one of the DA9063 evaluation kits. For more details of the different configuration of boards available, see the document DA9063 Evaluation Board Ordering Information [11].

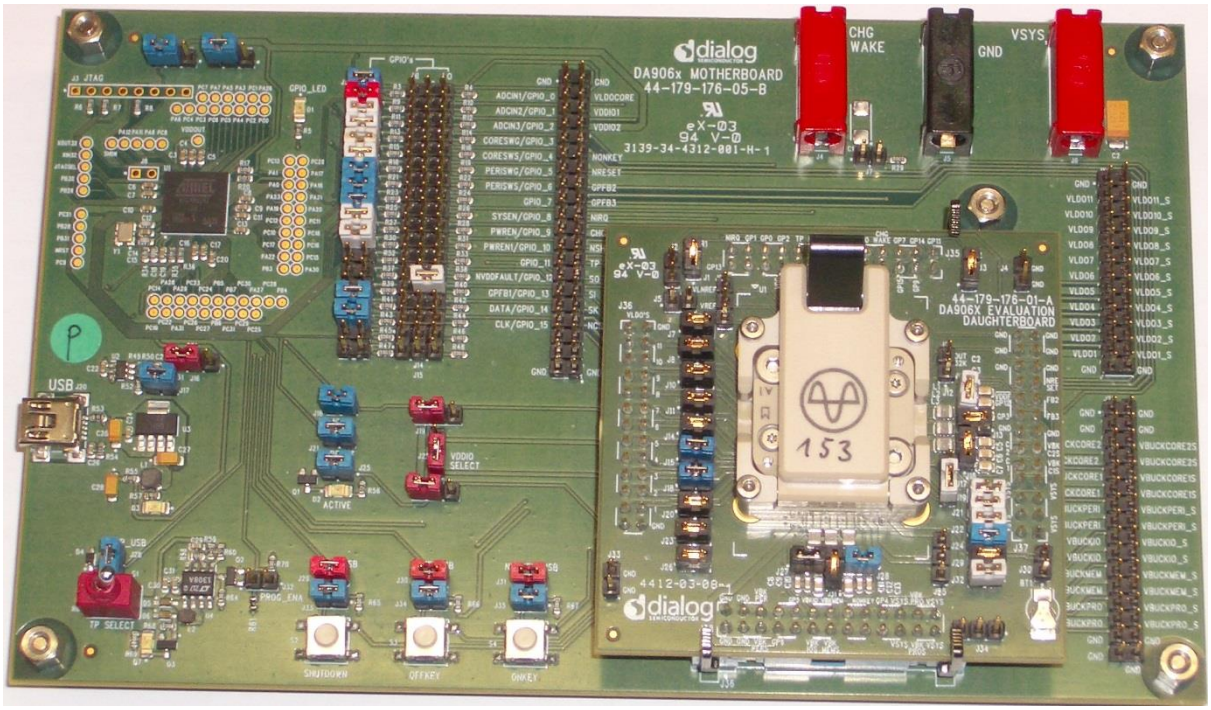

Figure 7: DA9063 Socket Evaluation board

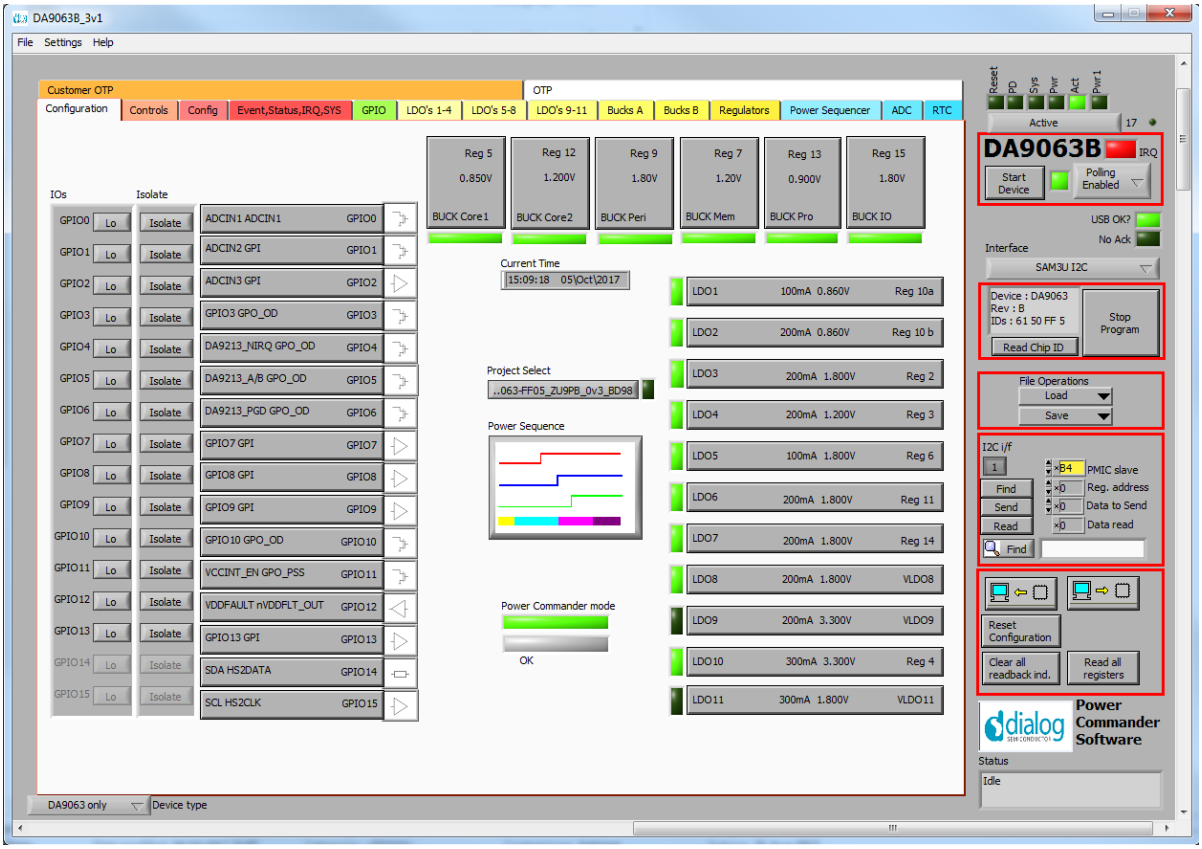

Figure 8: DA9063 Power Commander GUI

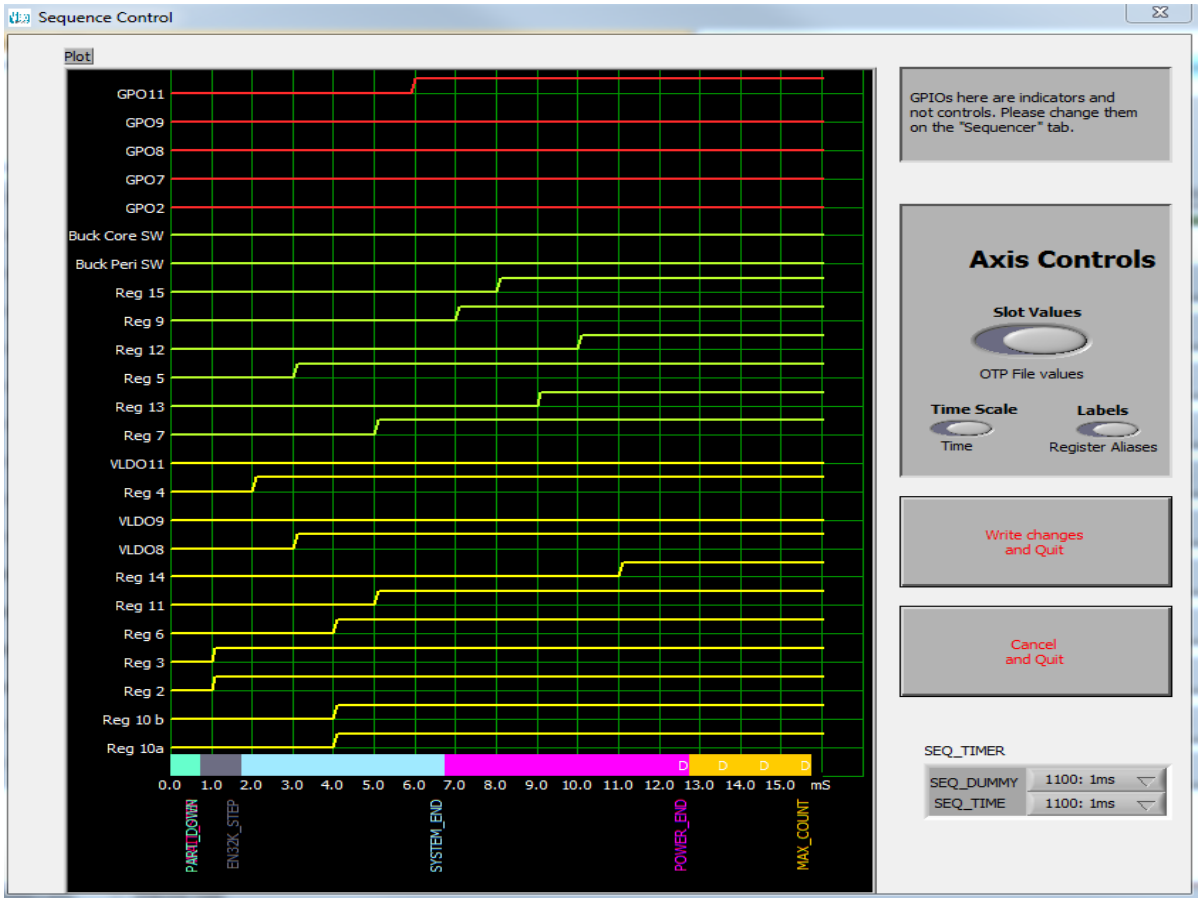

Figure 9: Power Commander Drag and Drop Sequence Tool

4.6 Alternative Mappings

As previously mentioned it is possible to support alternative power supply consolidation options. This section provides mappings that address the three options proposed by Xilinx in [12].

4.6.1 Always On: Optimized for Cost

Table 5: Always On: Optimized for Cost Mapping

Always On: Cost Optimized					Dialog Mapping	
	Power Regulator	**Possible Power Rail Consolidation**	**Voltage (V)**	**Current (A)**	**Resource**	**Current (A)**
Required	1	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM	0.85	23.95	Dual DA9210	24
	2	VCC_PSAUX, VCC_PSADC(1), VCC_PSDDR_PLL(2), VCCAUX, VCCAUX_IO, and VCCADC(1)	1.8	1.34	Peri	1.5
	3	VCCO_PSDDR	USER	0.5	Mem	1.5
	4	VCC_PSPLL, VMGTAVTT (GTH), and VMGTAVTT (GTY)	1.2	2.1	Core1	2.5
	5	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
User-defined	6	VPS_MGTRAVCC	0.85	0.3	LDO1 and 2	0.1+0.2
	7	VPS_MGTRAVTT, VMGTVCCAUX (GTH), and VMGTVCCAUX (GTY)	1.8	0.2	LDO3	0.2
	8	VMGTAVCC (GTH) and VMGTAVCC (GTY)	0.9	2	Pro	2.5
	9	Optional PL and PS I/O voltages	USER	1.5	IO	1.5
Spare			Core2, LDO4, 5, 6, 7, 8, 9, 11			

4.6.2 Always On: Optimized for Power and/or Efficiency

Table 6: Always On: Optimized for Power and/or Efficiency Mapping

Always On: Power/Efficiency Optimized					Dialog Mapping	
	Power Regulator	**Possible Power Rail Consolidation**	**Voltage (V)**	**Current (A)**	**Resource**	**Current (A)**
Required	1	VCCINT	0.72/0.85	20	DA9213	20
	2	VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, VCCBRAM	0.85	3.95	Core1 and 2	5
	3	VCC_PSAUX, VCC_PSADC(1), VCC_PSDDR_PLL(2), VCCAUX, VCCAUX_IO, and VCCADC(1)	1.8	1.34	Peri	1.5
	4	VCCO_PSDDR	USER	0.5	Mem	1.5
	5	VCC_PSPLL, VMGTAVTT (GTH), and VMGTYAVTT (GTY)	1.2	2.1	Pro	2.5
	6	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
User-defined	7	VPS_MGTRAVCC	0.85	0.3	LDO1 and 2	0.1+0.2
	8	VPS_MGTRAVTT, VMGTVCCAUX (GTH), and VMGTYVCCAUX (GTY)	1.8	0.2	LDO3	0.2
	9	VMGTAVCC (GTH) and VMGTYAVCC (GTY)	0.9	2	External	
	10	Optional PL and PS I/O voltages	USER	1.5	IO	1.5
Spare			LDO4, 5, 6, 7, 8, 9, 11			

4.6.3 Always On: Optimized for PL Performance

Table 7: Always On: Optimized for PL Performance Mapping

Always On: PL Performance Optimized					Dialog Mapping	
	Power Regulator	**Possible Power Rail Consolidation**	**Voltage (V)**	**Current (A)**	**Resource**	**Current (A)**
Required	1	VCCINT, VCC_PSINTFP, VCC_PSINTLP, VCC_PSINTFP_DDR, VCCINT_IO, and VCCBRAM	0.9	23.95	Dual DA9210	24
	2	VCC_PSAUX, VCC_PSADC, VCC_PSDDR_PLL,VCCAUX, VCCAUX_IO, and VCCADC	1.8	1.34	Peri	1.5
	3	VCCO_PSDDR	USER	0.5	Mem	1.5
	4	VCC_PSPLL, VMGTAVTT (GTH), and VMGTYAVTT (GTY)	1.2	2.1	Core1	2.5
	5	VCCO_PSIO[0:3] assuming all PS I/Os run from same voltage	USER	0.3	LDO10	0.3
User-defined	6	VPS_MGTRAVTT, VMGTVCCAUX (GTH), and VMGTYVCCAUX (GTY)	1.8	0.2	LDO3	0.2
	7	VPS_MGTRAVCC	0.85	0.3	LDO1 and 2	0.1+0.2
	8	VMGTAVCC (GTH) and VMGTYAVCC (GTY)	0.9	2	Pro	2.5
	9	Optional PL and PS I/O voltages (VCCO)	USER	1.5	IO	1.5
Spare			Core2, LDO4, 5, 6, 7, 8, 9, 11			

4.7 Bench Measurements

This section provides some basic performance measurements made using the DA9063 Evaluation kit. The following measurements are included:

- power-on sequence
- buck efficiency
- static load regulation.
- buck transient load regulation
- reference measurements

4.7.1 Power-On Sequence

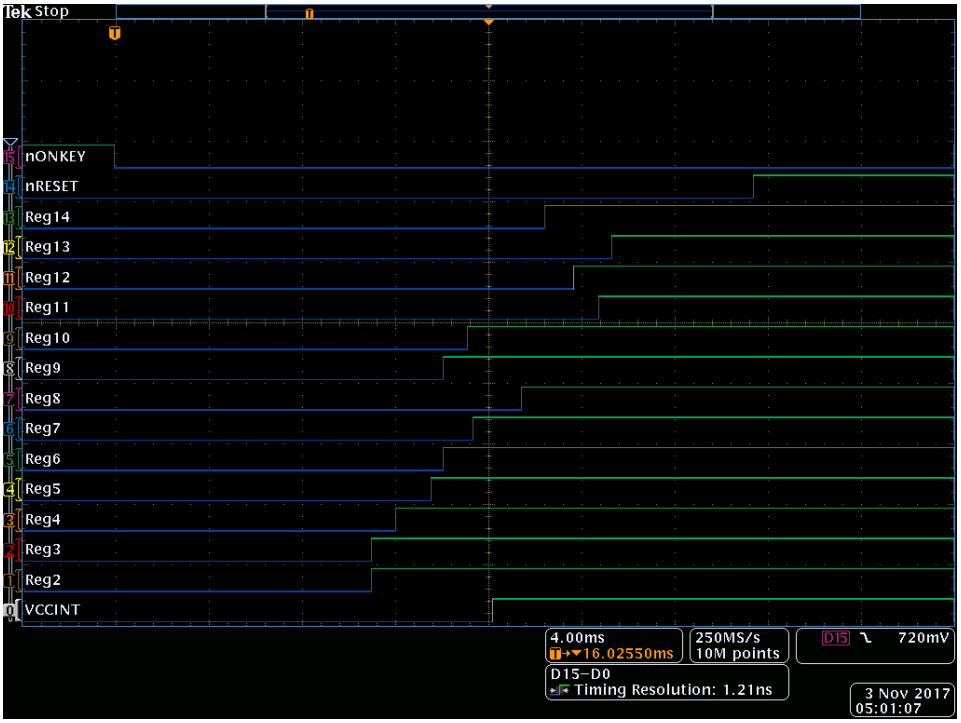

Figure 10: Example ZU9 Power-On Sequence

4.7.2 Buck Efficiency

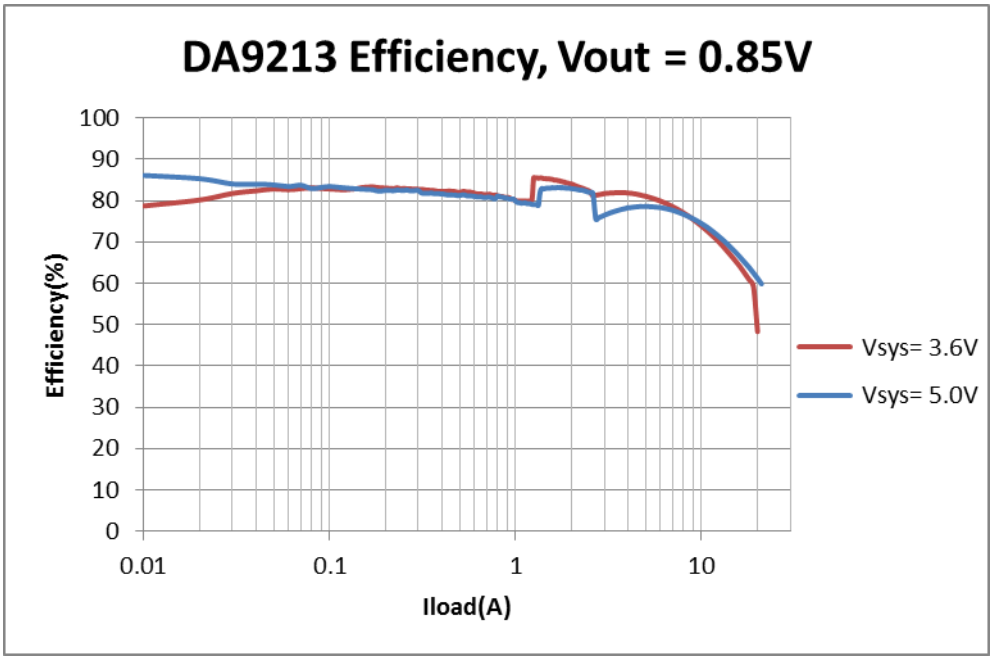

Figure 11: DA9213 Efficiency, V_{OUT} = 0.85 V and V_{IN} = 5 V and 3.6 V

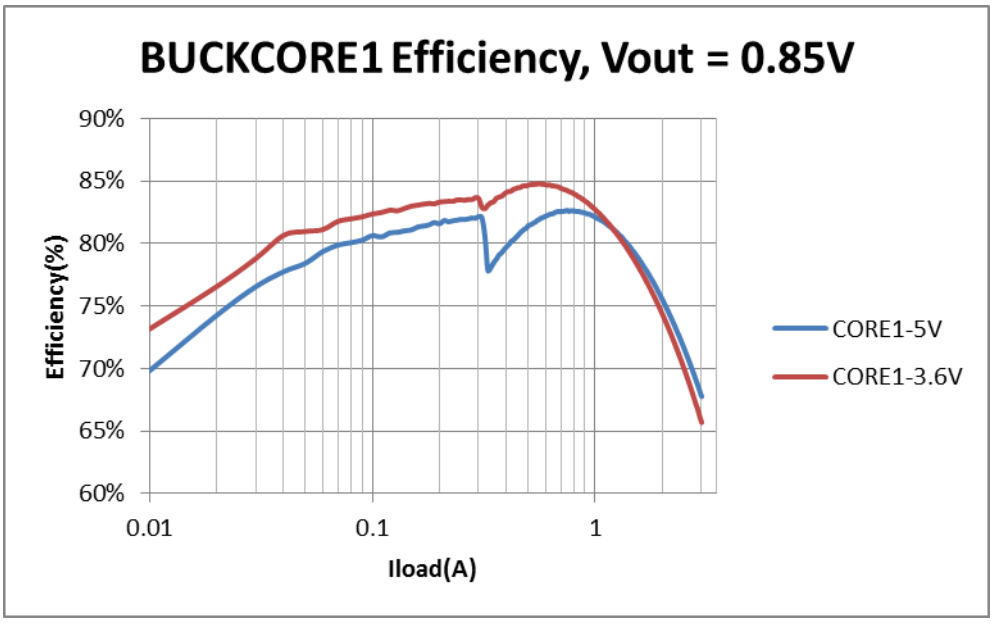

Figure 12: BUCKCORE1 Efficiency with V_{OUT} = 0.85 V and V_{IN} = 5 V and 3.6 V

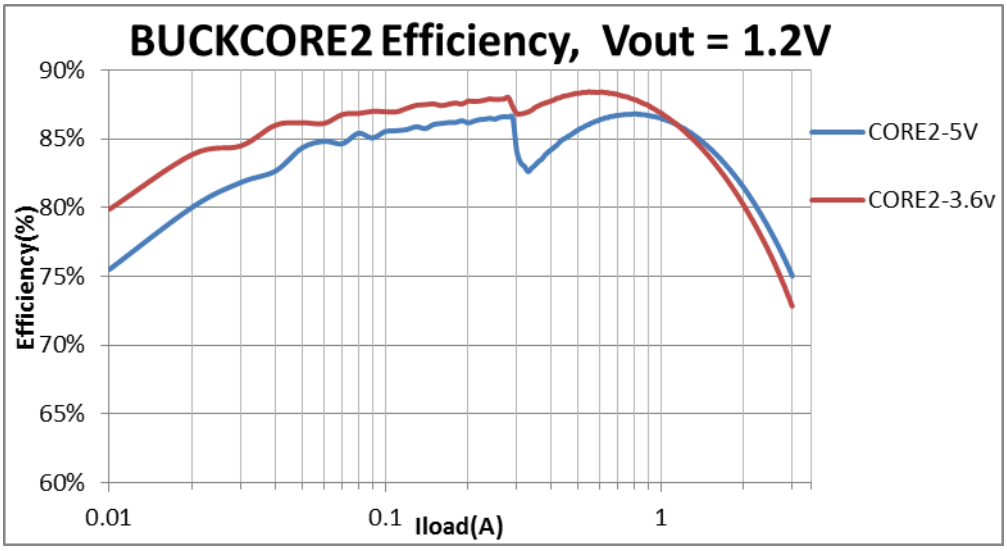

Figure 13: BUCKCORE2 Efficiency with V_{OUT} = 1.2 V and V_{IN} = 5 V and 3.6 V

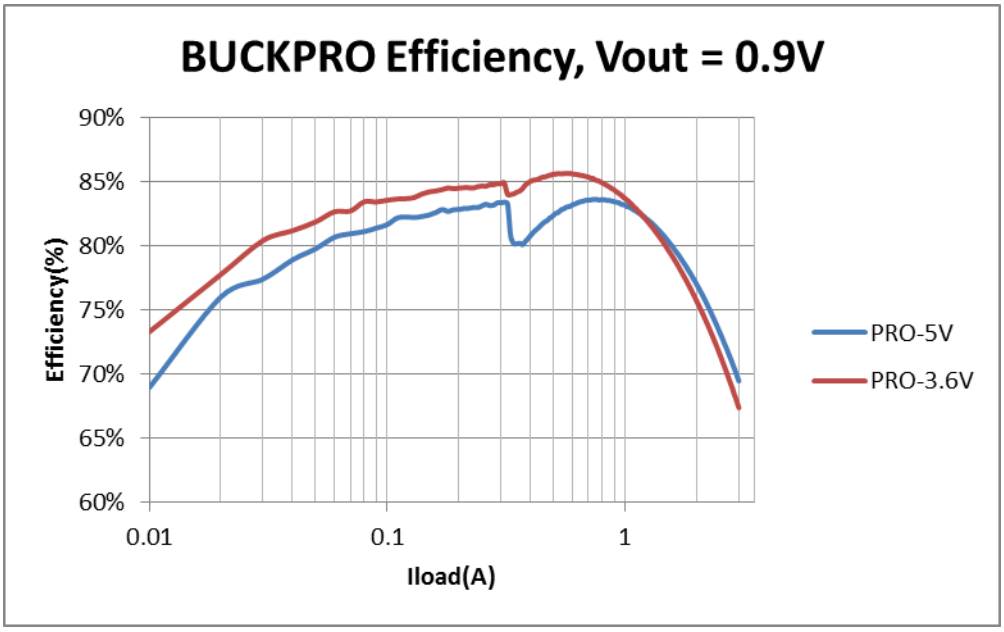

Figure 14: BUCKPRO Efficiency with V_{OUT} = 0.9 V and V_{IN} = 5 V and 3.6 V

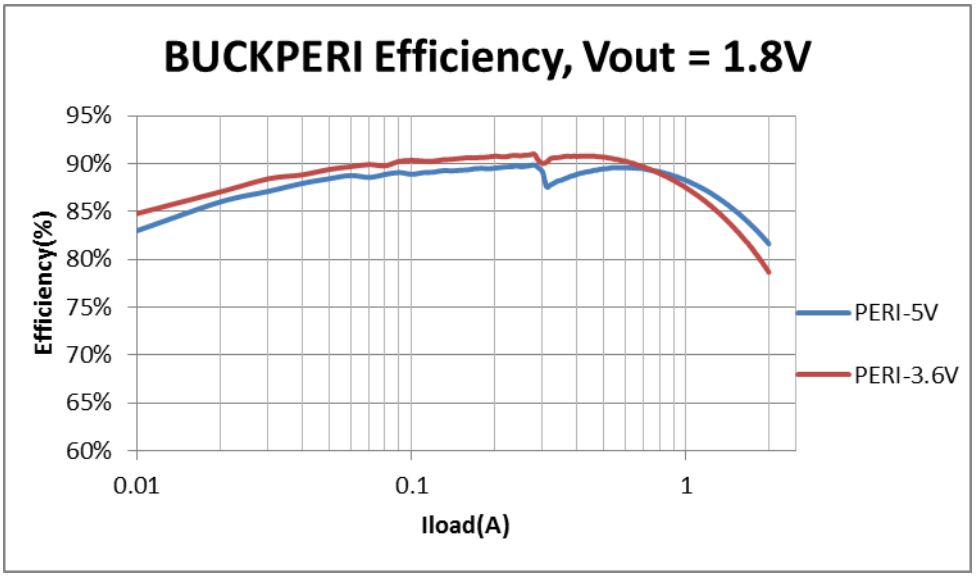

Figure 15: BUCKPERI Efficiency with V_{OUT} = 1.8 V and V_{IN} = 5 V and 3.6 V

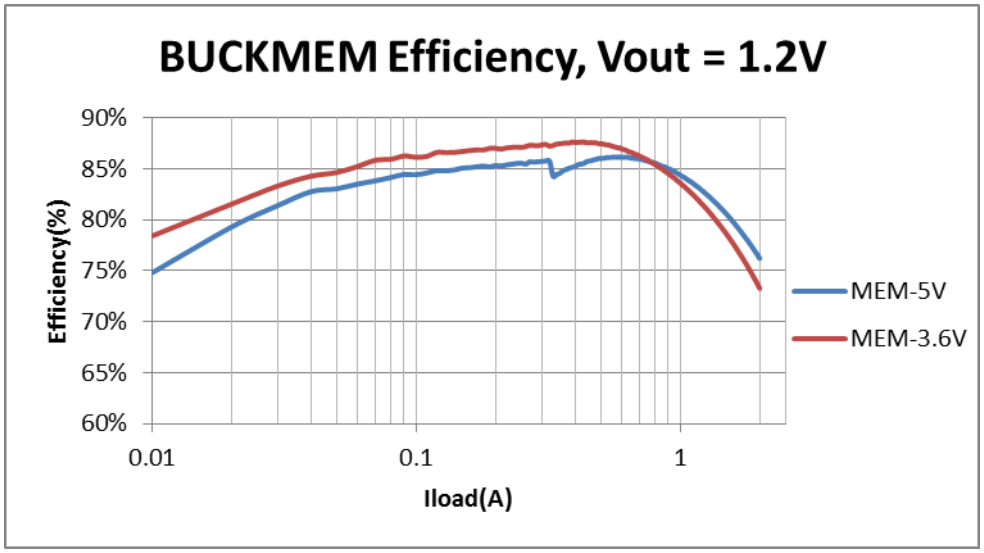

Figure 16: BUCKMEM Efficiency with V_{OUT} = 1.2 V and V_{IN} = 5 V and 3.6 V

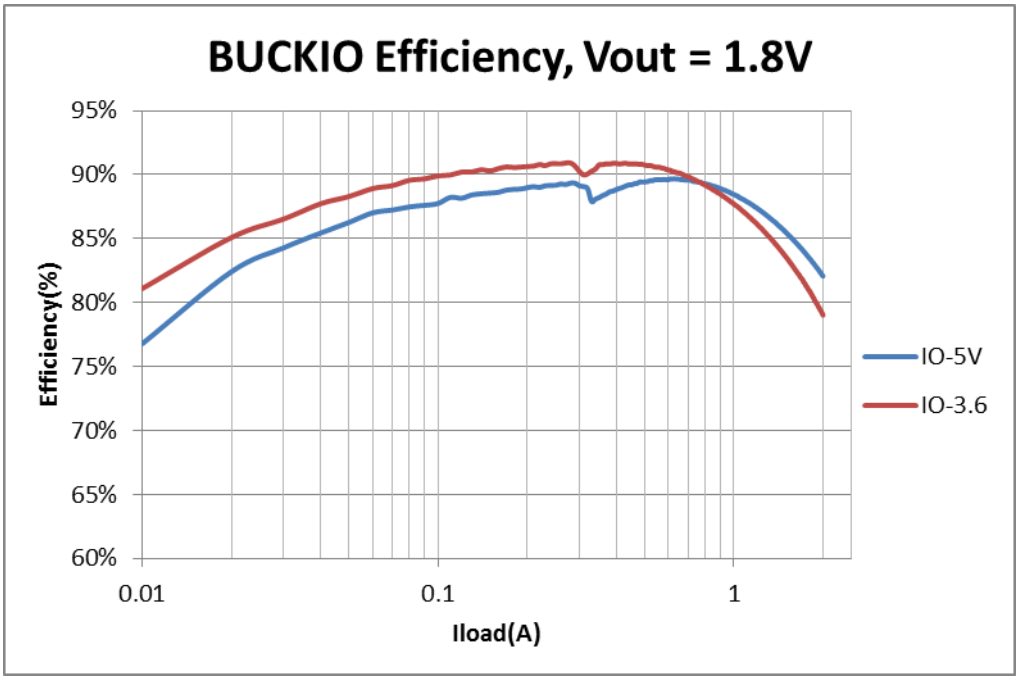

Figure 17: BUCKIO Efficiency with V_{OUT} = 1.8 V and V_{IN} = 5 V and 3.6 V

4.7.3 Static Load Regulation

The following static load regulation plots show the variation on the output voltage over a sweep of the load. The buck regulators are running in Auto mode. The change in slope at approximately 300 mA is where the buck transitions from PFM to PWM.

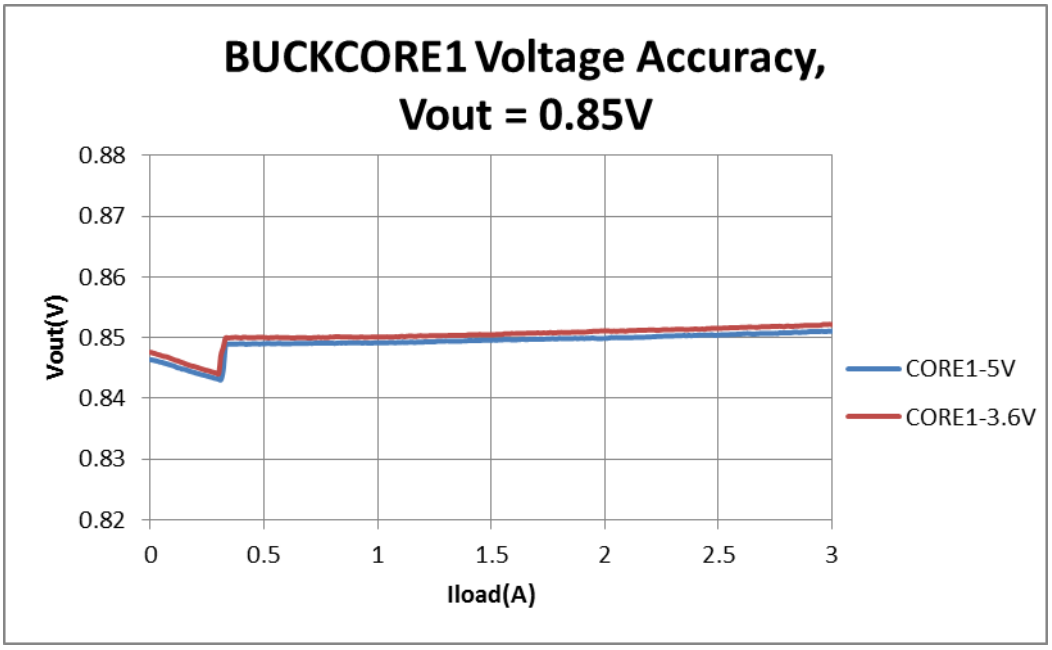

Figure 18: BUCKCORE1 Static Load Regulation

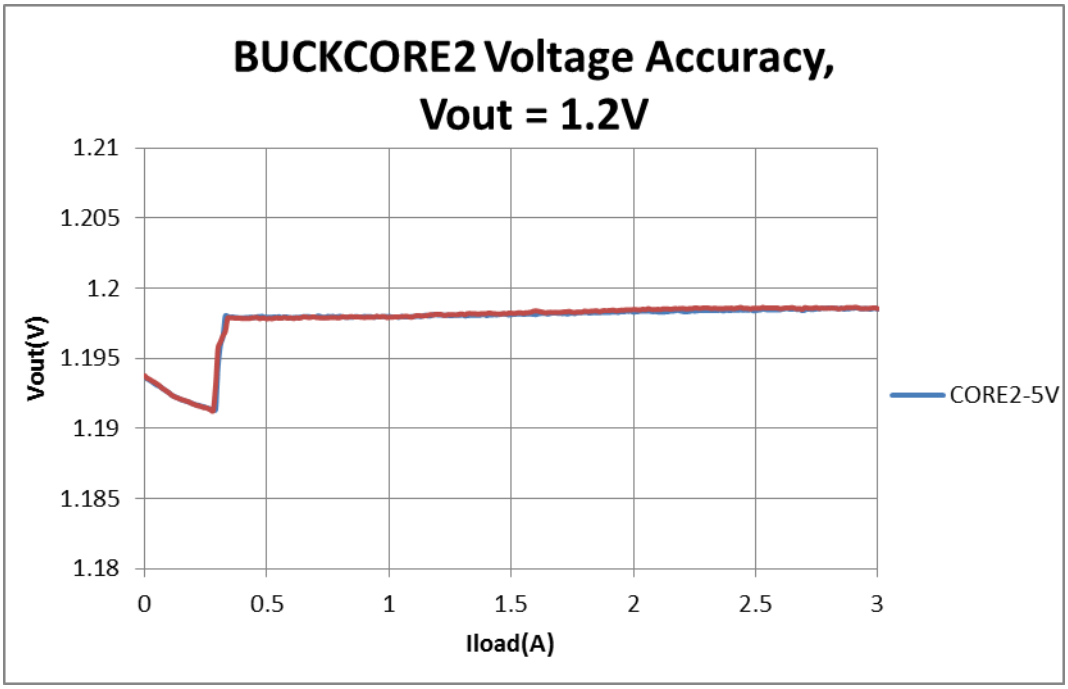

Figure 19: BUCKCORE2 Static Load Regulation

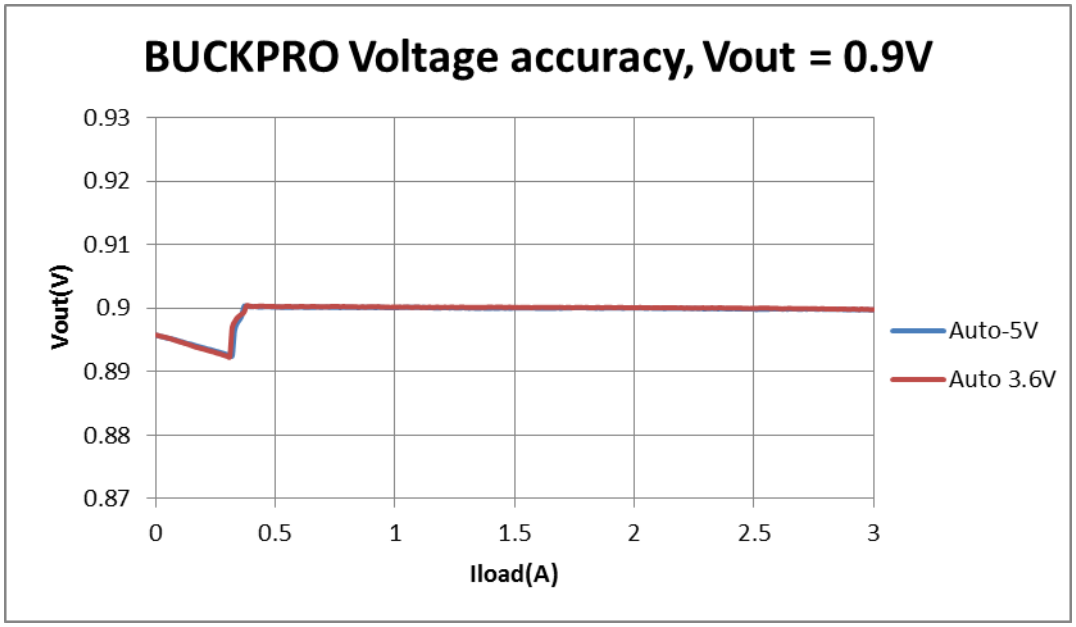

Figure 20: BUCKPRO Static Load Regulation

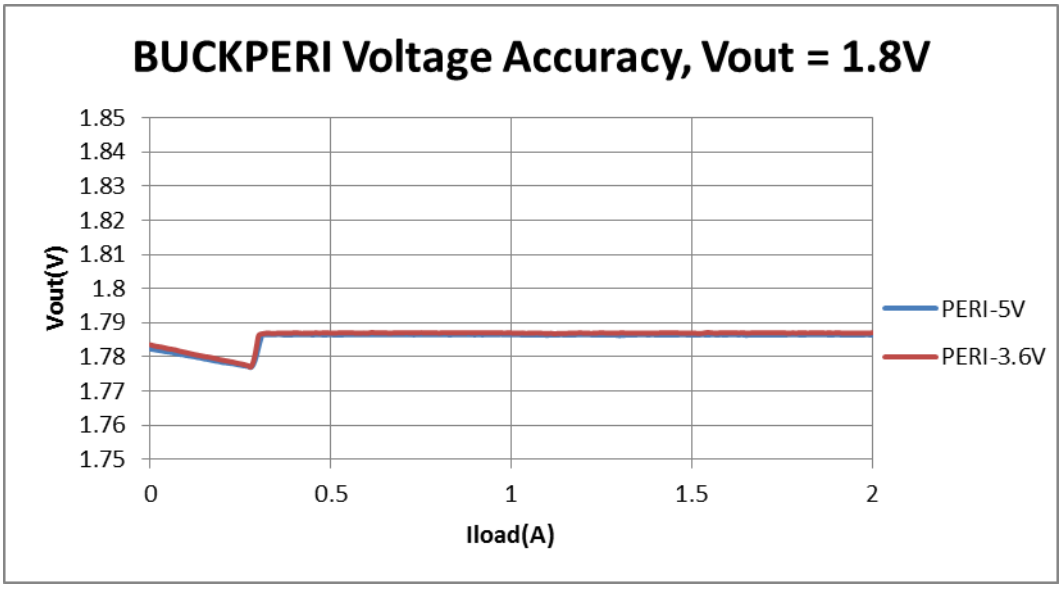

Figure 21: BUCKPERI Static Load Regulation

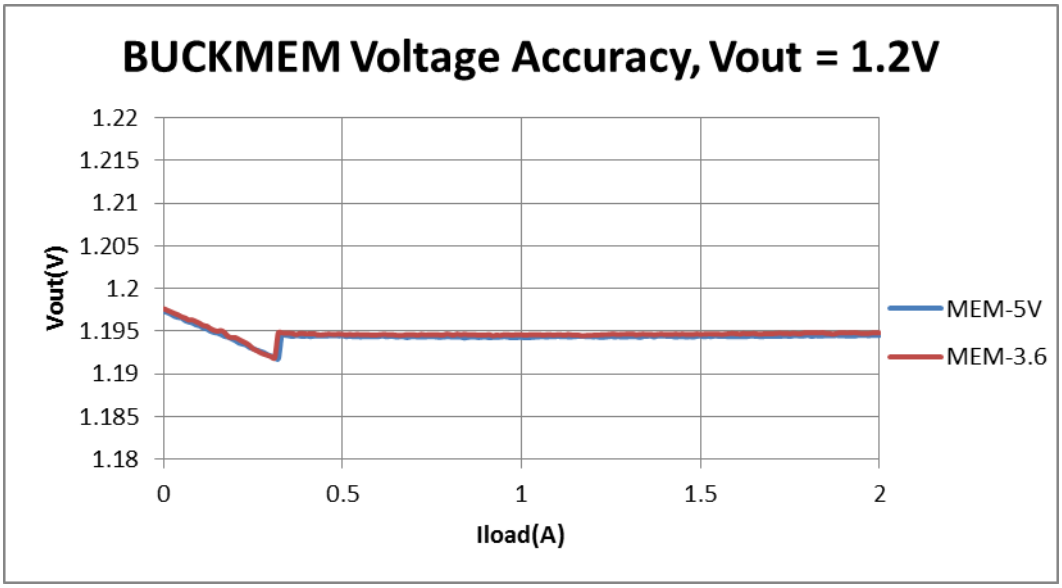

Figure 22: BUCKMEM Static Load Regulation

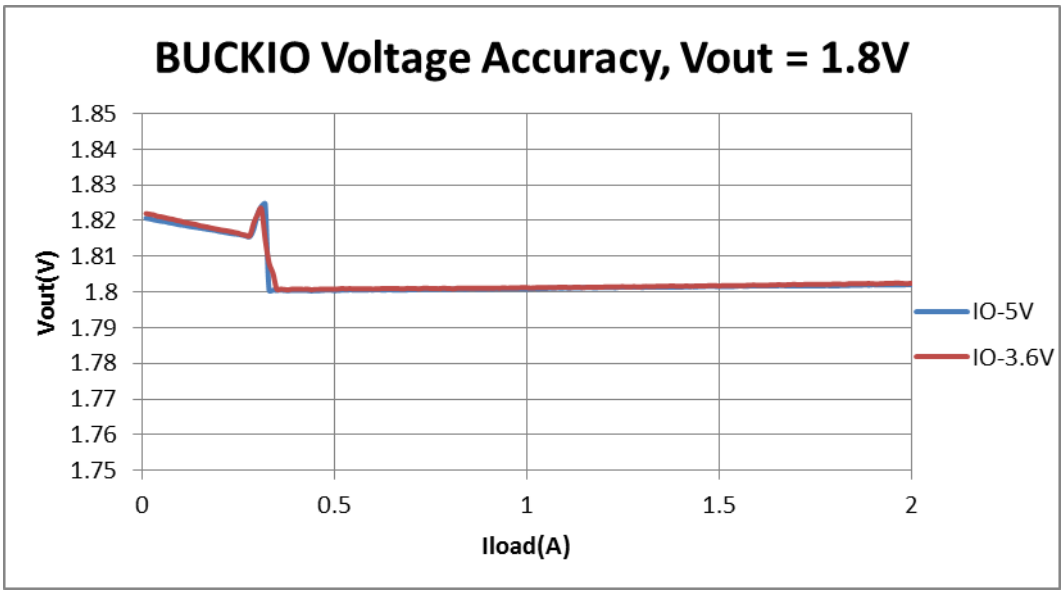

Figure 23: BUCKIO Static Load Regulation

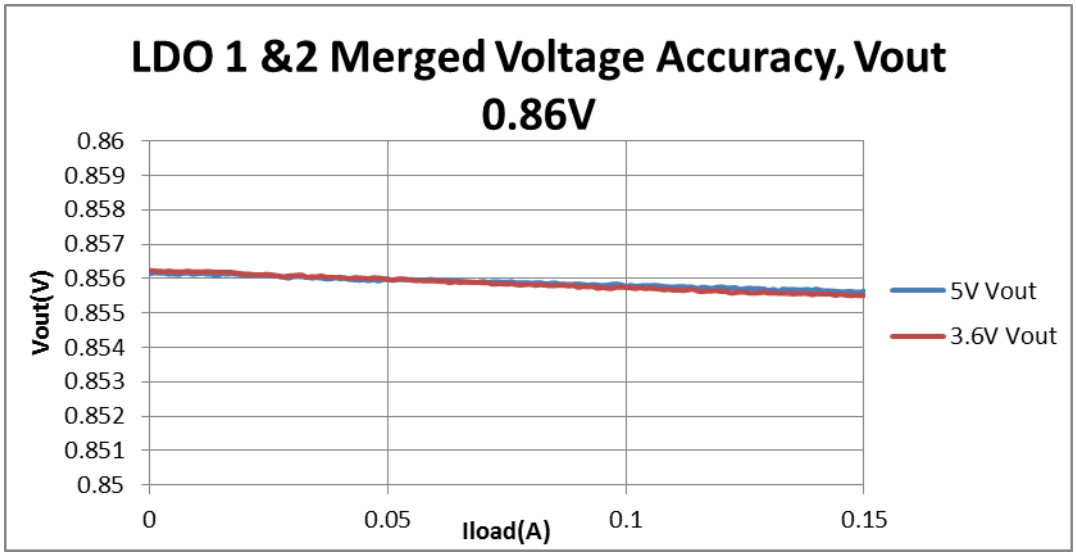

Figure 24: LDO1 and 2 Static Load Regulation

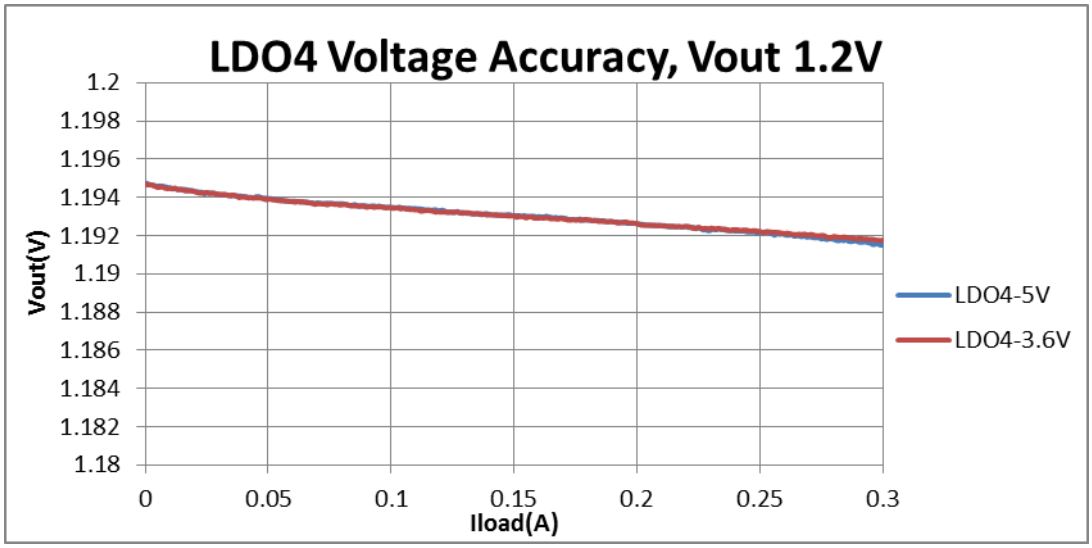

Figure 25: LDO4 Static Load Regulation

4.7.4 Buck Transient Load Regulation

For the transient measurements in this section, the oscilloscope was configured as follows:

- Channel1 (Yellow) shows the regulator output.
  The output was AC coupled, The buck was set to 0.95 V. The Min and Max measurements show the maximum excursion during the transient event.
- Channel 2 (Blue) shows the transient load being applied.
  The Low and High measurements were configured to show the levels of the current pulse waveform. The pulse duration was set to 10 µs.
- Channel 3 (Magenta), where shown, displays the DC coupled output voltage.
- The “a” and “b” horizontal cursors show the Xilinx specification limits for the specific voltage rail.

In Table 8, Table 9, and Table 10, the results are given for the transient as a percentage of the maximum load for the regulator. For example, 625 mA is 25 % of 2.5 A. The ±3 % specification is then calculated in mV for comparison against the measured result.

Table 8: VCCINT Transient Load Results

VCCINT (V)	Transient Load			Spec. Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3 %	3 %	Min	Max
0.85	2960	5920	15	-25.5	25.5	-10.48	13.97
0.85	2900	7900	25	-25.5	25.5	-18.64	22

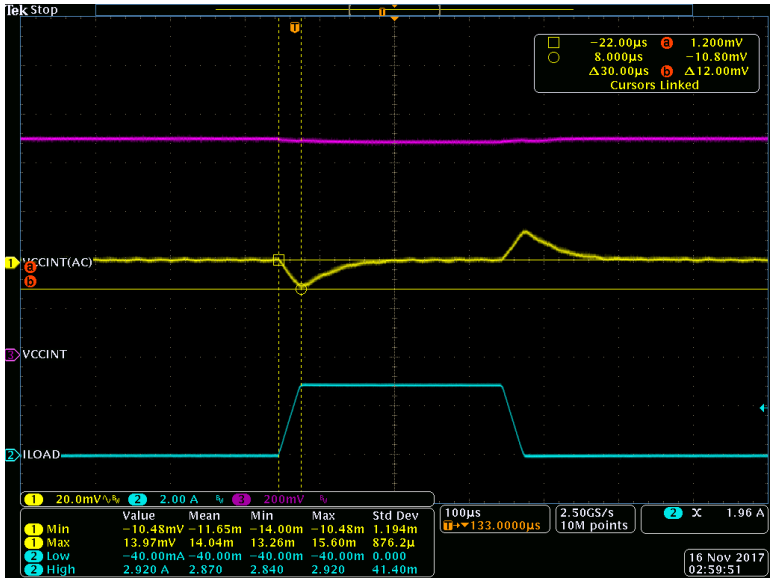

Figure 26: VCCINT (DA9213) Transient Response, 2960 mA to 5920 mA Step

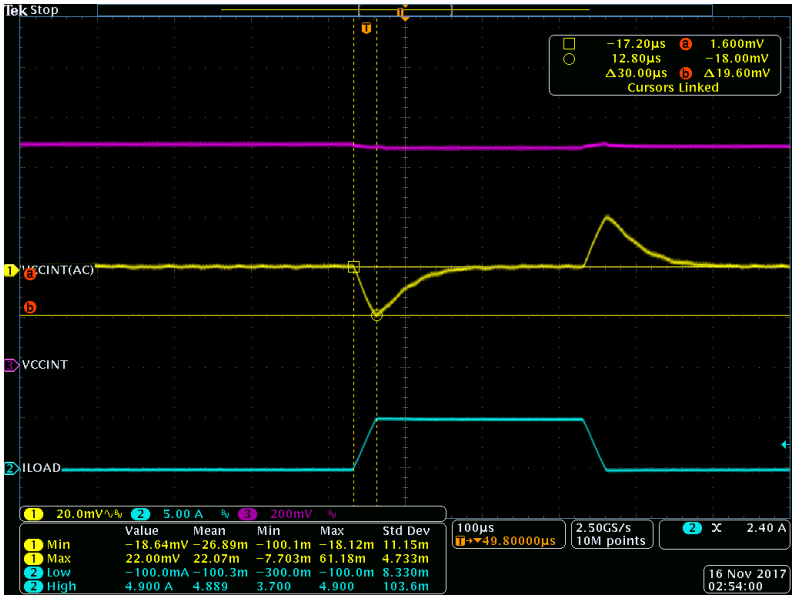

Figure 27: VCCINT (DA9213) Transient Response, 5 A Step

Table 9: VDDQ Transient Load Results

VDDQ (V)	Transient Load			Spec. Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3 %	3 %	Min	Max
1.2	230	830	40	-36	36	-19.35	20.11
1.35	230	830	40	-40.5	40.5	-19.06	20.54

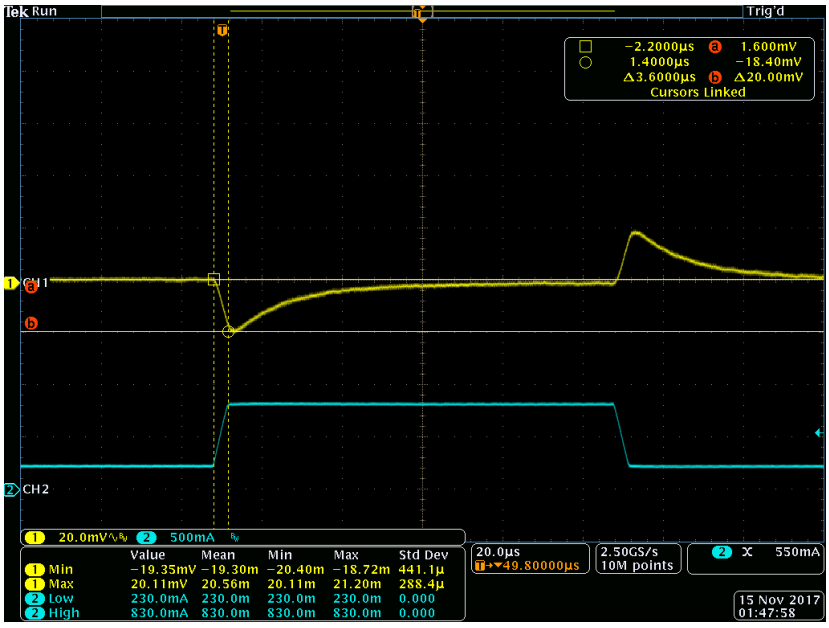

Figure 28: VDDQ (BUCKMEM) Transient Response, V_{OUT} = 1.2 V, 0.6 A Step

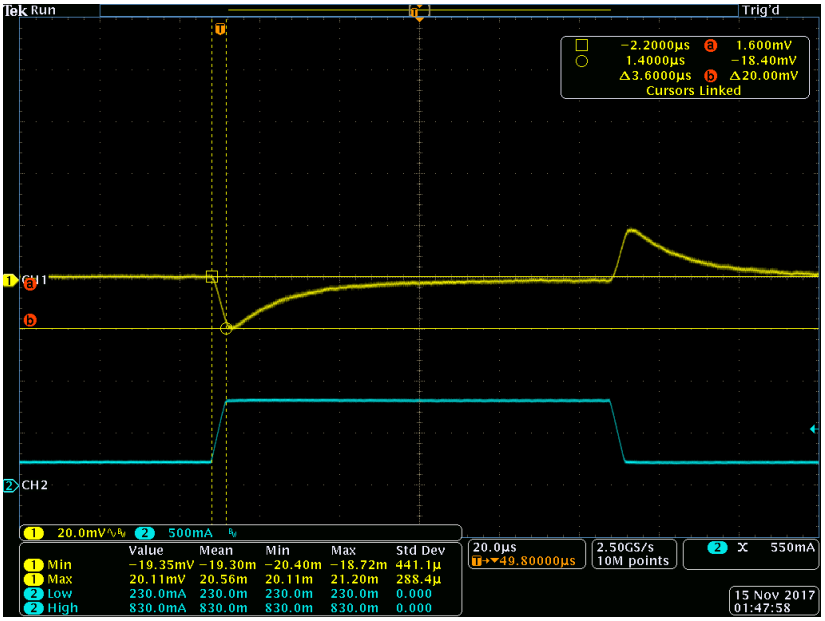

Figure 29: VDDQ (BUCKMEM) Transient Response, V_{OUT} = 1.35 V, 0.6 A Step

Table 10: VCCIO Transient Load Results

VCCIO (V)	Transient Load			Spec. Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3 %	3 %	Min	Max
2.5	310	910	40	-75	75	-19.77	22.68
2.5	310	1060	50	-75	75	-25.16	27.85
3.3	310	910	40	-99	99	-21.05	23.95
3.3	310	1060	50	-99	99	-25.85	28.97

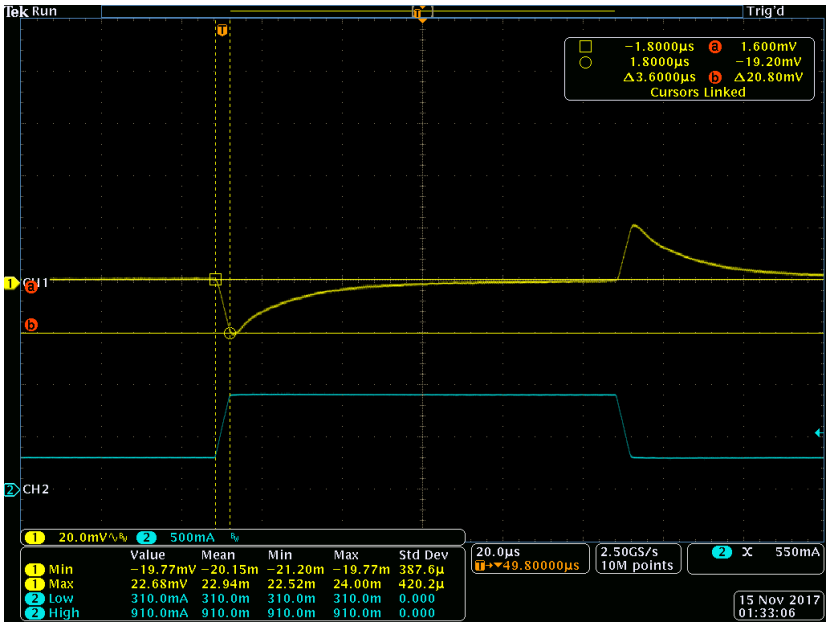

Figure 30: VCCIO (BUCKIO) Transient Response, V_{OUT} = 2.5 V, 0.6 A Step

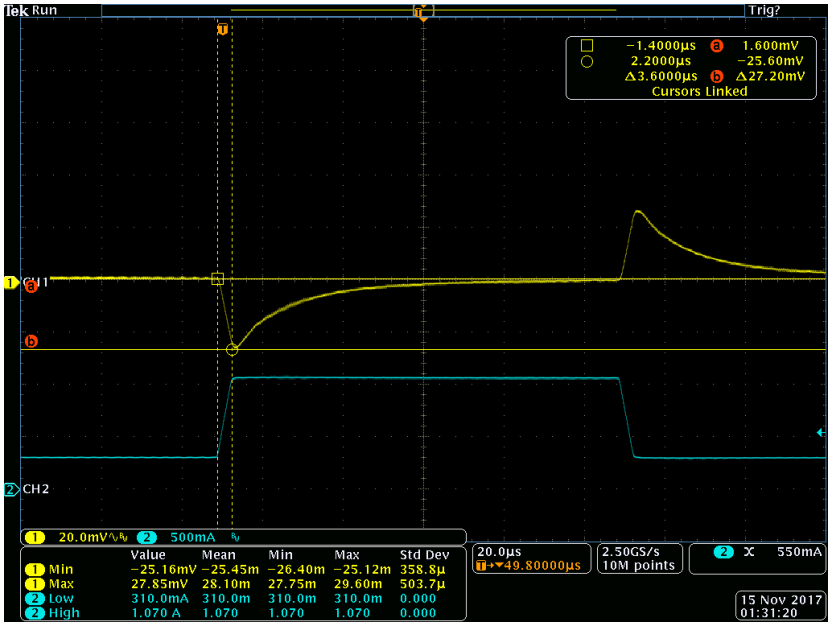

Figure 31: VCCIO (BUCKIO) Transient Response, V_{OUT} = 2.5 V, 0.76 A Step

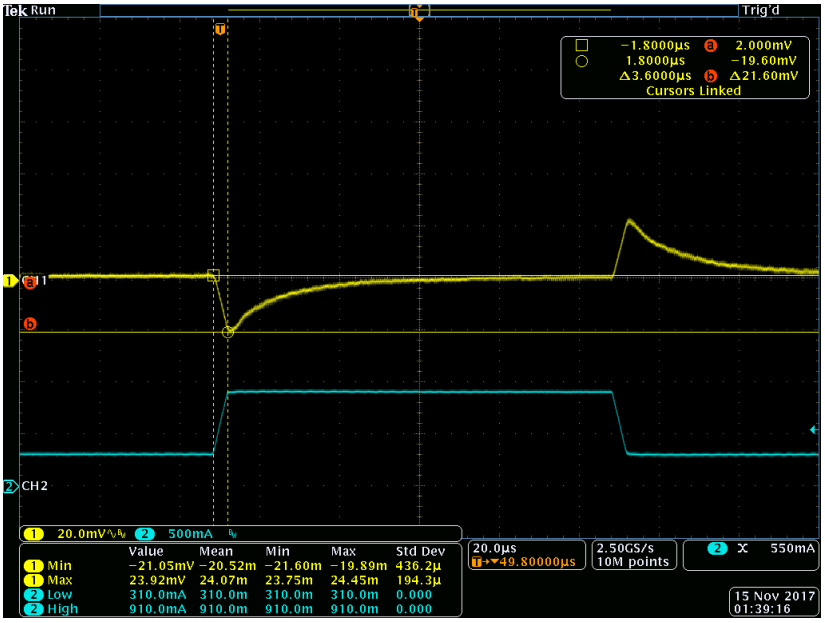

Figure 32: VCCIO (BUCKIO) Transient Response, V_{OUT} = 3.3 V, 0.6 A Step

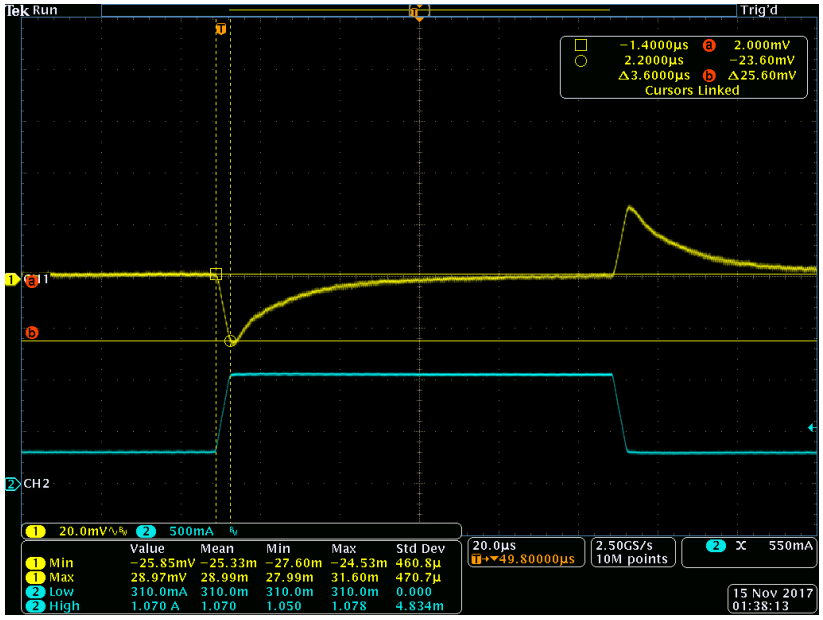

Figure 33: VCCIO (BUCKIO) Transient Response, V_{OUT} = 3.3 V, 0.75 A Step

4.7.5 Reference Measurements

The operating performance of the PMIC is affected by the performance of the voltage references. This section shows the performance of the voltage references over temperature.

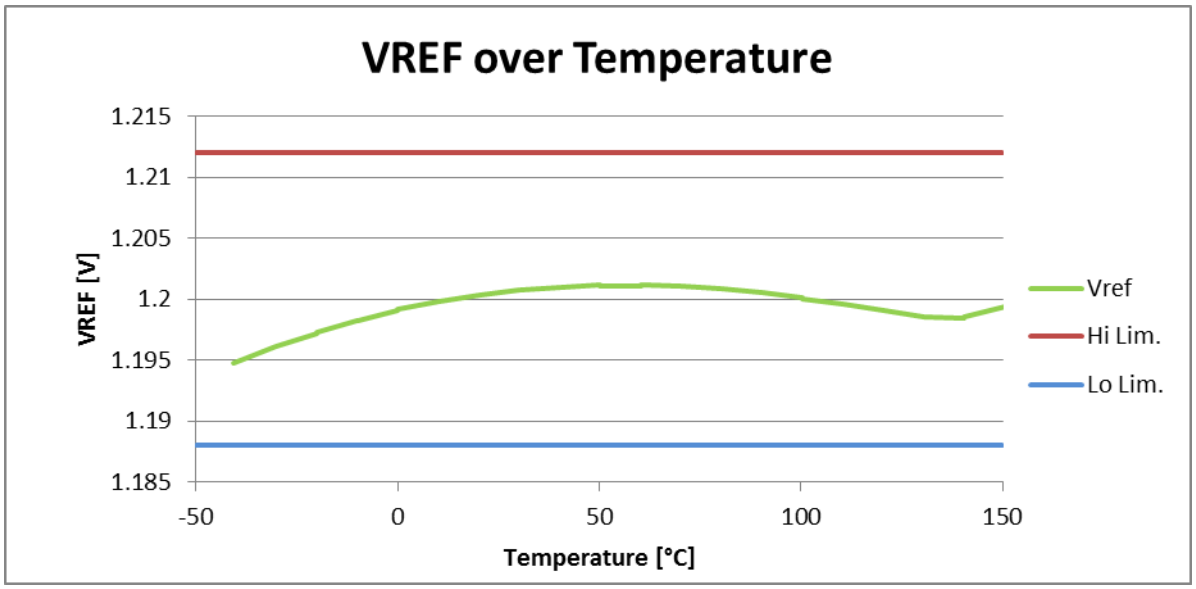

Figure 34: V_{REF} Over Temperature

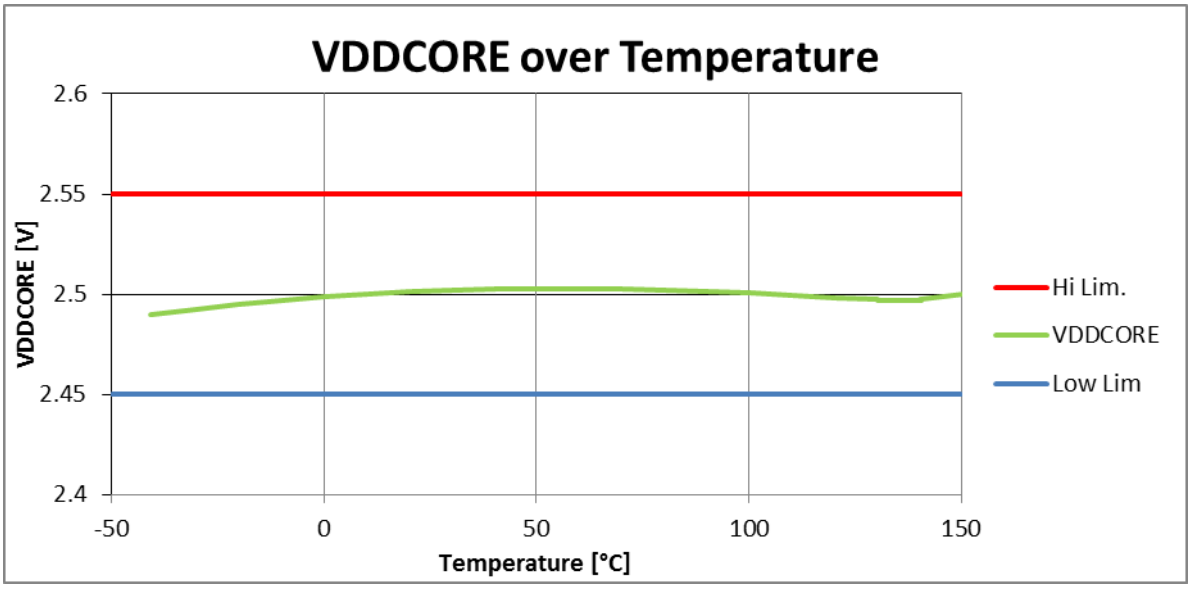

Figure 35: VDDCORE Over Temperature

5 Conclusions

By providing a high level of integration and efficiency in a small PCB footprint, the Dialog DA9063 along with the DA9213 can be seen to be an ideal partner to the Xilinx Ultrascale+ ZU9EG or other members of the Ultrascale+ family of devices.

Revision History

Revision	Date	Description
1.0	17-Nov-2017	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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