Renesas RA Family

System Specifications for Standard Boot Firmware

Introduction

This document describes the specification of standard boot firmware for Renesas RA microcontrollers. This document assumes that the reader has an understanding of specifications for Renesas RA products, FPSYS/FACI, and FCB.

Target Device

This document is for the RA2A1, RA4M1, RA4W1, RA6M1, RA6M2, RA6M3, and RA6T1 MCU Groups. This document will be revised to include other products as needed.

Contents

1. Definition of Terms....3
1.1 Flash Memory....3
1.2 Boot Firmware....3
1.3 SCI: Serial Communication Interface....4
1.4 AW: Access Window....4
2. System Architecture....6
2.1 Renesas RA4M1/RA4W1....6
2.2 Renesas RA2A1....7
2.3 Renesas RA6M1/RA6M2/RA6M3/RA6T1....8
2.4 Mode Entry....9
3. Serial Programming Interface....9
3.1 Communication Mode....9
3.1.1 Two-wire UART Communication....10
3.1.2 USB Communication....10
3.2 Operating Procedures....11
3.2.1 Communication Setting Phase....11
3.2.2 Authentication Phase....13
3.2.3 Command Acceptance Phase....13
3.2.4 State Transitions....14
3.2.5 Beginning Communication....15
3.3 Packet Format....16
3.3.1 Command Packet....17
3.4 Communication Command....17
3.4.1 List of Command Codes....17
3.4.2 List of Status Codes....18
3.4.3 Executable Command in Each Phase....18
3.4.4 Unsupported Command....18
3.4.5 Inquiry Command....19

3.4.6 Erase Command 21
3.4.7 Write Command 23
3.4.8 Read Command 26
3.4.9 ID Authentication Command 28
3.4.10 Baud Rate Setting Command 32
3.4.11 Signature Request Command 35
3.4.12 Area Information Request Command 37
3.5 Recommended Procedure for Flash Programmer 39
3.5.1 Beginning Communication 39
3.5.2 Total Area Erasure 40
3.5.3 Acquisition of Device Information 40
3.5.4 Code and Data in User Area Updates 41
3.5.5 Configuration Data Updates 41

Revision History 43

1. Definition of Terms

The terminology used in this specification is defined in this section.

1.1 Flash Memory

The ROM area where program code is written is called the Code Flash. The ROM area where data is written is called the Data Flash. Both are called Flash Memory. The area used by user is called the User area. The area that stores configuration data is called the Config area.

Example: Figure 1 is an example of flash memory structure. Note that memory structure will differ from device to device.

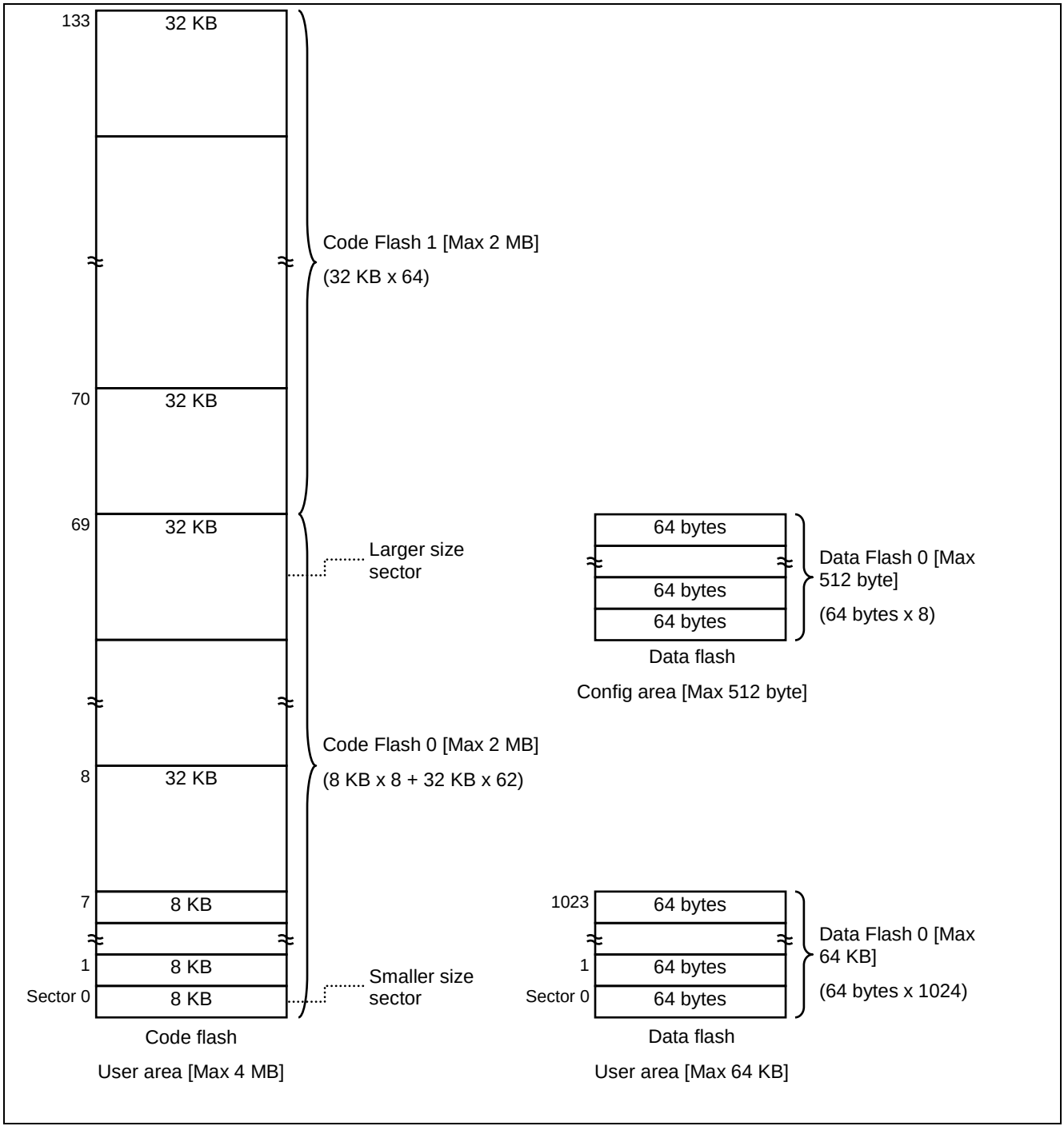


Figure 1. Flash Memory Structure Example

1.2 Boot Firmware

The program included in the microcontroller to rewrite the flash memory is called the Boot Firmware.

1.3 SCI: Serial Communication Interface

The interface module which performs serial communication is called the Serial Communication Interface (SCI). This boot firmware uses the common SCI configured as UART (Universal Asynchronous Receiver/Transmitter).

1.4 AW: Access Window

The function that assigns accessible sectors to erase or write in code flash is called the Access Window (AW). This function allows access from start sector to end sector and disallows access to other areas. Users set a value corresponding to the “start sector” to the FAWS, and set a value corresponding to “end sector + 1” to the FAWE. If FSPR is 0, FAWS and FAWE cannot be changed. For details, please refer to the Renesas RA Flash Memory Programming Application Note.

Table 1. Example of the RA6 Series Flash Memory Structure

Sector No.	Base address	Size	Setting value
0	00000000h	8 KB	000h
1	00002000h	8 KB	001h
2	00004000h	8 KB	002h
3	00006000h	8 KB	003h
4	00008000h	8 KB	004h
5	0000A000h	8 KB	005h
6	0000C000h	8 KB	006h
7	0000E000h	8 KB	007h
8	00010000h	32 KB	008h
9	00018000h	32 KB	00Ch
10	00020000h	32 KB	010h
11	00028000h	32 KB	014h
:	:	:	:
132	003F0000h	32 KB	1F8h
133	003F8000h	3 2KB	1FCh

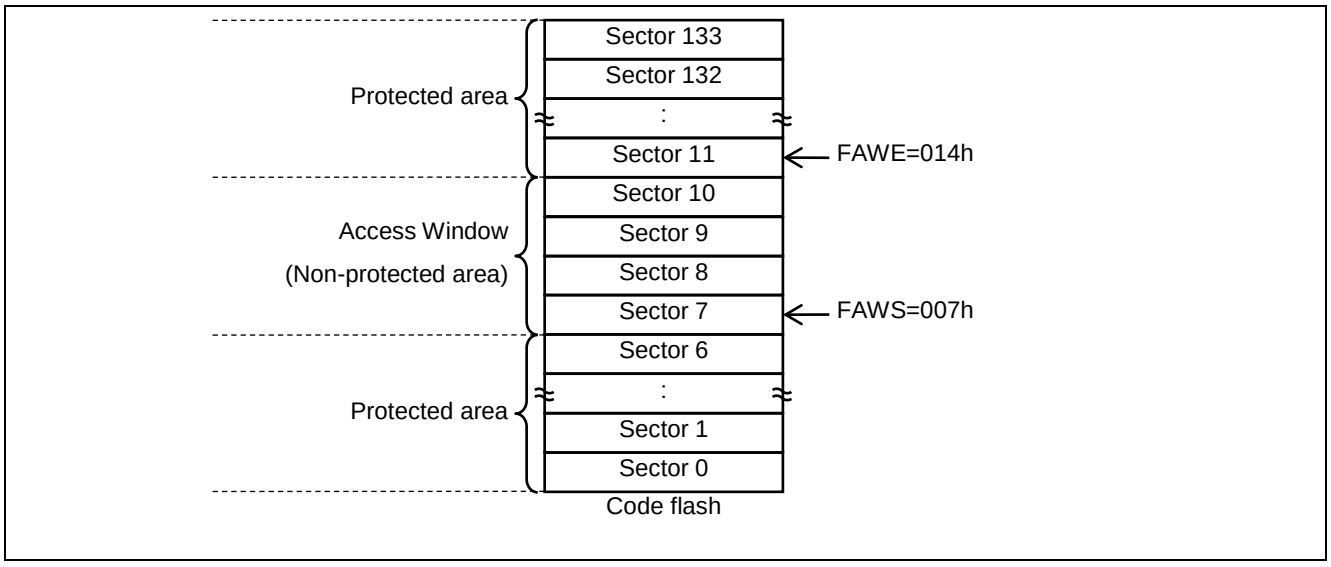


Figure 2. Access Window Example: FAWS = 007h, FAWE = 014h

Table 2. Example of RA4 Series Flash Memory Structure

Sector No.	Base address	Size	Setting value
0	00000000h	2 KB	000h
1	00000800h	2 KB	002h
2	00001000h	2 KB	004h
3	00001800h	2 KB	006h
4	00002000h	2 KB	008h
5	00002800h	2 KB	00Ah
6	00003000h	2 KB	00Ch
7	00003800h	2 KB	00Eh
8	00004000h	2 KB	010h
9	00004800h	2 KB	012h
10	00005000h	2 KB	014h
11	00005800h	2 KB	016h
:	:	:	:
510	000FF000h	2 KB	3FCh
511	000FF800h	2 KB	3FEh

Table 3. Example of RA2 Series Flash Memory Structure

Sector No.	Base address	Size	Setting value
0	00000000h	1 KB	000h
1	00000400h	1 KB	001h
2	00000800h	1 KB	002h
3	00000C00h	1 KB	003h
4	00001000h	1 KB	004h
5	00001400h	1 KB	005h
6	00001800h	1 KB	006h
7	00001C00h	1 KB	007h
8	00002000h	1 KB	008h
9	00002400h	1 KB	009h
10	00002800h	1 KB	00Ah
11	00002C00h	1 KB	00Bh
:	:	:	:
1022	000FF800h	1 KB	3FEh
1023	000FFC00h	1 KB	3FFh

2. System Architecture

Boot firmware has a serial programming interface to send and receive flash control commands between the microcontroller and the flash programmer in serial programming mode. In debug mode, boot firmware only erases all of the User area and Config area. Boot firmware is embedded in the device.

2.1 Renesas RA4M1/RA4W1

Table 4. RA4 Series Serial Programming

Operating mode	When VCC is higher than 2.4 V: High-speed mode When VCC is lower than 2.4 V: Middle-speed mode
Supported communication	Two-wire UART, USB*1
Main-OSC input	When using USB: Necessary*2 When not using USB: Unnecessary
Operating voltage condition	VCC = 1.8 V–5.5 V*3

Notes:*1. For devices that have a UCKSEL register (in other words, devices where HOCO is selectable as USB clock source), boot firmware generates the USB clock from HOCO. Therefore, USB communication is not guaranteed in an environment where the accuracy of HOCO oscillation does not meet the standard of USB clock. For the accuracy of HOCO oscillation, refer to the device's electrical characteristics.

*2. For devices that have a UCKSEL register (in other words, devices where HOCO is selectable as USB clock source), boot firmware can operate by HOCO even when using USB.

*3. USB communication is not available when VCC < 3 V.

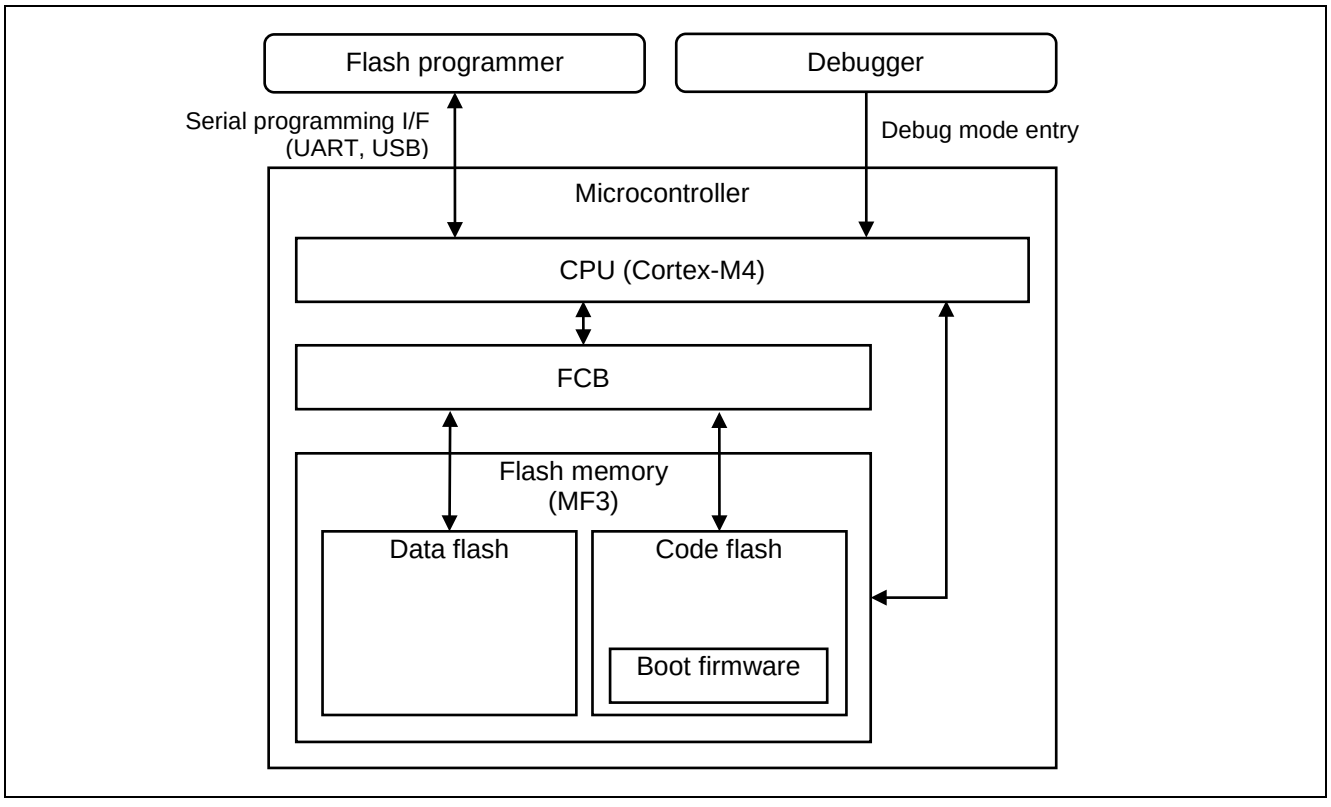


Figure 3. RA4 Series Flash System Architecture

2.2 Renesas RA2A1

Table 5. RA2A1 Serial Programming

Operating mode	When VCC is higher than 2.4 V: High-speed mode When VCC is lower than 2.4 V: Middle-speed mode
Supported communication	Two-wire UART
Main-OSC input	Unnecessary
Operating voltage condition	VCC = 1.8 V–5.5 V

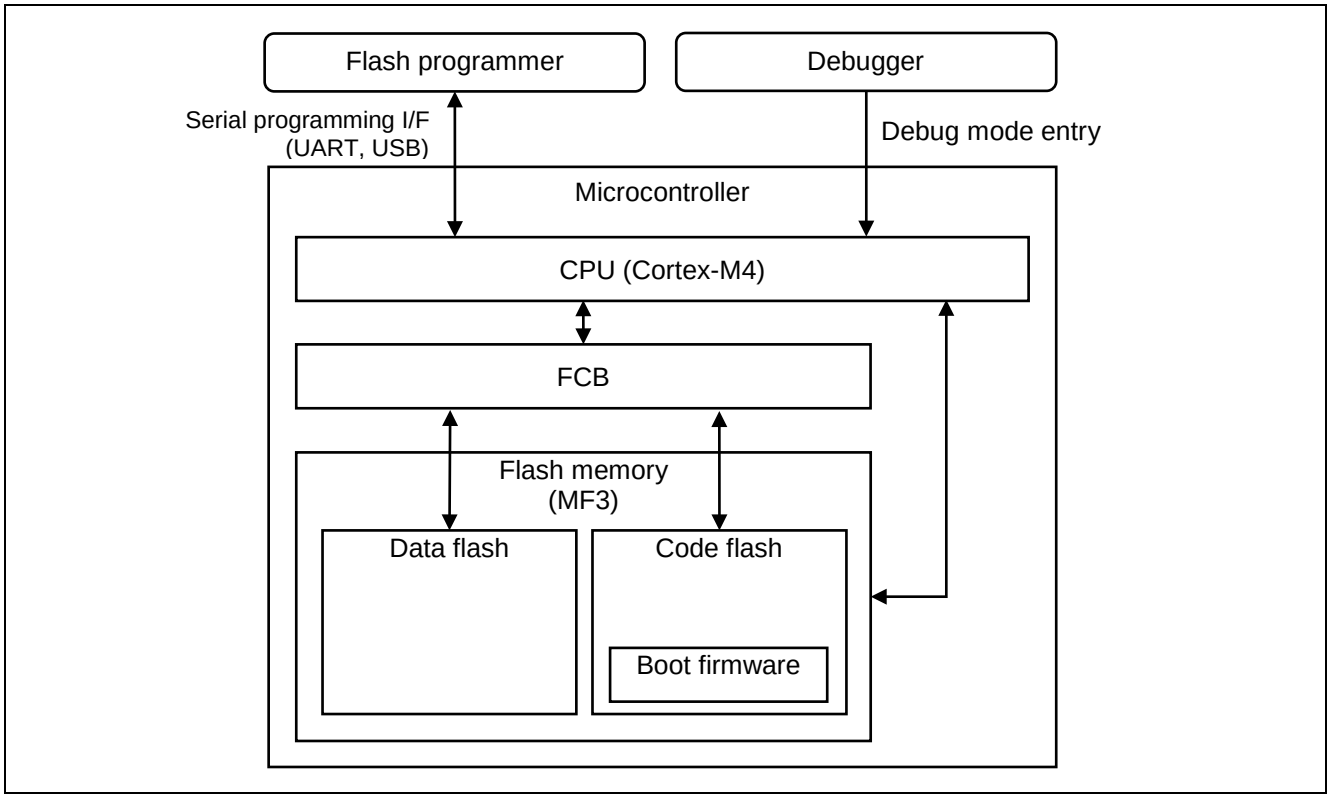


Figure 4. RA2A1 Flash System Architecture

2.3 Renesas RA6M1/RA6M2/RA6M3/RA6T1

Table 6. RA6 Series Serial Programming

Operating mode	High-speed mode
Supported communication	Two-wire UART, USB
Main-OSC input	When using USB: Necessary When not using USB: Unnecessary
Operating voltage condition	VCC = 2.7 V–3.6 V. Same as device specification.*

Note: * USB communication is not available when VCC < 3.

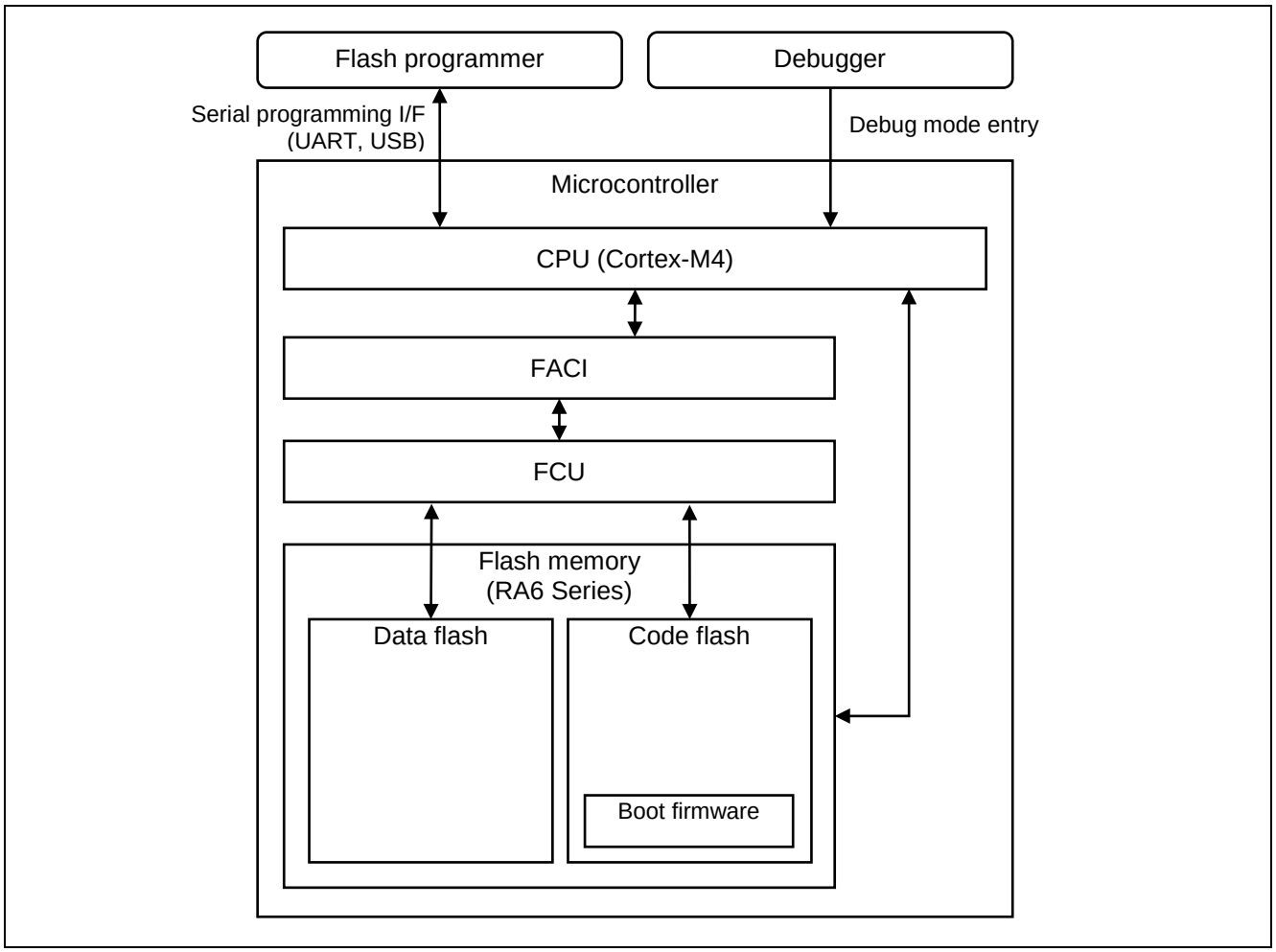


Figure 5. RA6 Series Flash System Architecture

2.4 Mode Entry

Boot firmware selects Serial programming mode or Debug mode based on the MD pin level at reset timing. If the operating mode is Serial programming mode, boot firmware transitions to the Communication setting phase. If the operating mode isn't Serial programming mode, boot firmware erases all of the User area and Config area, and then goes into an infinite loop. If Security MPU is valid, boot firmware goes into an infinite loop without transition to either mode.

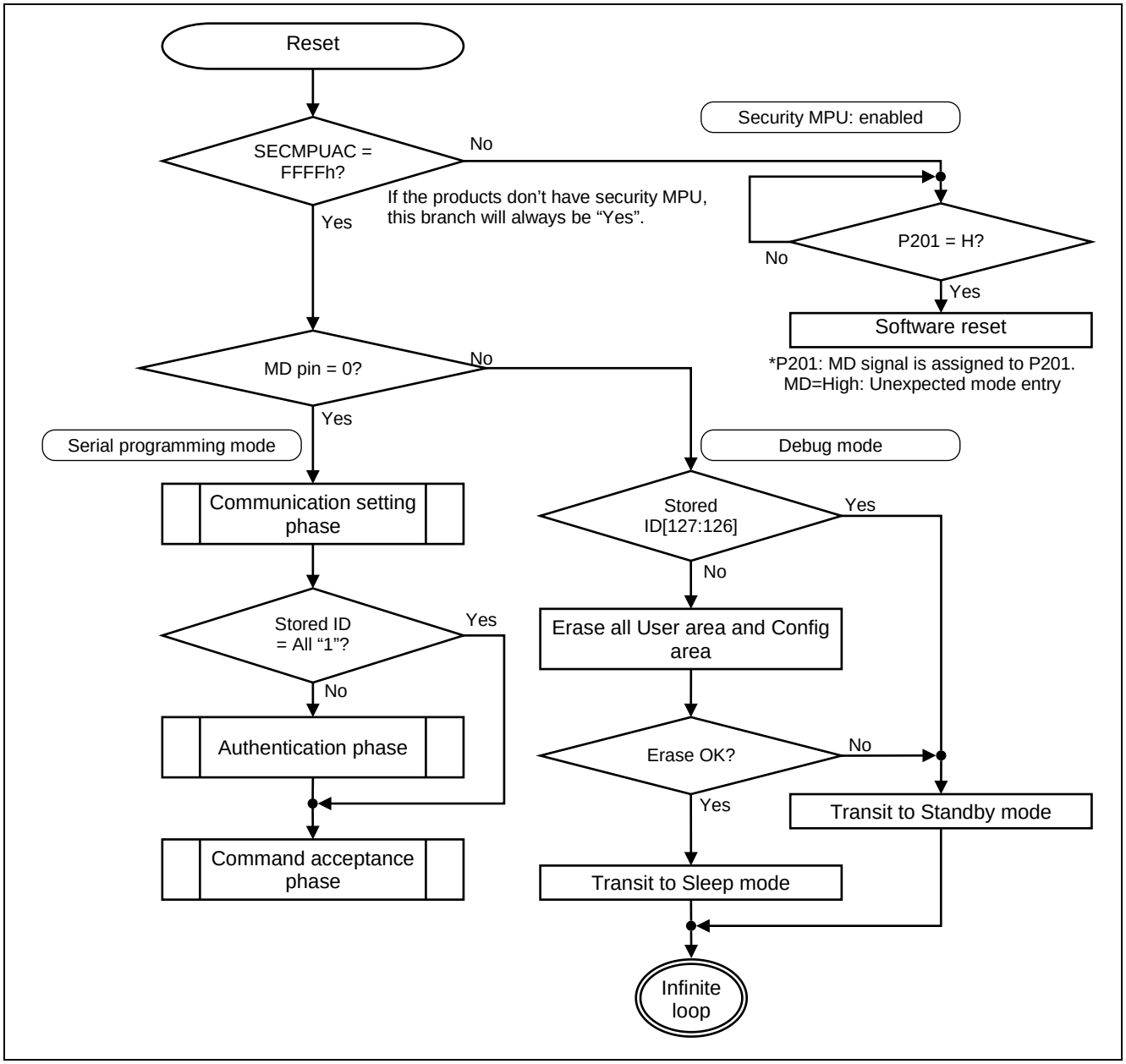


Figure 6. Flash Modes

3. Serial Programming Interface

3.1 Communication Mode

Boot firmware has interfaces for the following communication modes. Section 3.2.1 includes a flowchart for selecting the mode.

- Two-wire UART communication
- USB communication

3.1.1 Two-wire UART Communication

Boot firmware supports two-wire UART communication (Figure 7).

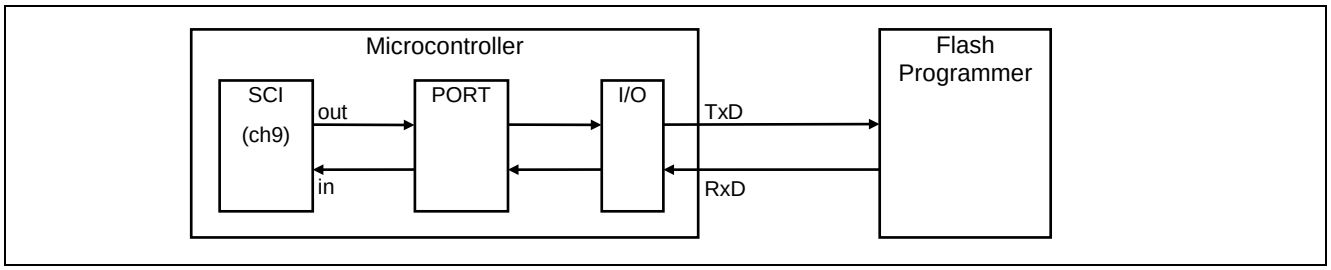


Figure 7. Two-Wire UART Communication

In Serial programming mode, boot firmware sets RxD to port-In for communication mode detection. Boot firmware selects UART communication and initializes the SCI by the detecting the falling edge of RxD.

Table 7. UART Settings

Interface	SCI ch9
RxD	Reception and Transmission mode
TxD	Reception and Transmission mode
Baud rate	9600 bps
Data length	8 bits (LSB first)
Parity bit	None
Stop bit	1 bit

Communication speed is 9600 bps until the baud rate setting command is completed. Communication speed is changed to the intended rate after successful completion of the baud rate setting command (Figure 8).

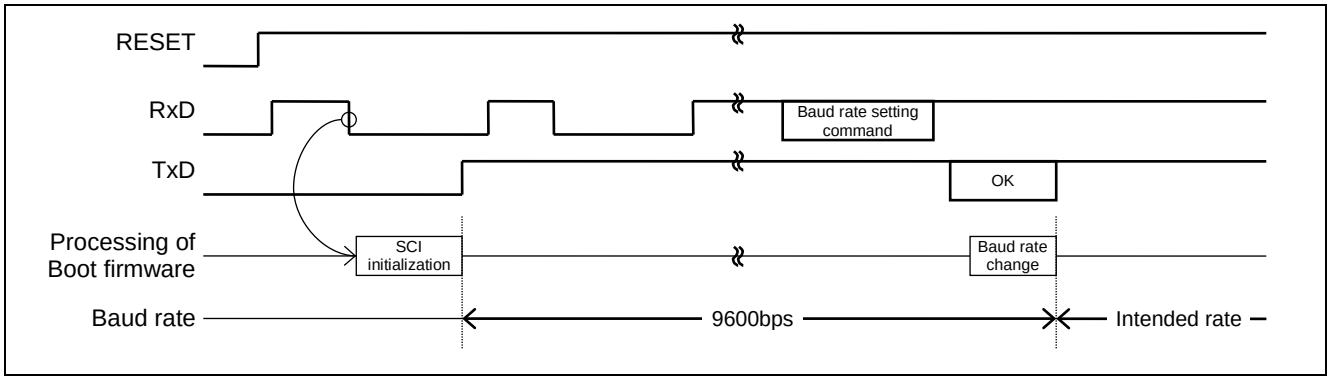


Figure 8. Baud Rate Setting

When using UART communication, do not connect to flash programmer with the USB cable.

If the UART communication cable is unplugged during transmission, the result is undefined.

3.1.2 USB Communication

Boot firmware supports USB communication (Figure 9).

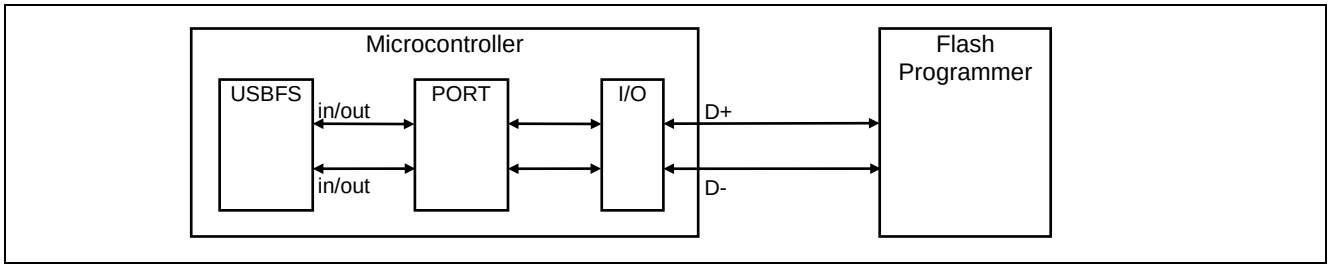


Figure 9. USB Communication

In Serial programming mode, boot firmware sets USB state to enumeration. Boot firmware selects USB communication and initiates communication by the detection of the “Configured” state.

Table 8. USB Settings

Interface	USBFS
VBUS	Input mode
D+	Input-Output mode
D-	Input-Output mode
Transfer rate	12 Mbps (USB2.0 Full Speed)
Device class	Communication device class (CDC) SubClass: Abstract Control Model (ACM) Protocol: Common AT commands
Vendor ID	045Bh (Renesas)
Product ID	0261h (RA USB Boot)
Transfer mode	Control (in/out) Bulk (in, out) Interrupt (in)
End points	**RA4, RA6 series** EP0: Default control pipe, Control transfers (in/out) EP1: TxD pipe, Bulk transfers (in) 64 bytes EP2: RxD pipe, Bulk transfers (out) 64 bytes EP6: Control pipe, Interrupt transfers (in) **RA2A1** EP0: Default control pipe, Control transfers (in/out) EP4: TxD pipe, Bulk transfers (in) 64 bytes EP5: RxD pipe, Bulk transfers (out) 64 bytes EP6: Control pipe, Interrupt transfers (in)

Clock input from the Main clock oscillator with the frequencies listed in Table 9 is necessary to generate the clock for USB communication.

Table 9. Clock Frequencies for USB Communication

Series	Frequency
RA6	8, 10, 12, 15, 16, 20, or 24 MHz
RA4/2 w/o UCKSEL register	4, 6, 8 or 12 MHz
RA4/2 w/ UCKSEL register	N/A (Clock for USB is generated from HOCO, not Main oscillator)

When using USB communication, release the reset after connecting to the flash programmer with the USB cable.

If the USB cable is unplugged during transmission, the result is undefined.

When using USB communication, boot firmware notifies host that the power mode is self-powered.

3.2 Operating Procedures

3.2.1 Communication Setting Phase

After reset release, boot firmware selects the communication mode (two-wire UART or USB) by the flowchart in Figure 10. After communication setting and the receipt of Generic code via the selected communication method, boot firmware transitions to the Authentication phase. However, if the ID code stored in the device is all “1”, boot firmware transitions to the Command acceptance phase directly.

3.2.1.1 Selection of Communication Mode

Table 10. Communication Mode Selection

Condition	Communication mode
Detection of High level on MD (P201): Single chip mode	Unexpected mode entry (-> Software reset)
Detection of “Configured” state (Enumeration is completed)	USB mode
Detection of a falling edge on RxD	UART mode

* P201: MD signal is assigned to P201.

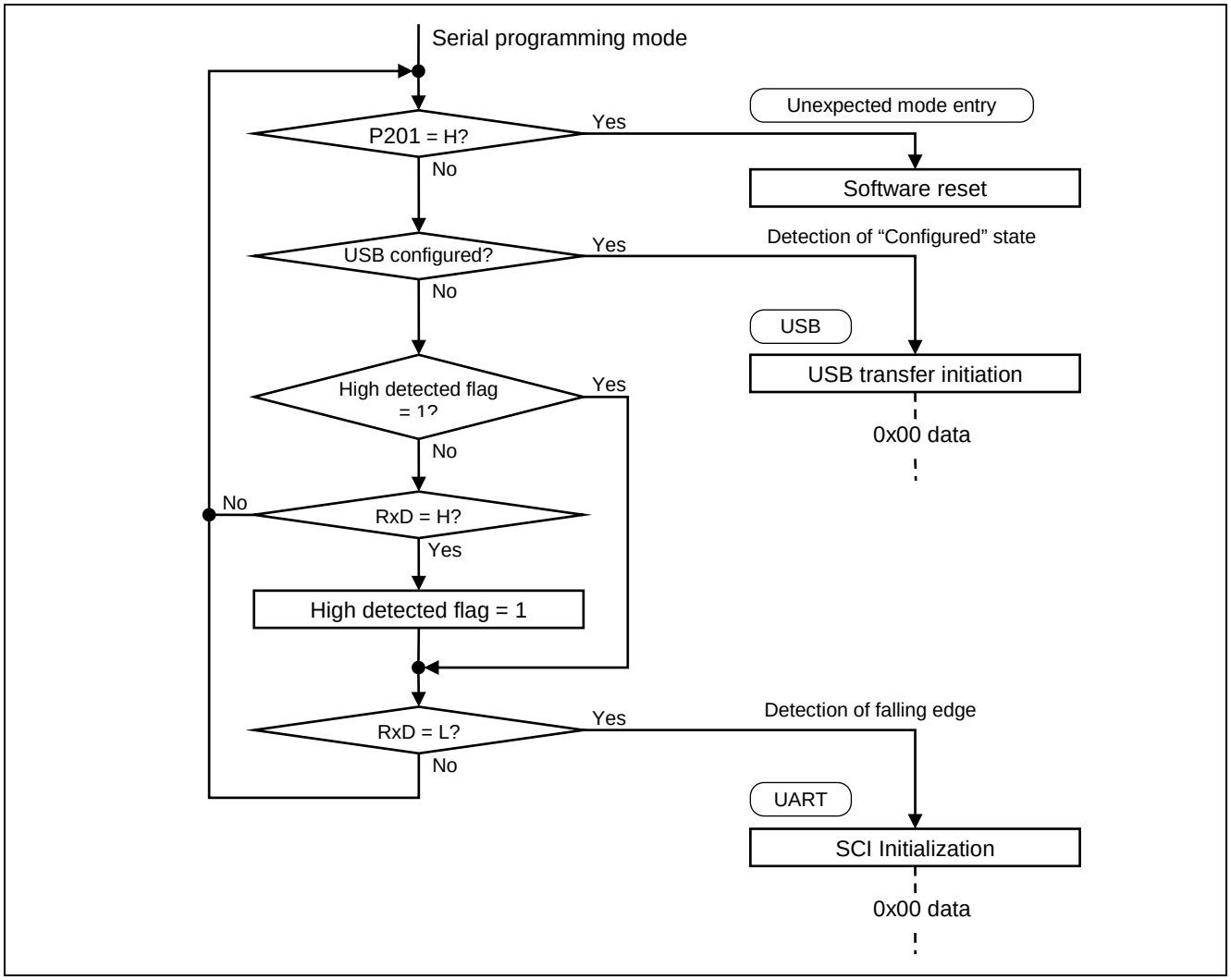


Figure 10. Selecting Communication Mode

3.2.1.2 Setting Up Two-wire UART Communication

To use UART communication, the flash programmer sends 0x00 data (low pulse) at 9600 bps at least two times. (If the environment is noisy, retry sending the low pulse until ACK is received.) Boot firmware selects UART communication and initializes the SCI when it detects the falling edge on RxD. After that, boot firmware receives the second low pulse as 0x00 data in SCI, then returns the ACK, receives the Generic code, then returns the Boot code. This completes communication setting.

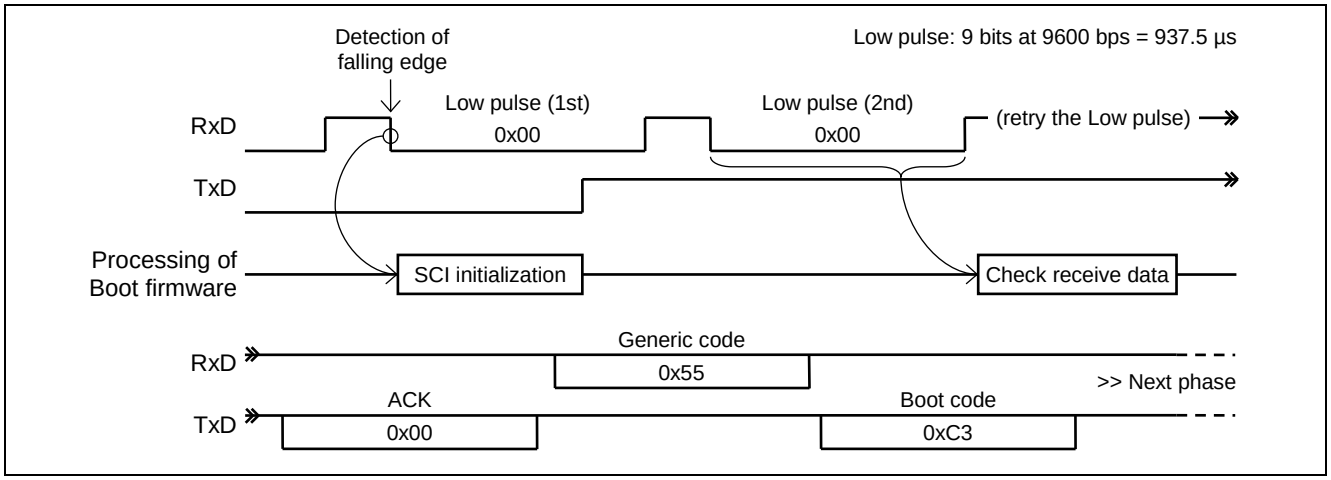


Figure 11. Two-Wire UART Set Up

3.2.1.3 Setting Up USB Communication

Boot firmware selects USB communication when it detects the Configured state. After that, boot firmware receives 0x00 data from the RxD pipe, then returns the ACK, receives the Generic code, then returns the Boot code. This completes communication settings.

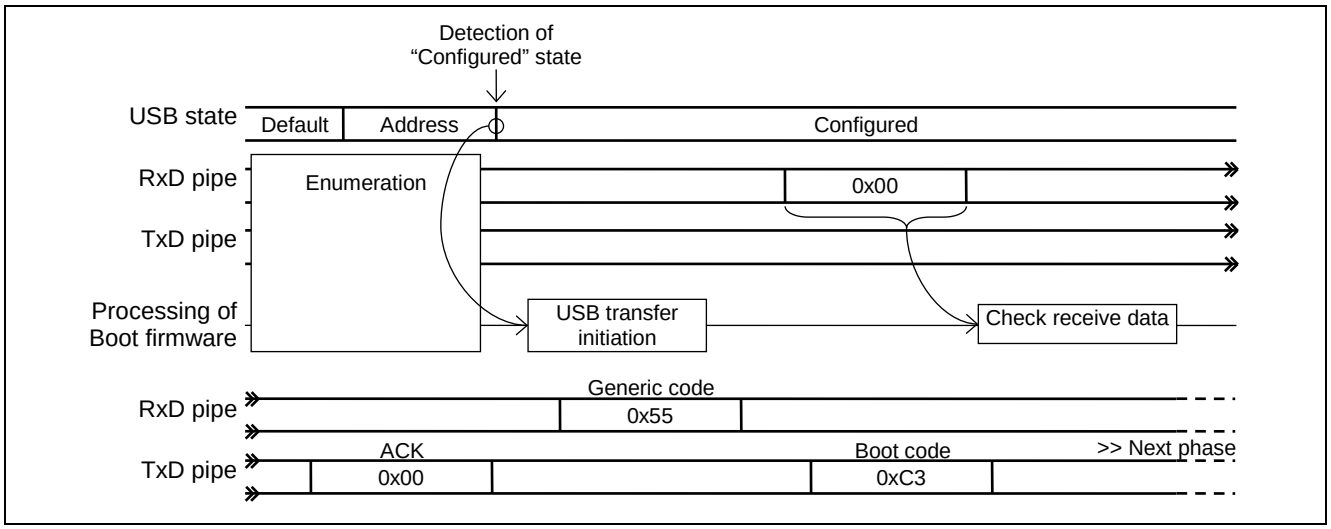


Figure 12. USB Communication Set Up

3.2.2 Authentication Phase

Boot firmware authenticates ID code in this phase. This phase can accept only the Authentication command. If the Authentication command passes successfully, boot firmware transitions to Command acceptance phase.

3.2.3 Command Acceptance Phase

This phase can accept all commands except the Authentication command. The flash programmer can judge if the current phase is Command acceptance phase or Authentication phase by the result of an Inquiry command.

3.2.4 State Transitions

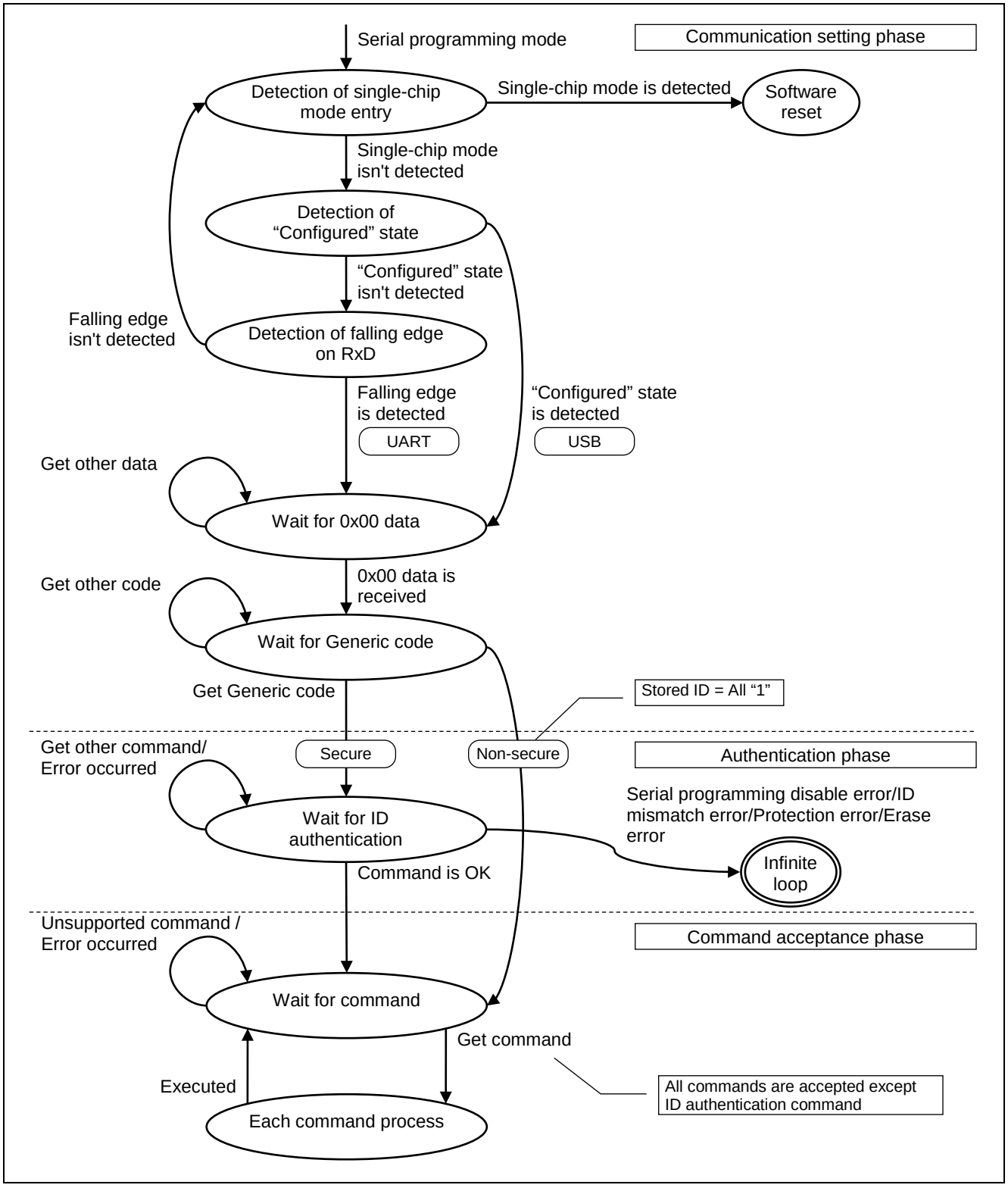


Figure 13. State Transitions

3.2.5 Beginning Communication

3.2.5.1 If ID Code is Already Stored [Secure]

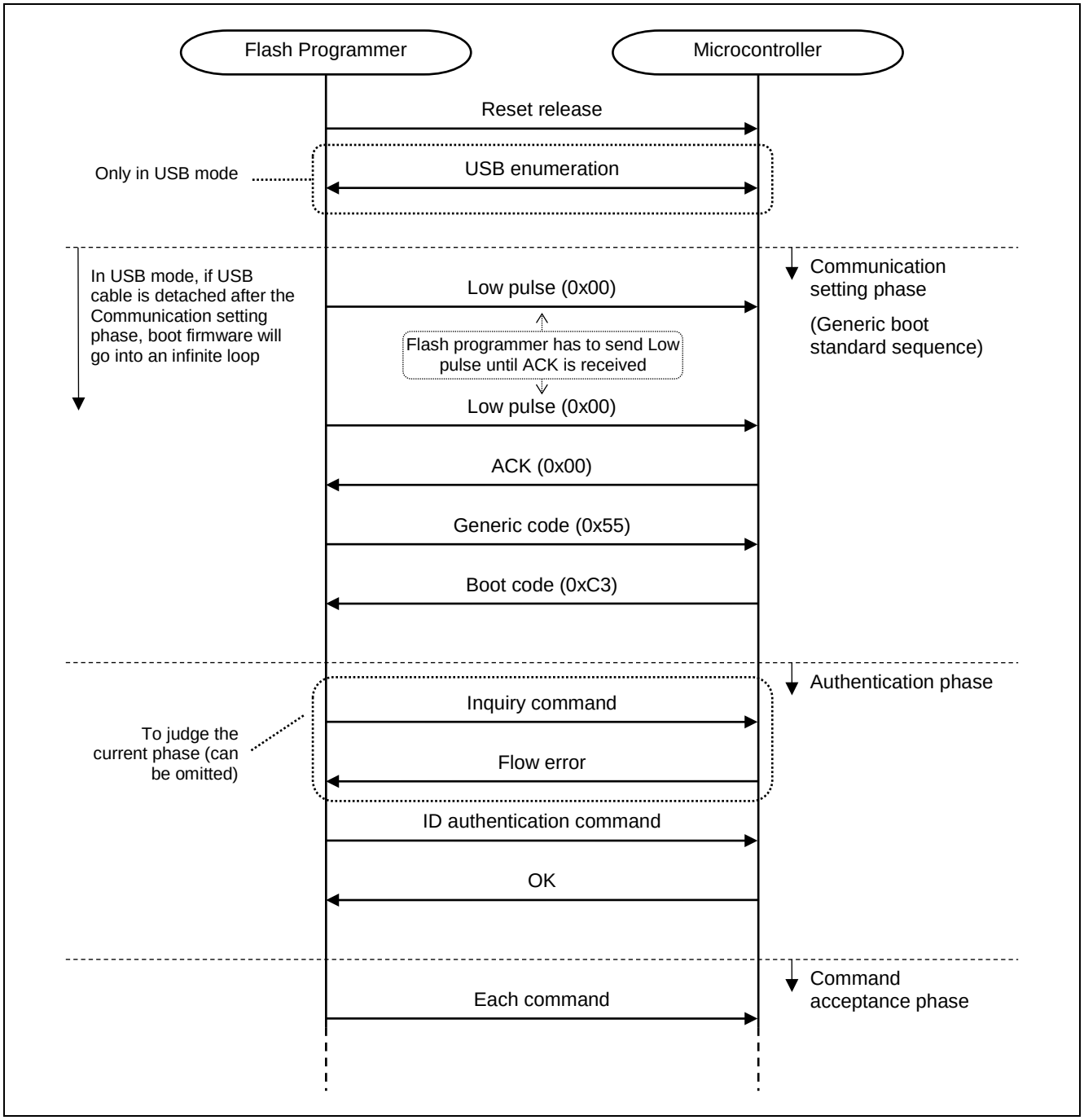


Figure 14. Beginning Communication (Secure)

3.2.5.2 If ID Code Is Not Stored [Non-Secure]

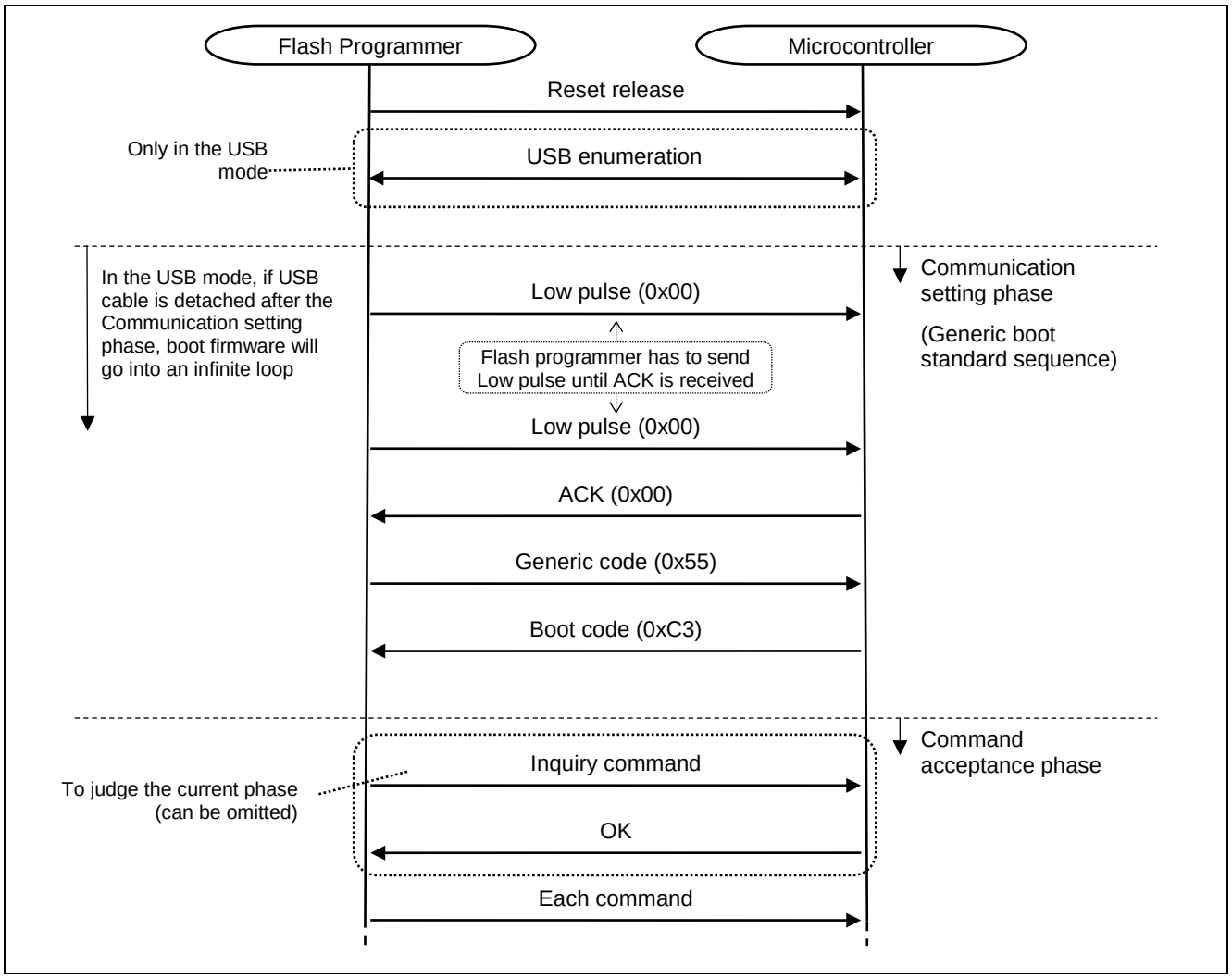


Figure 15. Beginning Communications (Non-secure)

3.3 Packet Format

Be sure to follow this format. If the boot firmware receives a packet of more than 1024 bytes, the boot firmware may not be able to reply.

3.3.1 Command Packet

The flash programmer sends data of a command packet to the microcontroller in the following format.

SOH	LNH	LNL	COM	Command information (flexible length [max:255 bytes])	SUM	ETX

Symbol	Size	Code	Description
SOH	1 byte	0x01	Start of command packet
LNH	1 byte	-	Packet length (Length = COM + Command information) [High]
LNL	1 byte	-	Packet length (Length = COM + Command information) [Low]
COM	1 byte	-	Command code (refer to section 3.4.1)
Command information	-	-	Command information [Max: 255 bytes] Example: For write command: Write destination address For erase command: Erase target address
SUM	1 byte	-	Sum data of LNH + LNL + COM + Command information (expressed as two's complement) Example: LNH + LNL + COM + Command information(1) + Command information(2) + ... + Command information(n) + SUM = 0x00
ETX	1 byte	0x03	End of packet

Note: If the packet length is 0 or over 1024, the value of RES will not be defined.

3.4 Communication Command

3.4.1 List of Command Codes

Table 11. Command Codes

Command code	Command name	Description
0x00	Inquiry command	Return ACK (to determine the current phase)
0x12	Erase command	Erase data on target area
0x13	Write command	Write data on target area
0x15	Read command	Read data on target area
0x30	ID authentication command	Authenticate ID for connection with the device
0x34	Baud rate setting command	Set baud rate for UART
0x3A	Signature request command	Get signature information
0x3B	Area information request command	Get area information

3.4.2 List of Status Codes

Table 12. Status Codes

Status code	Description
0x00 | Command code	OK (ongoing normally): used in Response code [RES]
0x80 | Command code	ERR (occurrence of an error): used in Response code [RES]
0x00	OK (successful completion)
0xC0	Unsupported command error
0xC1	Packet error (Illegal length, Missing ETX, and so forth)
0xC2	Checksum error
0xC3	Flow error
0xD0	Address error
0xD4	Baud rate margin error
0xDA	Protection error
0xDB	ID mismatch error
0xDC	Serial programming disable error
0xE1	Erase error (*1)
0xE2	Write error (*1)
0xE7	Sequencer error (*1)

Note: *1 For Erase command or Write command, boot firmware checks the status registers of the flash sequencer (FACI or FCB) and returns the following status.

Status	Flash process	Condition
Erase error	RA2/RA4 Series	If ERERR is detected
	RA6 Series	If ERSERR is detected
Write error	RA2/RA4 Series	If PRGERR or PRGERR01 are detected
	RA6 Series	If PRGERR is detected
Sequencer error	RA2/RA4 Series	If ILGLERR or EILGLERR are detected
	RA6 Series	If ILGLERR or FLWEERR are detected

3.4.3 Executable Command in Each Phase

Table 13. Executable Commands

Command	Communication setting phase	Authentication phase	Command acceptance phase
Inquiry command	NG (*1)	Flow error	OK
Erase command	NG (*1)	Flow error	OK
Write command	NG (*1)	Flow error	OK
Read command	NG (*1)	Flow error	OK
ID authentication command	NG (*1)	OK	Flow error
Baud rate setting command	NG (*1)	Flow error	OK
Signature request command	NG (*1)	Flow error	OK
Area information request command	NG (*1)	Flow error	OK

Note: *1 Boot firmware does not return any data packet.

3.4.4 Unsupported Command

If boot firmware receives the command packet of a command code that is not defined in section 3.4.1, it returns the unsupported command error, then goes back to the Wait for command state.

3.4.4.1 Command Processing Procedure

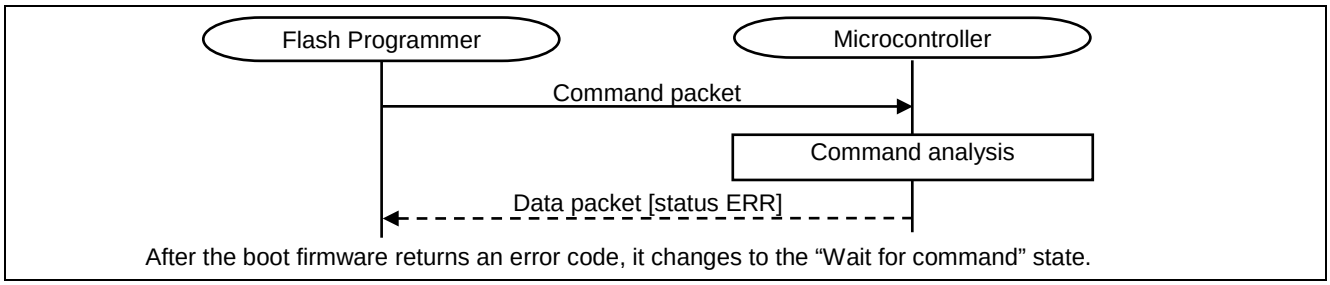


Figure 16. Unsupported Command Processing

3.4.4.2 Command Packet

SOH	LNH	LNL	COM	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	Length high
LNL	(1 byte)	Length low
COM	(1 byte)	Command code not defined in section 3.4.1
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.4.3 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x80 | COM (ERR)
STS	(1 byte)	Status code 0xC0 (Unsupported command error) 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.4.4 Status Code from Microcontroller [Priority high: 1 -> low: 10]

Table 14. Unsupported Command Status Codes

Condition	Status	Priority	Code
If COM in the received packet is undefined code	Unsupported command error	4	0xC0
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2

3.4.5 Inquiry Command

The Inquiry command is used to check if boot firmware is in Command acceptance phase or not. This command can be performed only in Command acceptance phase.

3.4.5.1 Command Processing Procedure

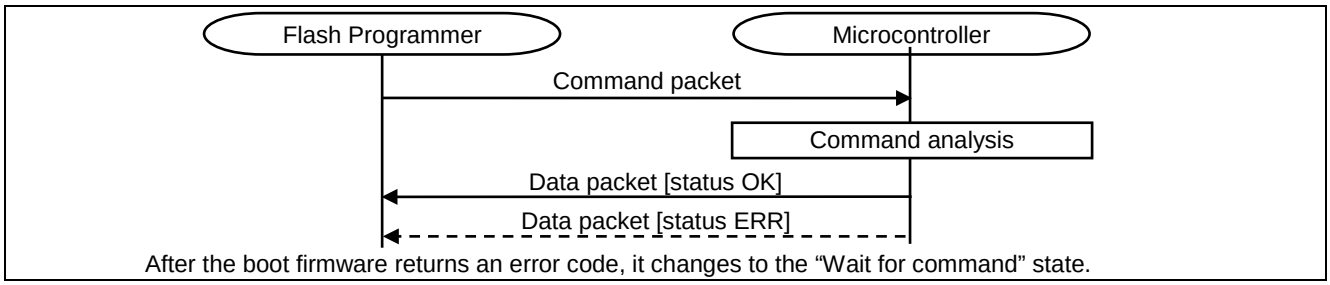


Figure 17. Inquiry Command Processing

3.4.5.2 Command Packet

SOH	LNH	LNL	COM	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x01
COM	(1 byte)	0x00 (Inquiry command)
SUM	(1 byte)	0xFF
ETX	(1 byte)	0x03

3.4.5.3 Data Packet [Status OK]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x00 (OK)
STS	(1 byte)	Status code 0x00 (OK)
SUM	(1 byte)	0xFE
ETX	(1 byte)	0x03

3.4.5.4 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x80 (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.5.5 Status Code from Microcontroller [Priority High: 1 -> low: 10]

Table 15. Inquiry Status Codes

Condition	Status	Priority	Code
If the state is Command acceptance phase	OK	5	0x00
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3

3.4.6 Erase Command

The Erase command erases data in the designated area of the flash memory. The alignment of the target addresses follows the area information returned by the Area information request command. Erasures are executed in order from the start address to the end address by the erase access unit. This command can be performed only in Command acceptance phase.

3.4.6.1 Command Processing Procedure

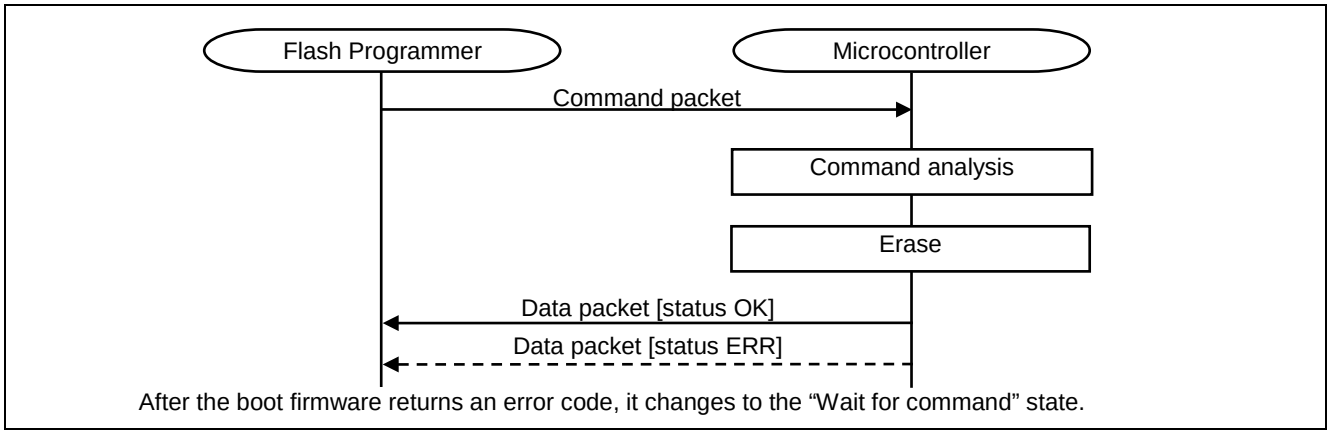


Figure 18. Erase Command Processing

3.4.6.2 Command Packet

SOH	LNH	LNL	COM	SAD	EAD	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x09
COM	(1 byte)	0x12 (Erase command)
SAD	(4 bytes)	Start address Example: 0000_4000h -> 0x00, 0x00, 0x40, 0x00
EAD	(4 bytes)	End address Example: 003F_FFFFh -> 0x00, 0x3F, 0xFF, 0xFF
SUM	(1 bytes)	Sum data
ETX	(1 bytes)	0x03

3.4.6.3 Data Packet [Status OK]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x12 (OK)
STS	(1 byte)	Status code 0x00 (OK)
SUM	(1 byte)	0xEC
ETX	(1 byte)	0x03

3.4.6.4 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x92 (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error) 0xD0 (Address error) 0xDA (Protection error) 0xE1 (Erase error) 0xE2 (Write error) 0xE7 (Sequencer error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.6.5 Status Code from Microcontroller [Priority High: 1 -> Low: 10]

Table 16. Erase Status Codes

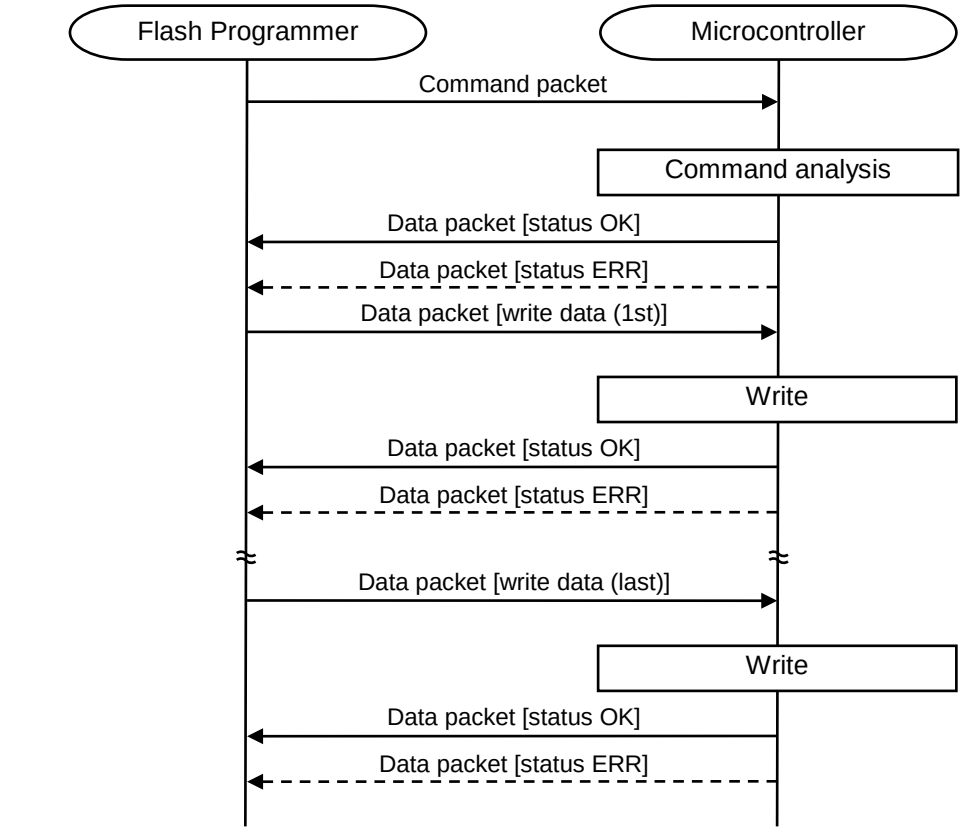
Condition	Status	Priority	Code
Successful completion	OK	8	0x00
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3
If the start address or the end address does not belong to any areas *1	Address error	5	0xD0
The start address is in a different area from the end address *1		5	
This command isn't available for this area		5	
The start address is bigger than the end address		5	
If the start address or the end address does not match the alignment of the area		5	
If the target area is not entirely within the Access Window in the case of User area in code flash	Protection error	6	0xDA
If the target area is Config area, and the FSPR bit is 0		6	
If the erase error occurs	Erase error	7	0xE1
If the write error occurs	Write error	7	0xE2
If the sequencer error occurs	Sequencer error	7	0xE7

Note: *1 Scope of each area is subject to area information request command

3.4.7 Write Command

The Write command receives write data from the flash programme, and writes those data to the flash memory. The alignment of the target address follows the area information returned by the Area information request command. Writes are executed in order from start address to end address by the write access unit. This command can be performed only in the Command acceptance phase.

3.4.7.1 Command Processing Procedure



After the boot firmware returns an error code, it changes to the “Wait for command” state.

Figure 19. Write Command Processing

3.4.7.2 Command Packet

SOH	LNH	LNL	COM	SAD	EAD	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x09
COM	(1 byte)	0x13 (Write command)
SAD	(4 bytes)	Start address Example: 0000_4000h -> 0x00, 0x00, 0x40, 0x00
EAD	(4 bytes)	End address Example: 003F_FFFFh -> 0x00, 0x3F, 0xFF, 0xFF
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.7.3 Data Packet [Write Data]

SOD	LNH	LNL	RES	DAT	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	N + 1 (High)
LNL	(1 byte)	N + 1 (Low)
RES	(1 byte)	0x13 (OK)
DAT	(N bytes)	Write data
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

Note: N = 1–1024

3.4.7.4 Data Packet [Status OK]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x13 (OK)
STS	(1 byte)	Status code 0x00 (OK)
SUM	(1 byte)	0xEB
ETX	(1 byte)	0x03

3.4.7.5 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x93 (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error) 0xD0 (Address error) 0xDA (Protection error) 0xE1 (Erase error) 0xE2 (Write error) 0xE7 (Sequencer error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.7.6 Status Code from Microcontroller [Priority High: 1 -> low: 10]

Table 17. Write Status Codes

Condition	Status	Priority	Code
Successful completion	OK	9	0x00
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If the number of data of all data packets received from flash programmer is beyond the number of write data designated by the command packet		7	
If the write length does not match the write access unit of the area		7	
If the RES of received data packet isn't OK		7	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3
If the start address or the end address does not belong to any areas *1	Address error	5	0xD0
If the start address is in a different area from the end address *1		5	
If this command isn't available for this area		5	
If the start address is bigger than the end address		5	
If the start address or the end address does not match to the alignment of the area		5	
If the target area is not entirely within the Access Window in the case of User area in code flash	Protection error	6	0xDA
If the target area contain FAWS or FAWE or BTFLG in Config area, and the FSPR bit is 0		6	
If the erase error occurs	Erase error	8	0xE1
If the write error occurs	Write error	8	0xE2
If the sequencer error occurs	Sequencer error	8	0xE7

Note: *1 Scope of each area is subject to area information request command

3.4.7.7 Basic Precautions for Write Command

If you write any value except 0xFFFF to SECMPUAC, boot firmware will hang after the next reset release (refer to section 2.4).

If you write 0 to ID[127] in Config area, the device will lose the ability to perform ID authentication (ID authentication command will return the serial programming disable error) (refer to section 3.4.9).

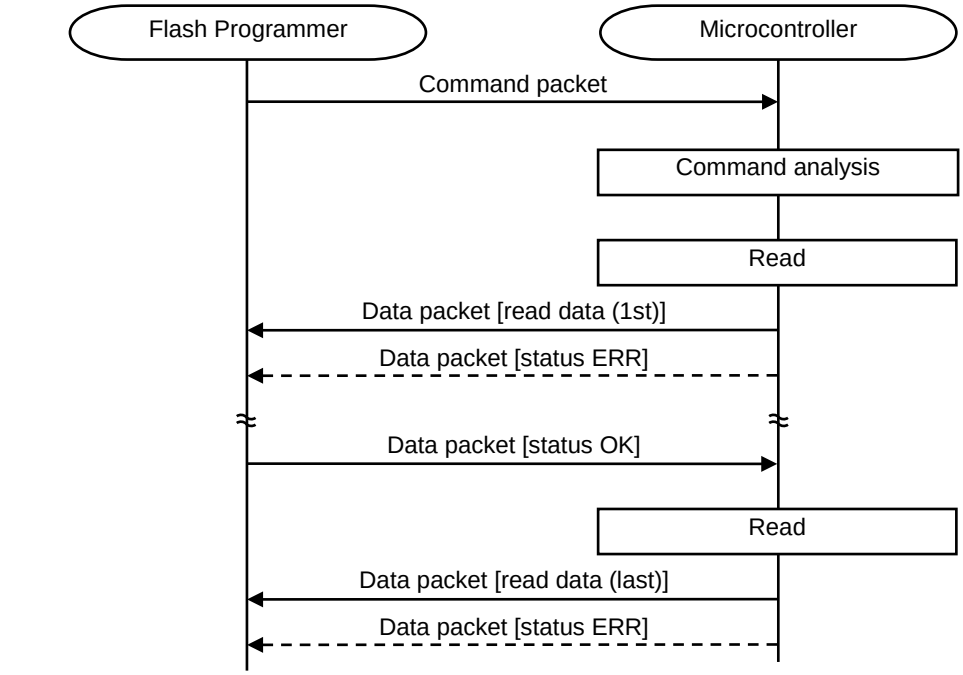
If you write 0 to ID[126] in Config area, the device will lose the ability of total area erasure by ID authentication command (refer to section 3.4.9).

In addition, device configuration data may be assigned in the Option-Setting Memory area and Config area. The result of writing to an unassigned address depends on each device. Therefore, these areas should be rewritten only after careful review of device documents.

3.4.8 Read Command

The Read command reads data from a designated area in the flash memory and sends that data to the flash programmer. The target address can be designated by 1-byte units. Reads are executed in order from start address to end address by 1 byte. This command can be performed only in Command acceptance phase.

3.4.8.1 Command Processing Procedure



After the boot firmware returns an error code, it changes to the “Wait for command” state.

Figure 20. Read Command Processing

3.4.8.2 Command Packet

SOH	LNH	LNL	COM	SAD	EAD	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x09
COM	(1 byte)	0x15 (Read command)
SAD	(4 bytes)	Start address Example: 0000_4000h -> 0x00, 0x00, 0x40, 0x00
EAD	(4 bytes)	End address Example: 003F_FFFFh -> 0x00, 0x3F, 0xFF, 0xFF
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.8.3 Data Packet [Read Data]

SOD	LNH	LNL	RES	DAT	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	N + 1 (High)
LNL	(1 byte)	N + 1 (Low)
RES	(1 byte)	0x15 (OK)
DAT	(N bytes)	Read data
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

Note: N = 1-1024

3.4.8.4 Data Packet [Status OK]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x15 (OK)
STS	(1 byte)	Status code 0x00 (OK)
SUM	(1 byte)	0xE9
ETX	(1 byte)	0x03

3.4.8.5 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x95 (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error) 0xD0 (Address error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.8.6 Status Code from Microcontroller [Priority High: 1 -> low: 10]

Table 18. Read Status Codes

Condition	Status	Priority	Code
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If the RES of received data packet isn't OK		6	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3
If the start address or the end address does not belong to any areas *1	Address error	5	0xD0
If the start address is a different kind of area from the end address *1		5	
If the start address is bigger than the end address		5	

Note: *1. Scope of each area is subject to area information request command.

3.4.9 ID Authentication Command

The ID authentication command compares the ID code stored in the device with the ID code received from the flash programmer. The result is sent to the flash programmer. This command can be performed only in Authentication phase.

Table 19. ID Authentication

Condition		Result
Stored ID[127] = 0		Go into an infinite loop
Stored ID[127:126] = 10b		Compare the received ID and the stored ID
Stored ID[127:126] = 11b	Received ID != ALeRASE	Compare the received ID and the stored ID
	Received ID = ALeRASE	Erase all User area and Config area [Total area erasure] -> Transition to Command acceptance phase
Compare	Received ID != stored ID	Go into an infinite loop
	Received ID = stored ID	Transition to Command acceptance phase

Note: * ALeRASE: 0x41, 0x4C, 0x65, 0x52, 0x41, 0x53, 0x45, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF.

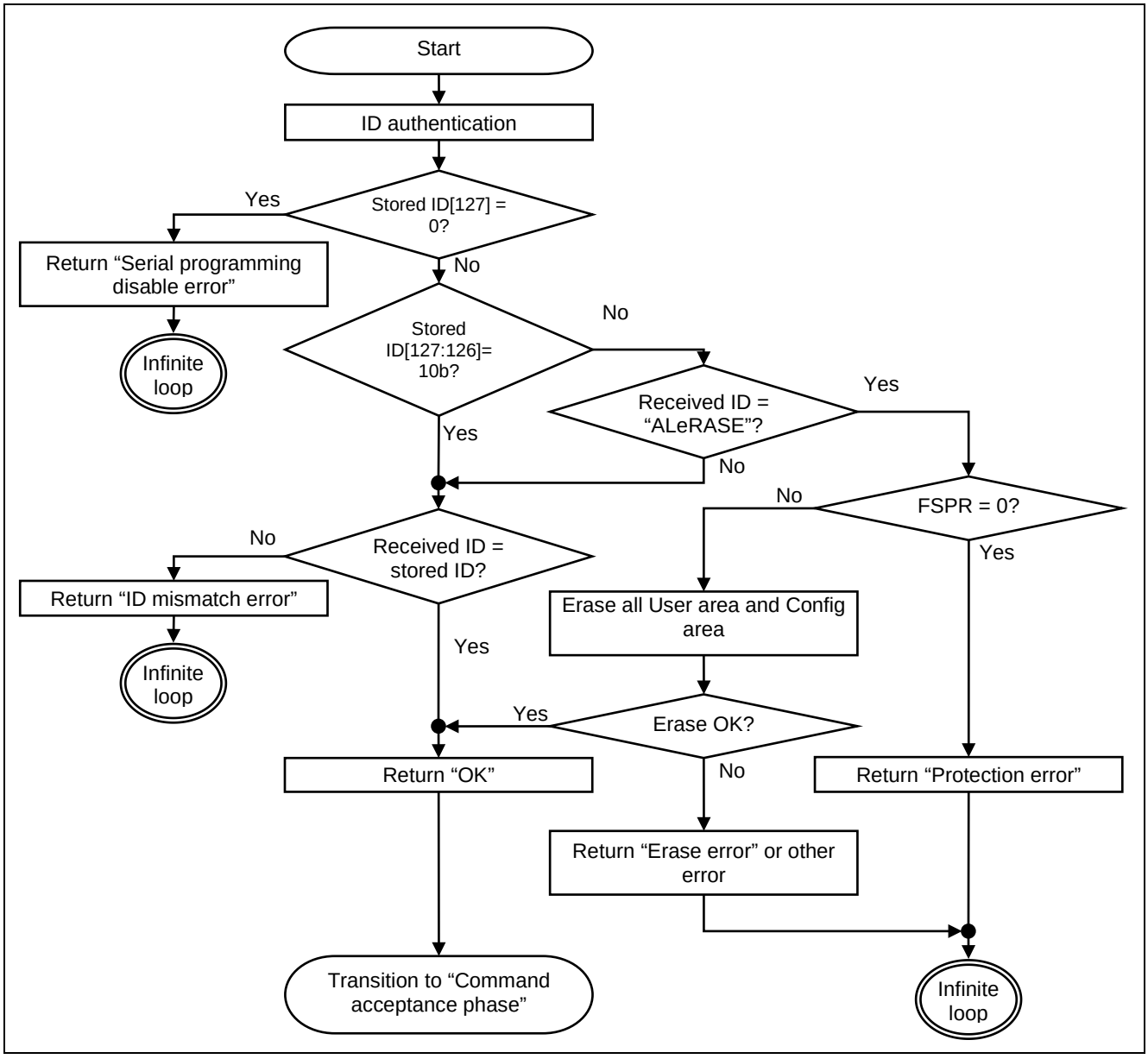
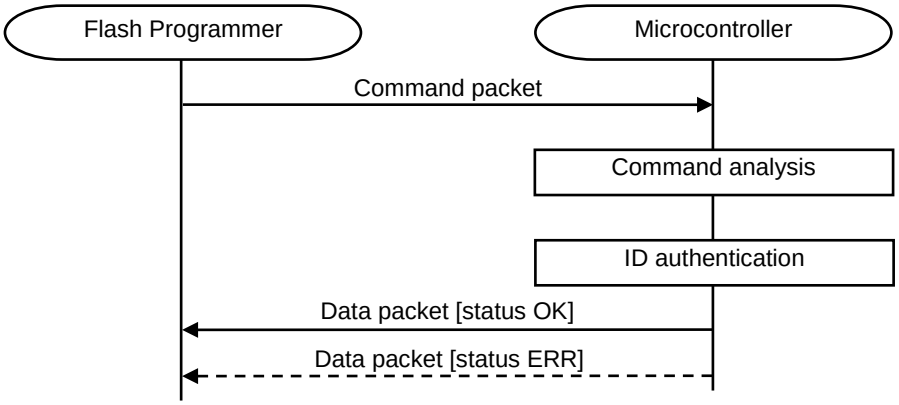


Figure 21. ID Authentication

3.4.9.1 Command Processing Procedure



After the boot firmware returns Packet error or Checksum error or Flow error, it changes to the “Wait ID authentication command” state.

Figure 22. ID Authentication Command Processing

3.4.9.2 Command Packet

SOH	LNH	LNL	COM	Authentication phase	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x11
COM	(1 byte)	0x30 (ID authentication command)
IDC	(16 byte)	ID code
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

Example: when stored ID = “0xF0F1F2F3_E4E5E6E7_D8D9DADB_CCCDCECF”,

Flash programmer sends IDC in order of “0xF0”, “0xF1”, “0xF2”, “0xF3”, “0xE4”, “0xE5”, “0xE6”, “0xE7”, “0xD8”, “0xD9”, “0xDA”, “0xDB”, “0xCC”, “0xCD”, “0xCE”, “0xCF”.

Stored ID:

ID[127:96]				ID[95:64]				ID[63:32]				ID[31:0]			
F0	F1	F2	F3	E4	E5	E6	E7	D8	D9	DA	DB	CC	CD	CE	CF

Order of sending IDC for ID authentication:

1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th
F0	F1	F2	F3	E4	E5	E6	E7	D8	D9	DA	DB	CC	CD	CE	CF

Example: for Total area erasure:

Flash programmer sends IDC in order of “0x41”, “0x4C”, “0x65”, “0x52”, “0x41”, “0x53”, “0x45”, “0xFF”, “0xFF”, “0xFF”, “0xFF”, “0xFF”, “0xFF”, “0xFF”, “0xFF”, “0xFF”.

Order of sending IDC for Total area erasure:

1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th
41	4C	65	52	41	53	45	FF	FF	FF	FF	FF	FF	FF	FF	FF

3.4.9.3 Data Packet [Status OK]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x30 (OK)
STS	(1 byte)	Status code 0x00 (OK)
SUM	(1 byte)	0xCE
ETX	(1 byte)	0x03

3.4.9.4 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0xB0 (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error) 0xDA (Protection error) 0xDB (ID mismatch error) 0xDC (Serial programming disable error) 0xE1 (Erase error) 0xE2 (Write error) 0xE7 (Sequencer error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.9.5 Status Code from Microcontroller [Priority High: 1 -> Low: 10]

Table 20. ID Authentication Status Codes

Condition	Status	Priority	Code
For ALeRASE, if erasure of all User area and Config area is done	OK	8	0x00
If the received ID matches the stored ID	OK	10	0x00
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Command acceptance phase	Flow error	4	0xC3
For ALeRASE, if the FSPR bit is 0	Protection error	6	0xDA
If the received ID is different from the stored ID	ID mismatch error	9	0xDB
If the highest-order bit of stored ID is “0”	Serial programming disable error	5	0xDC
For ALeRASE, if an erase error occurs	Erase error	7	0xE1
For ALeRASE, if a write error occur	Write error	7	0xE2
For ALeRASE, if a sequencer error occurs.	Sequencer error	7	0xE7

3.4.10 Baud Rate Setting Command

The Baud rate setting command receives baud rate data and changes the UART baud rate of the device. If an error occurs, the baud rate is not changed. This command can be performed only in Command acceptance phase. This command does not change the communication speed of USB communication.

3.4.10.1 Command Processing Procedure

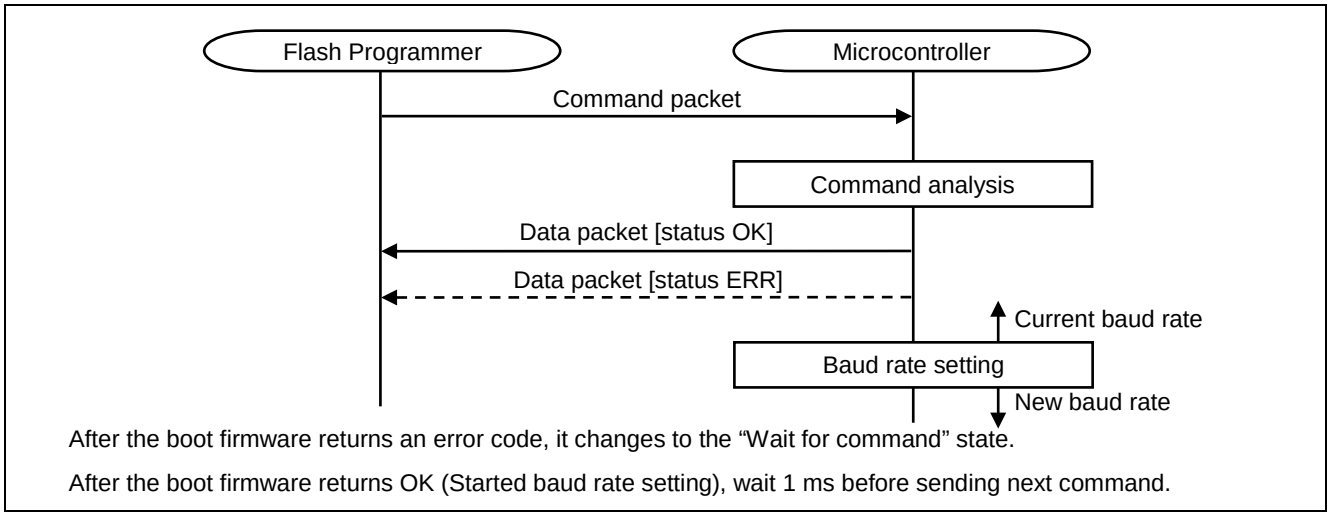


Figure 23. Baud Rate Setting Command Processing

3.4.10.2 Command Packet

SOH	LNH	LNL	COM	BRT	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x05
COM	(1 byte)	0x34 (Baud rate setting command)
BRT	(4 bytes)	UART baud rate [bps] Example: 2 Mbps (2000000 bps) -> 0x00, 0x1E, 0x84, 0x80
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.10.3 Data Packet [Status OK]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0x34 (OK)
STS	(1 byte)	Status code 0x00 (OK)
SUM	(1 byte)	0xCA
ETX	(1 byte)	0x03

3.4.10.4 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0xB4 (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error) 0xD4 (Baud rate margin error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.10.5 Status Code from Microcontroller [Priority High: 1 -> low: 10]

Table 21. Baud Rate Setting Status Codes

Condition	Status	Priority	Code
Started the baud rate setting	OK	6	0x00
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3
If the baud rate error exceeds acceptable range (4%)	Baud rate margin error	5	0xD4
If the BRT value is 0			
If the BRT value exceeds the RMB value			

3.4.10.6 Baud Rate Setting Values

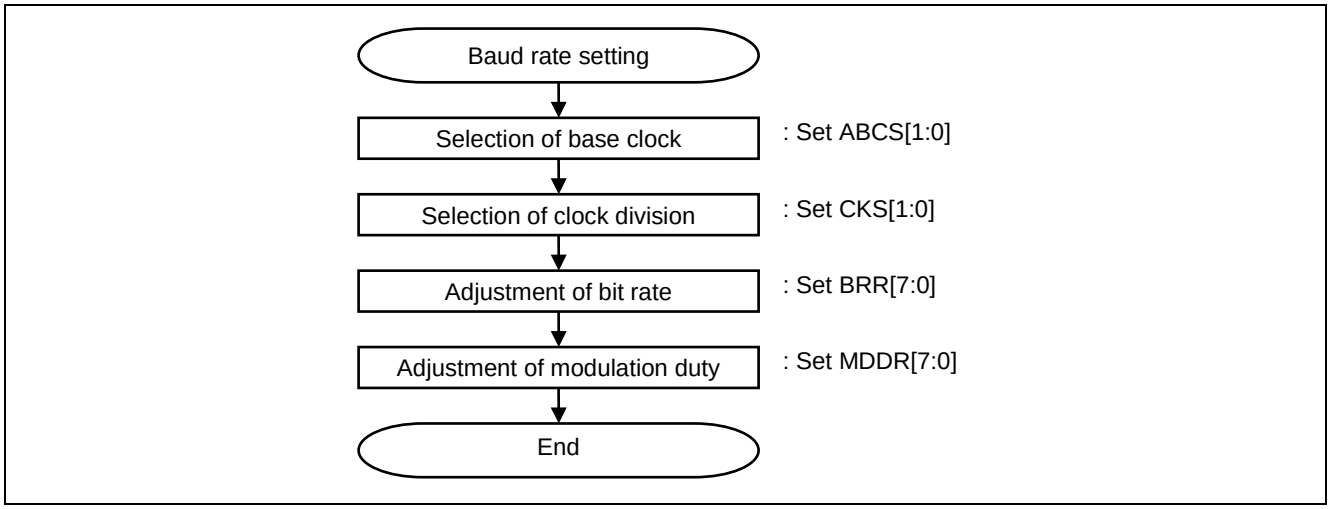


Figure 24. Baud Rate Setting Values

Table 22. Baud Rate Setting

Process	Condition	Setting value
Selection of base clock (ABCS setting)	In case of (SCI / BRT) < 32	ABCS = 1
	Otherwise	ABCS = 0
Selection of clock division (CKS setting)	-	CKS[1:0] = 00b
Adjustment of bit rate (BRR setting)	In case of (SCI / BRT) < 32	BRR[7:0] = 00h
	Otherwise	BRR[7:0] = (SCI / BRT) / 32 - 1
	* If BRR is overflow	BRR[7:0] = FFh
Adjustment of modulation duty (MDDR setting)	In case of (SCI / BRT) < 32	Baud rate = (SCI / (BRR+1)) / 16 MDDR[7:0] = 256 * BRT / baud rate
	Otherwise	Baud rate = (SCI / (BRR+1)) / 32 MDDR[7:0] = 256 * BRT / baud rate
	* If MDDR is overflow	MDDR[7:0] = (non-use) * disable the adjustment by MDDR
	* If MDDR < 128	MDDR[7:0] = 80h

Note: SCI: SCI operating clock frequency [Hz]
BRT: Intended baud rate [bps]

Example: Table 23 and Table 24 show typical settings for baud rate.

Table 23. Baud Rate Settings for Renesas RA6 Series [when SCI = 60 MHz]

Intended baud rate	ABCS	CKS[1:0]	BRR[7:0]	MDDR[7:0]	Accuracy
9600	0	00b	C2h	FFh	-0.3%
1000000	0	00b	00h	88h	-0.4%
1500000	0	00b	00h	CCh	-0.4%
2000000	1	00b	00h	88h	-0.4%
3000000	1	00b	00h	CCh	-0.4%
3500000	1	00b	00h	EEh	-0.4%
3750000	1	00b	00h	(Not used)	0.0%

Table 24. Baud Rate Settings for Renesas RA4 Series [when SCI = 24 MHz]

Intended baud rate	ABCS	CKS[1:0]	BRR[7:0]	MDDR[7:0]	Accuracy
9600	0	00b	4Dh	FFh	-0.3%
1000000	1	00b	00h	AAh	-0.4%
1500000	1	00b	00h	(Not used)	0.0%
2000000	disable	disable	disable	disable	-

3.4.11 Signature Request Command

The Signature request command sends information about the device signature to the flash programmer. This command can be performed in Command acceptance phase.

3.4.11.1 Command Processing Procedure

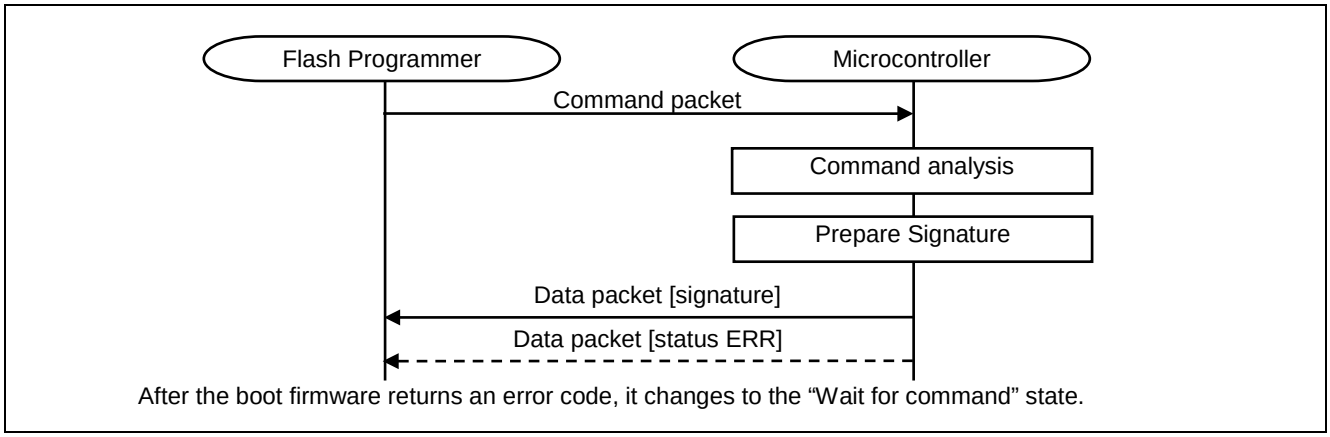


Figure 25. Signature Request Command Processing

3.4.11.2 Command Packet

SOH	LNH	LNL	COM	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x01
COM	(1 byte)	0x3A (Signature request command)
SUM	(1 byte)	0xC5
ETX	(1 byte)	0x03

3.4.11.3 Data Packet [Signature]

SOD	LNH	LNL	RES	SCI	RMB	NOA	TYP	BFV	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x0D
RES	(1 byte)	0x3A (OK)
SCI	(4 bytes)	SCI operating clock frequency [Hz] Example: 20 MHz (20000000 Hz) -> 0x01, 0x31, 0x2D, 0x00
RMB	(4 bytes)	Recommended maximum UART baud rate of the device [bps] Example: 2 Mbps (2000000 bps) -> 0x00, 0x1E, 0x84, 0x80
NOA	(1 byte)	Number of recordable areas Example: If device has following areas 0. User area in Code flash (1st) 1. User area in Code flash (2nd) 2. User area in Data flash 3. Config area -> 0x04
TYP	(1 byte)	Type code 0x02 (RA MCU + RA2/RA4 Series) 0x03 (RA MCU + RA6 Series)
BFV	(2 byte)	Boot firmware version Example: Ver10.8 -> 0x0A, 0x08
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.11.4 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0xBA (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.11.5 Status Code from Microcontroller [Priority High: 1 -> low: 10]

Table 25. Signature Request Status Codes

Condition	Status	Priority	Code
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3

3.4.12 Area Information Request Command

The Area information request command sends information about the designated area to the flash programmer. The alignment of the target address of Erase command and Write command will follow this area information. This command can be performed only in Command acceptance phase.

3.4.12.1 Command Processing Procedure

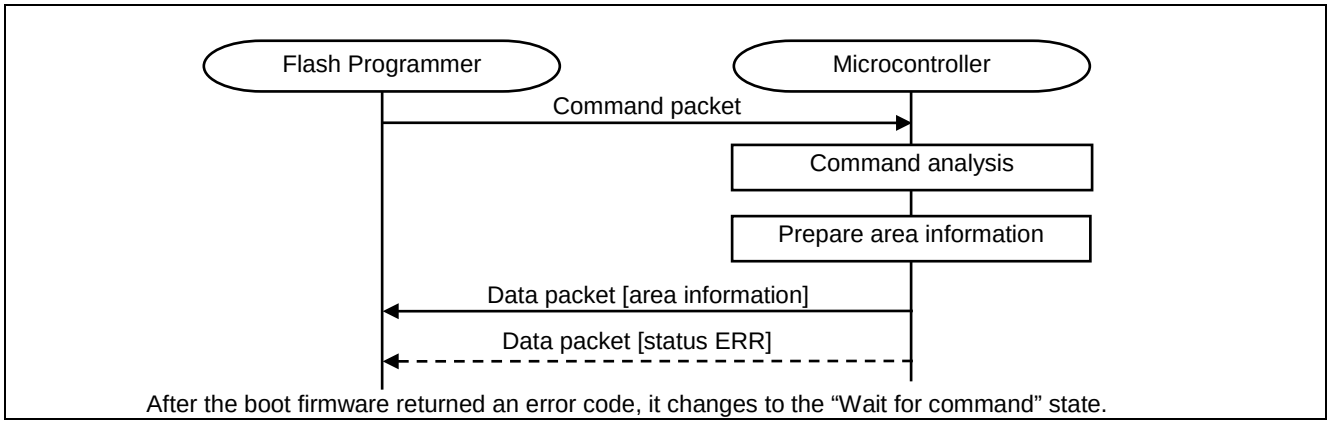


Figure 26. Area Information Request Command Processing

3.4.12.2 Command Packet

SOH	LNH	LNL	COM	NUM	SUM	ETX

SOH	(1 byte)	0x01
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
COM	(1 byte)	0x3B (Area information request command)
NUM	(1 byte)	Area number [0–NOA-1]
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.12.3 Data Packet [Area information]

SOD	LNH	LNL	RES	KOA	SAD	EAD	EAU	WAU	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x12
RES	(1 byte)	0x3B (OK)
KOA	(1 byte)	Kind of area 0x00 (User area in Code flash) 0x01 (User area in Data flash) 0x02 (Config area)
SAD	(4 bytes)	Start address Example: 0001_0000h -> 0x00, 0x01, 0x00, 0x00
EAD	(4 bytes)	End address Example: 001F_FFFFh -> 0x00, 0x1F, 0xFF, 0xFF
EAU	(4 bytes) *1	Erase access unit (alignment) [bytes] Example: 32 KB (32768 bytes) -> 0x00, 0x00, 0x80, 0x00
WAU	(4 bytes)	Write access unit (alignment) [byte] Example: 256 bytes -> 0x00, 0x00, 0x01, 0x00
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

Note: *1 If EAU is 0x00000000, Erase command is not available for the area.

3.4.12.4 Data Packet [Status ERR]

SOD	LNH	LNL	RES	STS	SUM	ETX

SOD	(1 byte)	0x81
LNH	(1 byte)	0x00
LNL	(1 byte)	0x02
RES	(1 byte)	0xBB (ERR)
STS	(1 byte)	Status code 0xC1 (Packet error) 0xC2 (Checksum error) 0xC3 (Flow error) 0xD0 (Address error)
SUM	(1 byte)	Sum data
ETX	(1 byte)	0x03

3.4.12.5 Status Code from Microcontroller [Priority High: 1 -> low: 10]

Table 26. Area Information Request Status Codes

Condition	Status	Priority	Code
If LNH and LNL in the received packet are different from defined values	Packet error	3	0xC1
If the received packet does not have ETX		1	
If SUM in the received packet is different from the value calculated by the boot firmware	Checksum error	2	0xC2
If the state is Authentication phase	Flow error	4	0xC3
If NUM in the received packet is a nonexistent area number	Address error	5	0xD0

3.5 Recommended Procedure for Flash Programmer

3.5.1 Beginning Communication

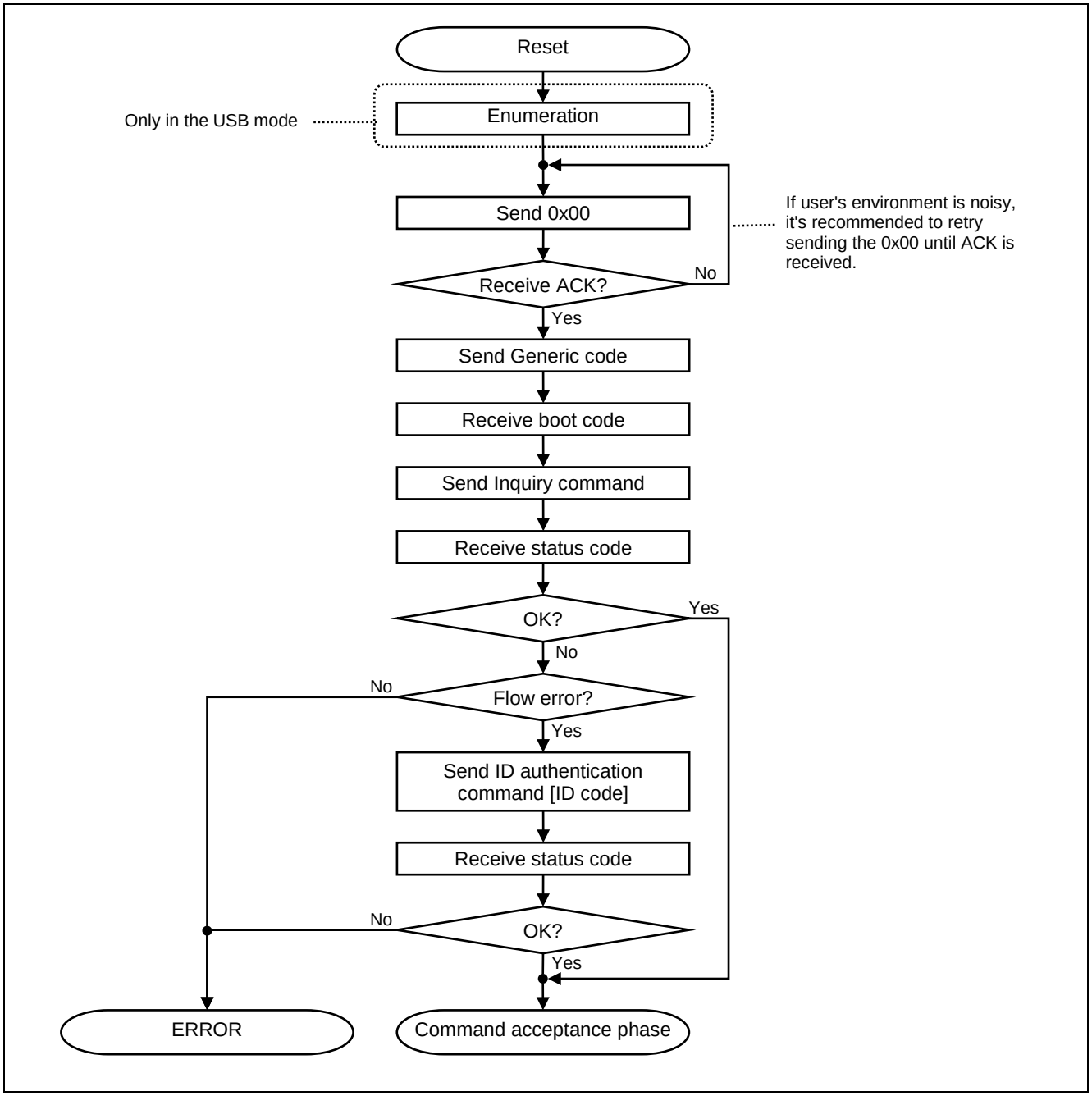


Figure 27. Beginning Communication

3.5.2 Total Area Erasure

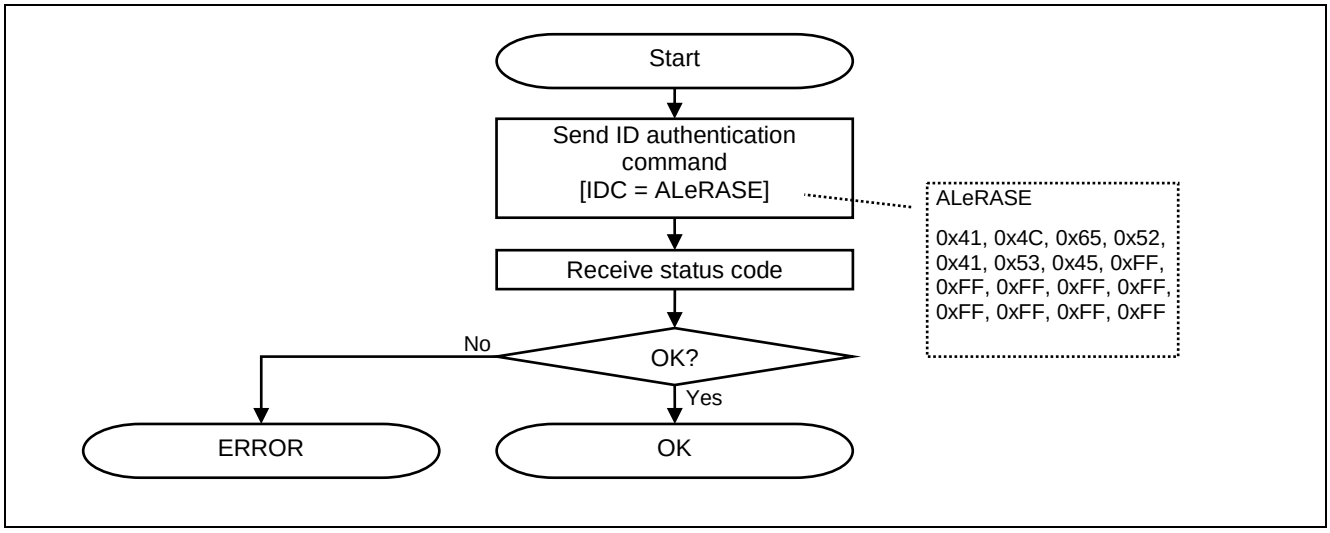


Figure 28. Total Area Erasure

3.5.3 Acquisition of Device Information

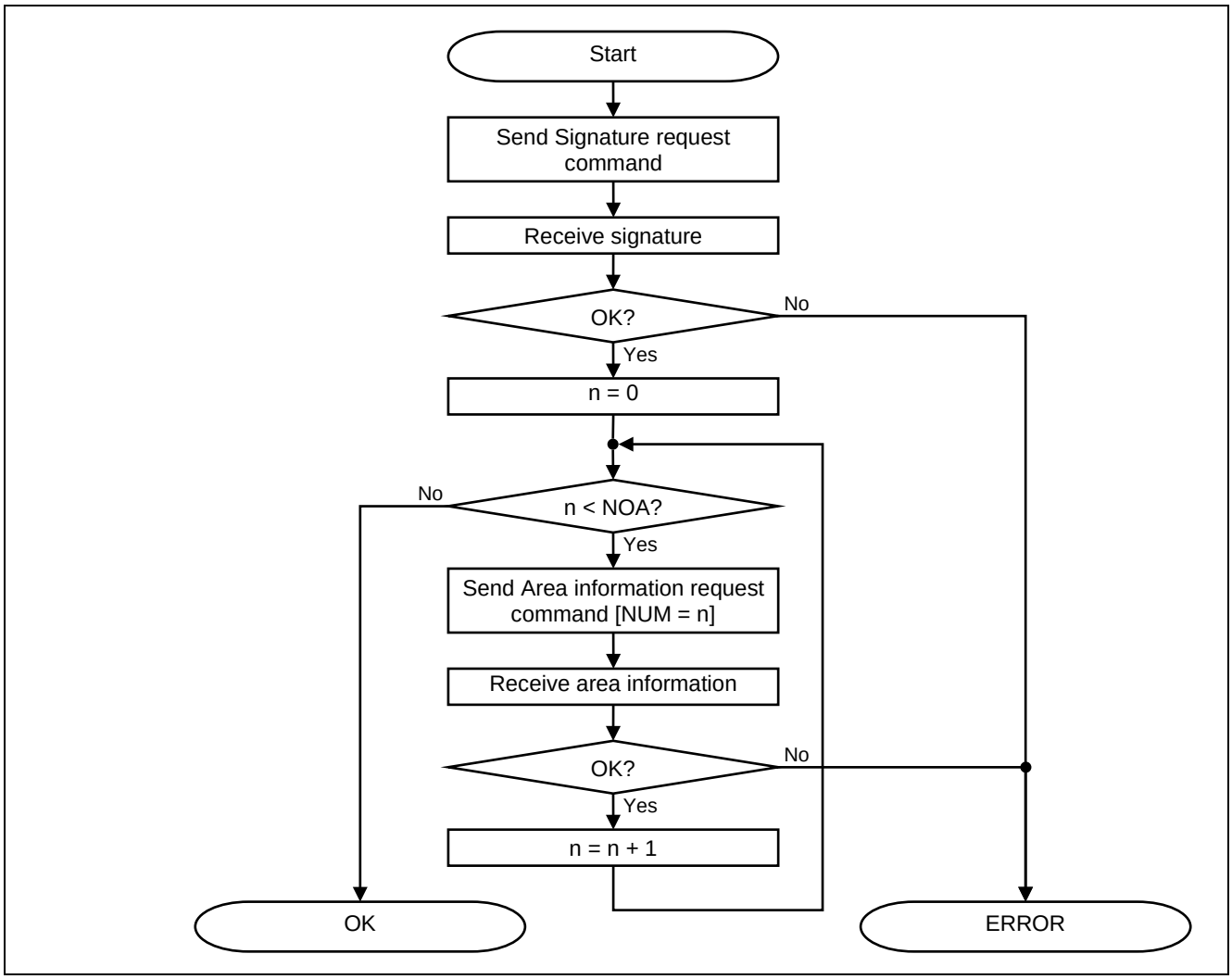


Figure 29. Acquisition of Device Information

3.5.4 Code and Data in User Area Updates

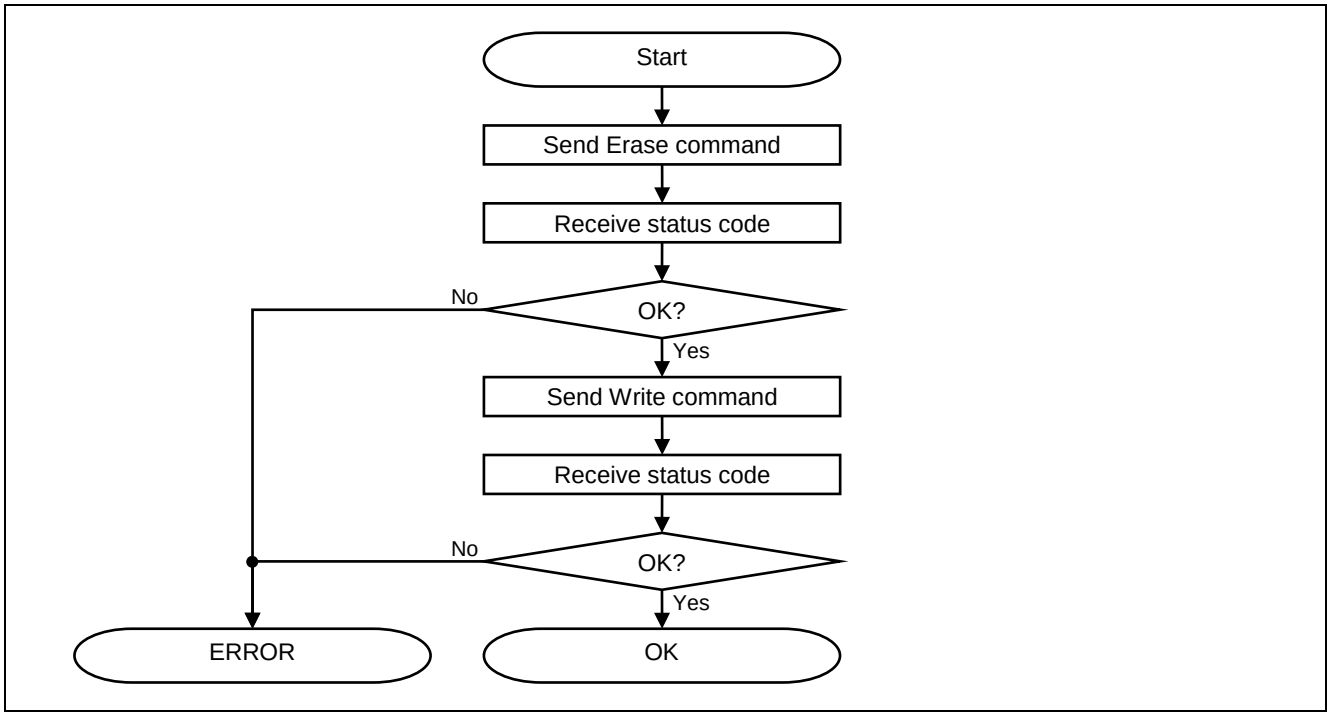


Figure 30. Code and Data in User Area Updates

3.5.5 Configuration Data Updates

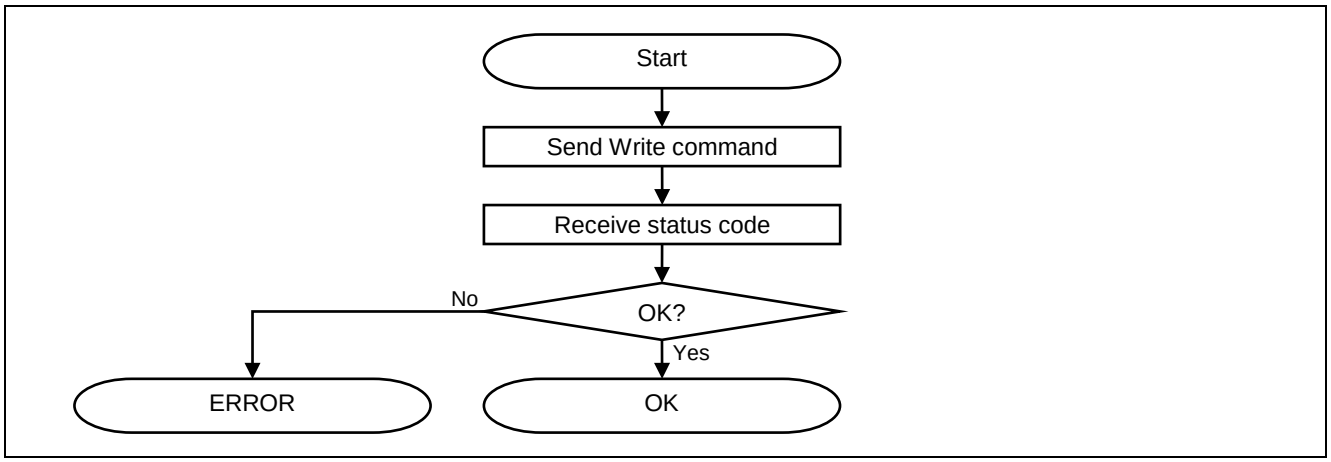


Figure 31. Configuration Data Updates

Website and Support

Visit the following URLs to learn about key elements of the RA family, download components and related documentation, and get support.

RA Product Information	www.renesas.com/ra
RA Product Support Forum	www.renesas.com/ra/forum
RA Flexible Software Package	www.renesas.com/FSP
Renesas Support	www.renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.02.20	—	First release document
1.10	Oct.20.21	1, 6, 8	Addition of RA4W1 and RA6T1

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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