RX72M Group

CPU Card CC-Link IE TSN ClassA Startup Manual

R01AN6978EJ0100
Rev.1.00
Aug. 31, 2023

Introduction

This is a quick start guide to running CC-Link IE TSN Class A communication on the RX72M CPU Card for evaluating industrial networks.

Target Device

RX72M Group

Sample Program

This sample program uses the CC-Link IE TSN Class A stack evaluation version of our partner Sherpa Co., Ltd. The stack's major communications specifications are as follows.

- Transfer protocol: CC-Link IE TSN Class A Version 2.0
- Security policy: None

For purchase of the official version of the stack and the specifications of the sample program, contact

Sherpa Inc.

Sherpa Inc. | Providing a Complete Suite of Real-time Solutions from Sherpa Inc. in Japan (sherpa-tech.jp)

[Restrictions]

The evaluation version CC-Link IE TSN Class A stack has the following functional restrictions.

This version is only made available for purposes of evaluation.

- The evaluation stack automatically stops running after 90 minutes. Re-starting the program requires resetting the device.

This stack cannot be used for embedding in commercial products. In that case, please consider purchasing the official version.

Contents

1. Operating Environment

The sample programs in this manual assumes the following environment.

Table 1.1 Operating Environment

Item	Description
Board	Renesas Electronics RX72M CPU Card Model name: RTK0EMXDE0C00000BJ
CPU	RX CPU (RXv3)
Operating frequency	CPU clock (CPUCLK): 240 MHz
Operating voltage	3.3 V
Operating modes	Single chip mode
Device requirements	R5F572MNDDBD • Code flash memory Capacity: 4 Mbytes ROM cache: 8 Kbytes • Data flash memory Capacity: 32 Kbytes • RAM/extended RAM Capacity: 512 Kbytes / 512 Kbytes
Communications protocol	OPC UA (UA-Binary)
Integrated development environment	e^2 studio (V7.5.0 or later) with the CC-RX compiler (V3.01.00)
Emulator (ICE)	Renesas Electronics On-board emulator E2 On-Board (E2OB)

2. Setting up and Connecting the Evaluation Board

For detailed information on this board, refer to the "RX72M CPU Card with RDC-IC User's Manual" (R12UZ0098EJ0100).

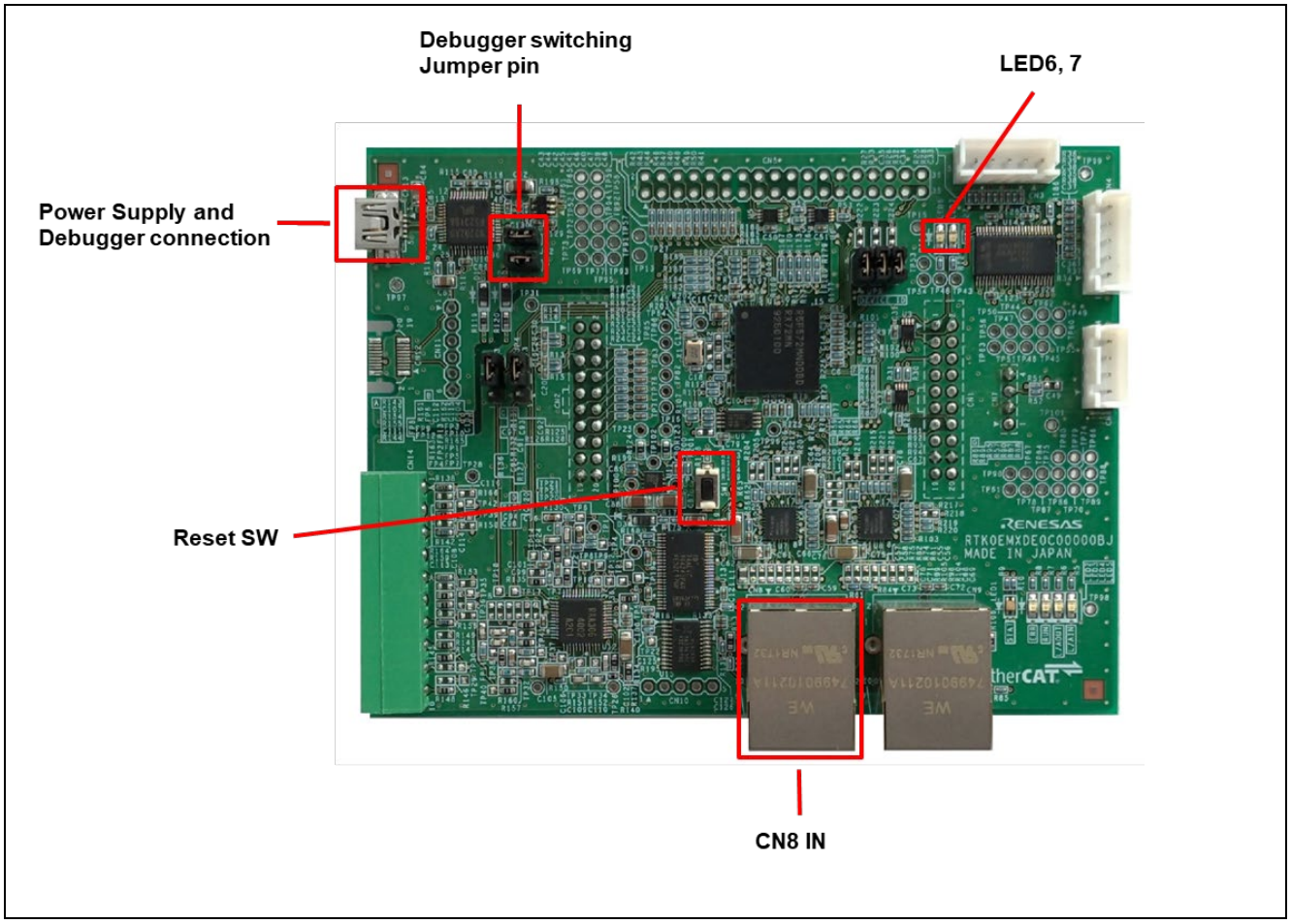


Figure 2.1 Configuration of the RX72M CPU Card

2.1 Download to flash.

CPU Card is equipped with an on-board emulator circuit E2 On-Board (flash programming circuit), which enables flash programming without the need for a separate tool product.

Connect the USB cable to CN13 (USB mini-B connector) and the USB connector of the PC, and write with e2studio.

2.2 CPU Card setting

Set the jumper pins before powering on the CPU Card.
Short the Debugger switching Jumper pins (JP2, JP3) when writing a program to the flash using E2OB.
Remove the jumper pin when executing a program written in the flash.

Using E2OB : Short the Debugger switching Jumper pins (JP2, JP3)

2.3 Power supply selection

CPU Card does not have DC Jack. Input DC5V from the USB connector.
Connect the common USB connector of the emulator and power supply to the host computer via USB.

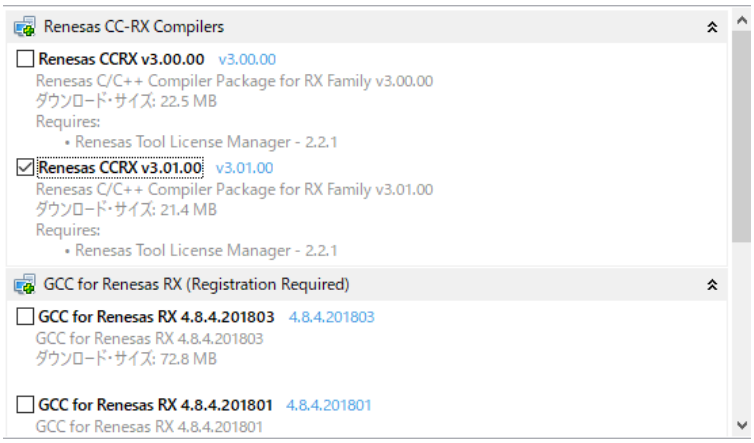
3. Installing the e² studio

Download the e² studio for RX72M (V7.5.0 or later) from the Web site below.

https://www.renesas.com/e2studio_download

3.1 Installing the CC-RX Compiler V3.01.00

The compiler selection dialog box appears while installing the e² studio. Click [Renesas CCRX v3.01.00] and select [Next]. CC-RX V3.01.00 Compiler for RX72M will be installed with the e² studio.



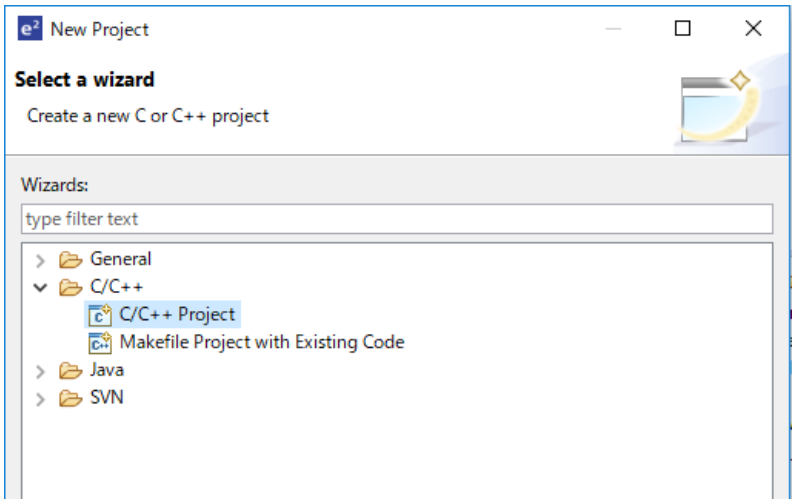
To start the e² studio, execute "e2studio.exe" in the following installation folder.

e2_studio_rx72m\eclipse

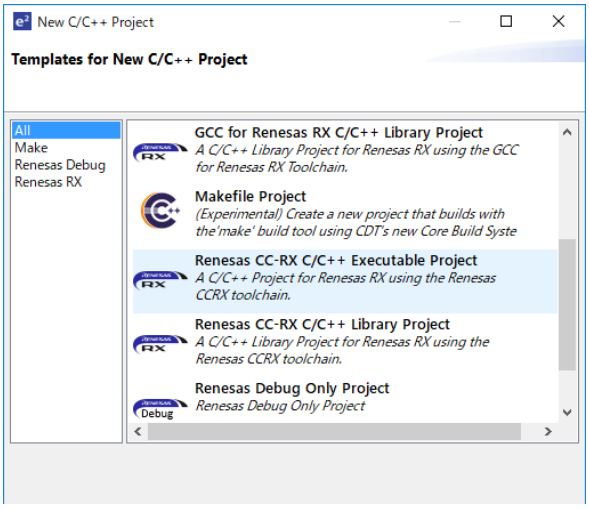
3.2 How to check the registered Compiler

(1) Start the e2 studio.

(2) Select [File] → [New] → [C/C++Project] → [Next].



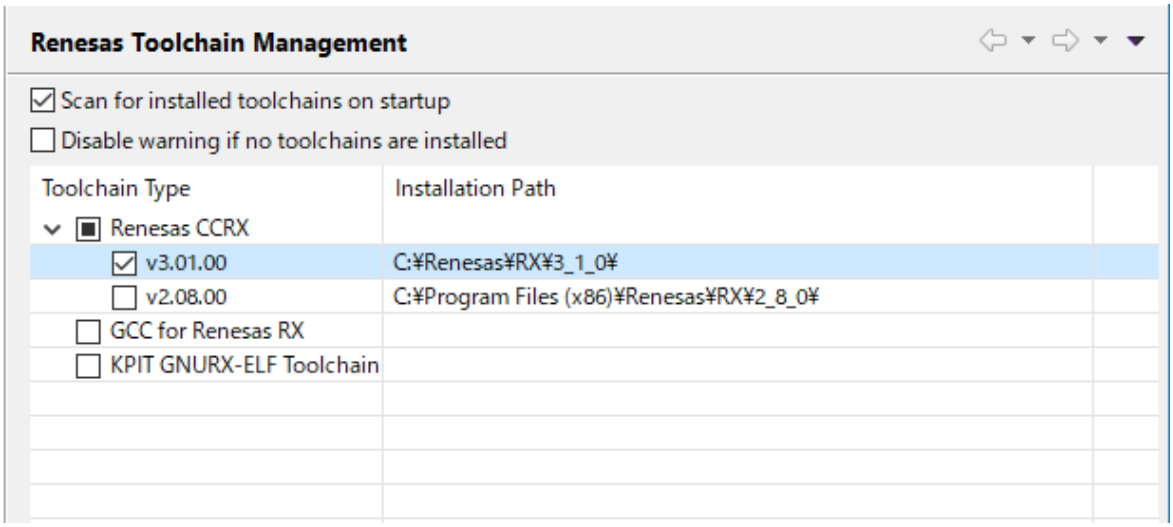
(3) In the [Templates for New C/C++ Project] dialog box, select [Renesas RX] → [Renesas CC-RX C/C++ Executable Project] → [Next].



(4) In the [New Renesas CC-RX C/C++ Executable Project] dialog box, enter a desired project name and select [Next].

(5) In the [Select toolchain, device & debug settings] dialog box, select [Manage Toolchains...] under [Toolchain Settings].

(6) In the [Renesas Toolchain Management] dialog box, the registration was successful if "v3.01.00" has been added under "Renesas CCRX".

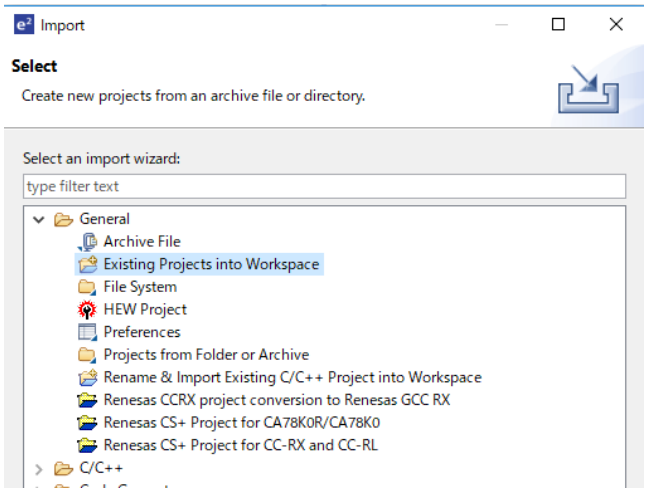


4. Importing a Sample Project to the e² studio

(1) Extract the archived sample project and store it in any folder.

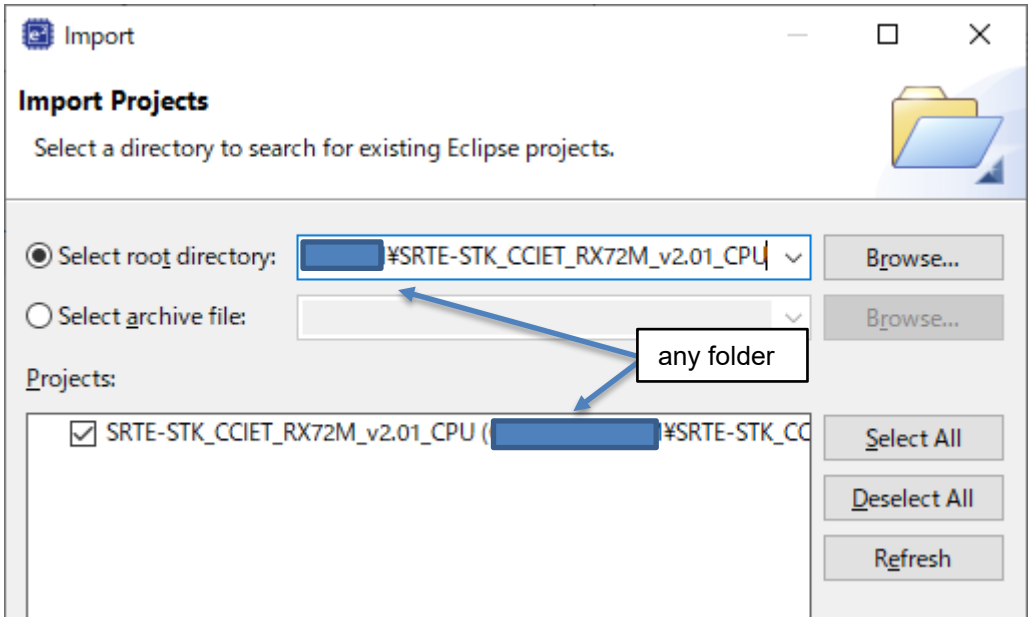
(2) Select [File] → [Import].

(3) In the [Select] dialog box, select [General] → [Existing Projects into Workspace] and select [Next].



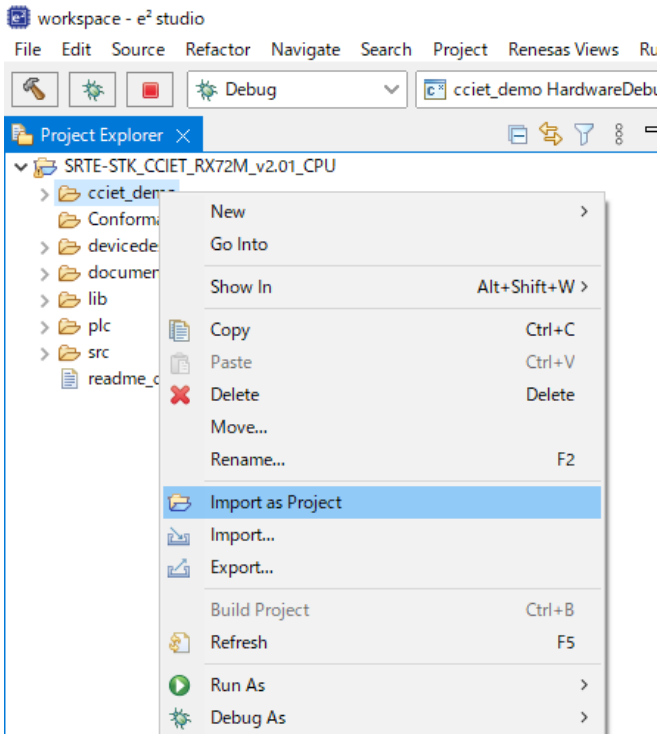
(4) In the [Import Projects] dialog box, check the "Select archive file:" button, then select [Browse...].

(5) Select the " SRTE-STK_CCIET_RX72M_v***_CPU " folder of the sample project stored in any folder in (1), and select [Open].



Check " SRTE-STK_CCIET_RX72M_v***_CPU (/SRTE-STK_CCIET_RX72M_v***_CPU) " under the "Projects" label and select [Next]. The project will be imported into the workspace.

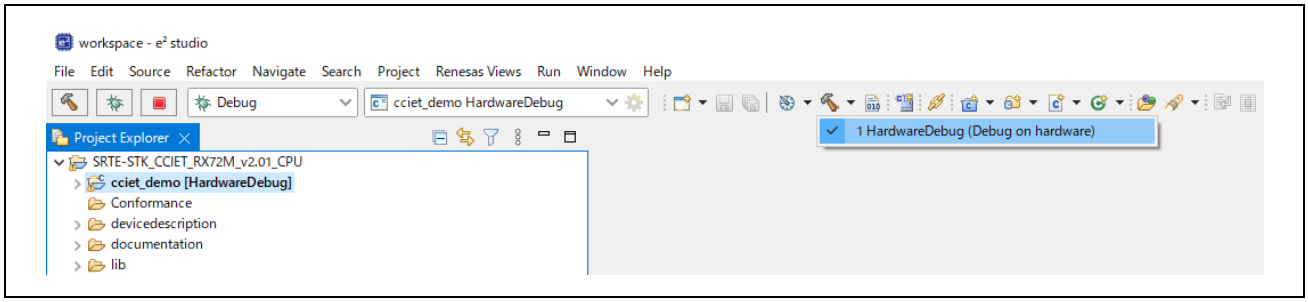
(6) Right-click the "cciet_demo" folder and select [Import Project] from the submenu. This will import the project file of the sample program, and will be able to build and run it.



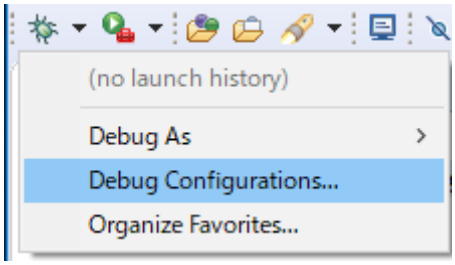
5. Programming and Debugging

(1) Select the " cciet_demo " project in the Project Explorer view. Select the arrow next to the build button (hammer icon) and select [HardwareDebug] from the drop-down menu.

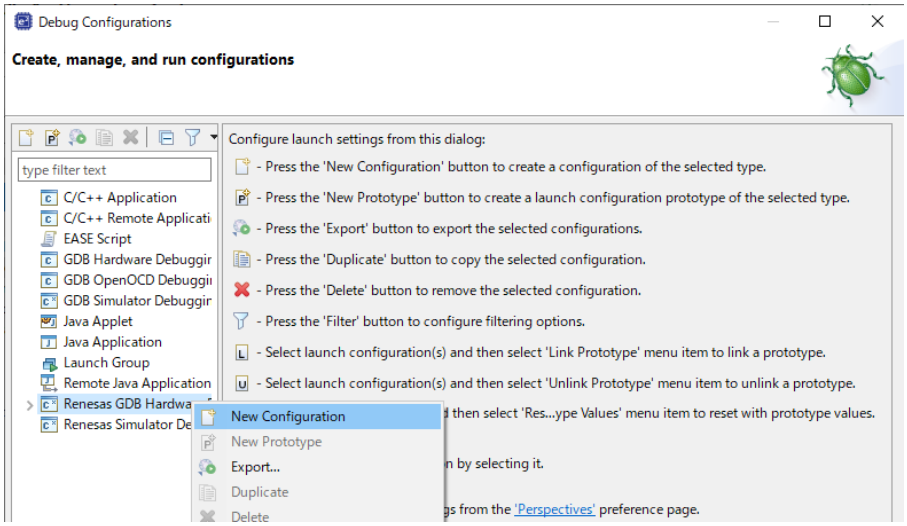
Selecting [Hardware Debug], e2 studio will build the project.

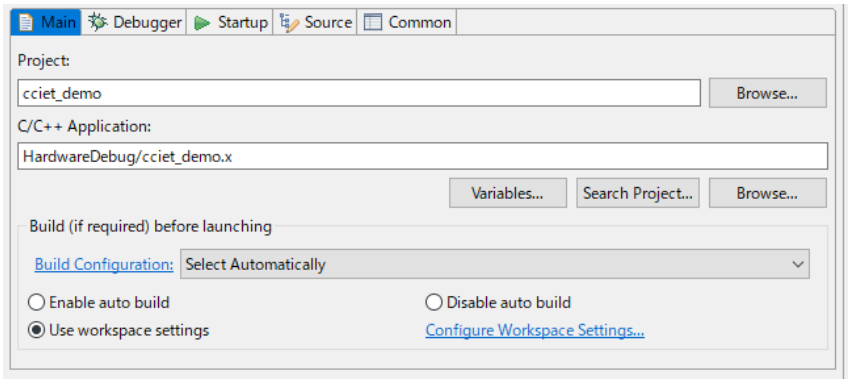


(2) e2 studio will build the project. After the build is completed, select the arrow next to the debug button (bug icon). You can start debugging by selecting [Debug Configurations...].

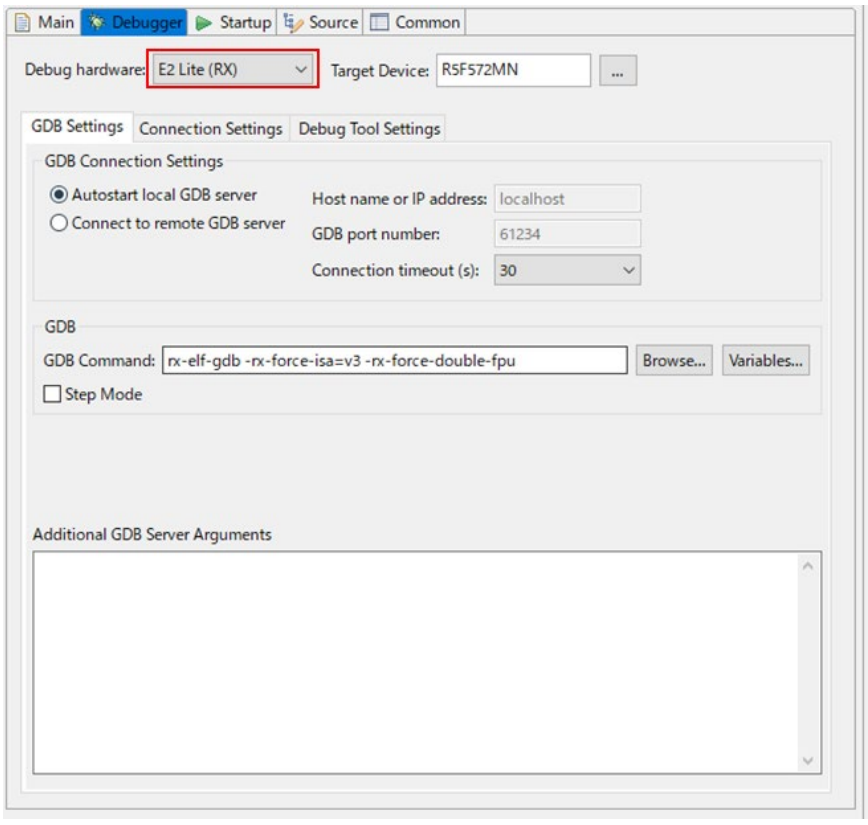


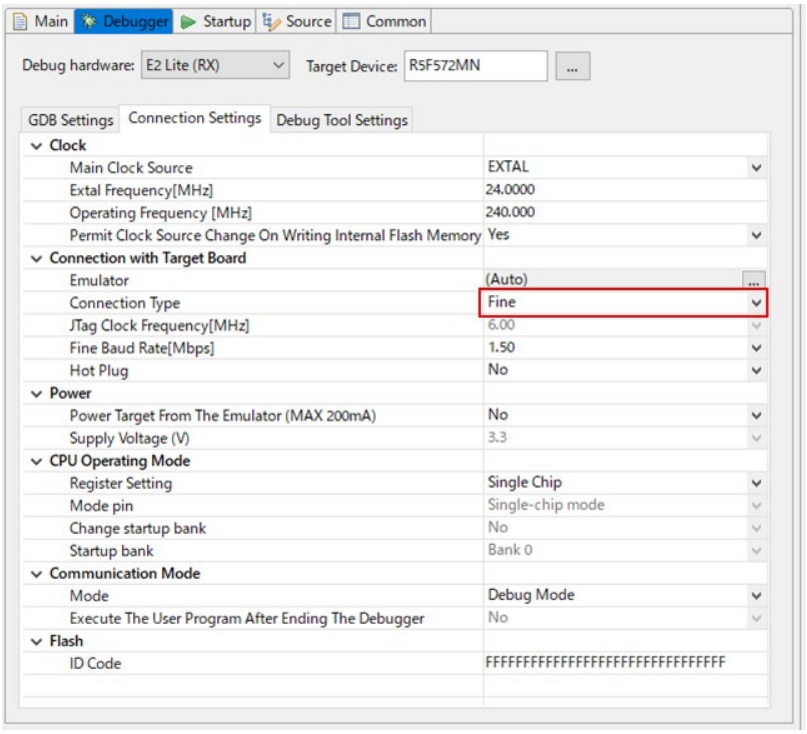
(3) Make debugger settings. A setting example is as follows.

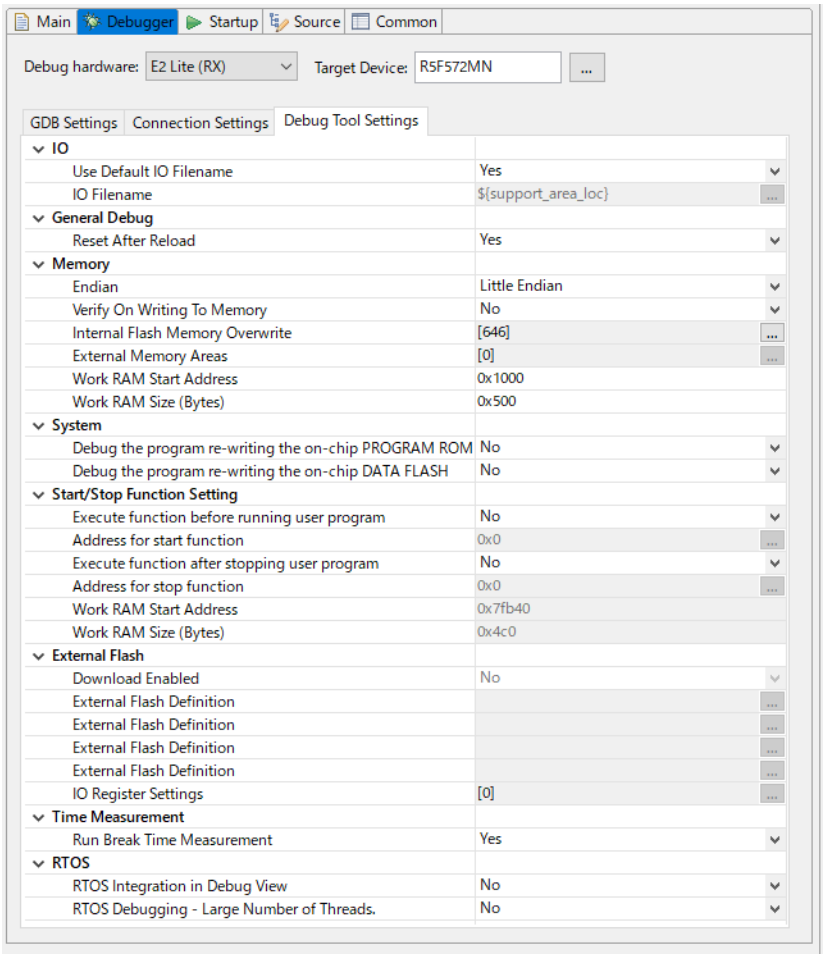




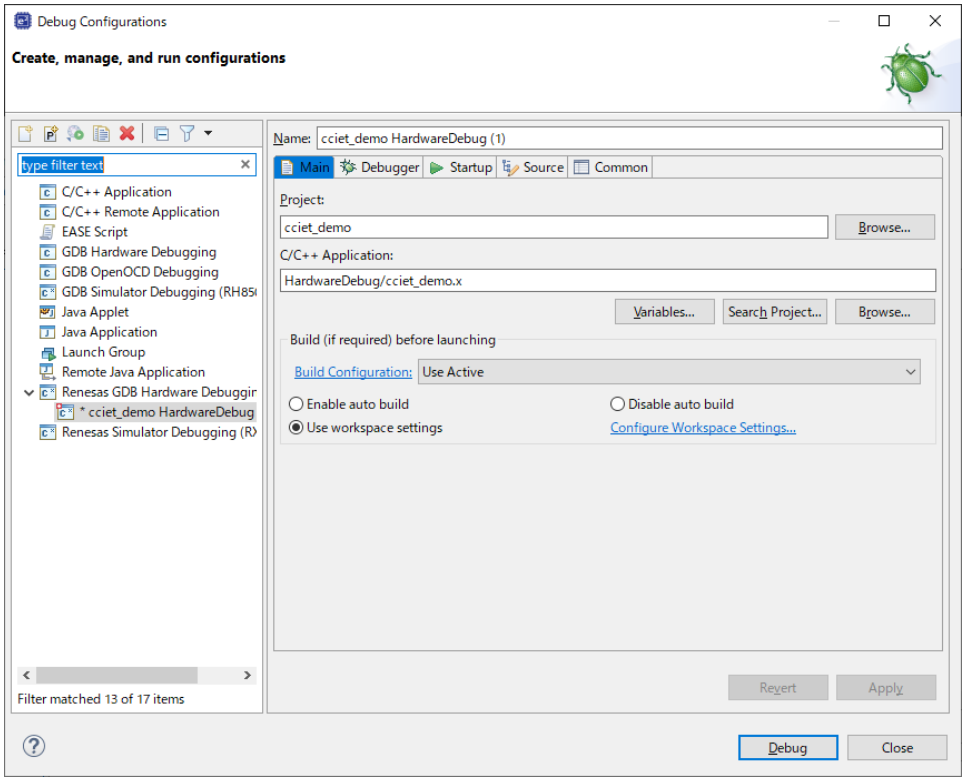
Set up E2OB. E2OB functions as an emulator equivalent to E2Lite, so when connecting, set the emulator type to "E2Lite" and the communication interface to "FINE". See below for other settings.




Main
Debugger
Startup
Source
Common
Debug hardware: E2 Lite (RX)
Target Device: R5F572MN
GDB Settings
Connection Settings
Debug Tool Settings
Clock
Main Clock Source: EXTAL
Extal Frequency[MHz]: 24.0000
Operating Frequency [MHz]: 240.000
Permit Clock Source Change On Writing Internal Flash Memory: Yes
Connection with Target Board
Emulator: (Auto)
Connection Type: Fine
JTag Clock Frequency[MHz]: 6.00
Fine Baud Rate[Mbps]: 1.50
Hot Plug: No
Power
Power Target From The Emulator (MAX 200mA): No
Supply Voltage (V): 3.3
CPU Operating Mode
Register Setting: Single Chip
Mode pin: Single-chip mode
Change startup bank: No
Startup bank: Bank 0
Communication Mode
Mode: Debug Mode
Execute The User Program After Ending The Debugger: No
Flash
ID Code: FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF


Main
Debugger
Startup
Source
Common
Debug hardware: E2 Lite (RX)
Target Device: R5F572MN
GDB Settings
Connection Settings
Debug Tool Settings
IO
Use Default IO Filename: Yes
IO Filename: ${support_area_loc}
General Debug
Reset After Reload: Yes
Memory
Endian: Little Endian
Verify On Writing To Memory: No
Internal Flash Memory Overwrite: [646]
External Memory Areas: [0]
Work RAM Start Address: 0x1000
Work RAM Size (Bytes): 0x500
System
Debug the program re-writing the on-chip PROGRAM ROM: No
Debug the program re-writing the on-chip DATA FLASH: No
Start/Stop Function Setting
Execute function before running user program: No
Address for start function: 0x0
Execute function after stopping user program: No
Address for stop function: 0x0
Work RAM Start Address: 0x7fb40
Work RAM Size (Bytes): 0x4c0
External Flash
Download Enabled: No
External Flash Definition
External Flash Definition
External Flash Definition
External Flash Definition
IO Register Settings: [0]
Time Measurement
Run Break Time Measurement: Yes
RTOS
RTOS Integration in Debug View: No
RTOS Debugging - Large Number of Threads.: No

(4) After setting the debugger, click the [Debug] button to download the program to the target.



(5) If a firewall warning is displayed for "e2-server-gdb.exe", check the checkbox for [Private networks, such as my home or work network] and select [Allow access].

(6) The User Account Control (UAC) dialog box may appear. Enter the administrator's password and select [Yes].

(7) If the Confirm Perspective Switch dialog box appears prompting you to switch the perspective, check the checkbox for [Remember my decision] and select [Yes].

(8) After downloading the code, select the [Resume] button to run the code. The code will break at the address where the main function starts. Select the [Resume] button again to continue to run the code.

6. Appendix

6.1 Verifying Operation of the Sample Program

Operation of the sample program can be verified as follows.

6.1.1 Operation check using GX-Works3

CC-Link IE TSN communication can be checked using Mitsubishi Electric's sequencer (PLC) MELSEC iQ-R series RJ71GN11-T2 as the master station.

The table below shows examples of sequencer unit combinations.

Table 6.1 List of Devices

	Unit type	Model No
Base	basic base unit	R35B
Power supply	Power supply unit	R61P
CPU	Sequencer CPU unit	R04CPU
Network	CC-Link IE TSN master/local module	RJ71GN11-T2

Note: Refer to the following manual for the connection method and how to use each unit.
- MELSEC iQ-R Module Configuration Manual (SH-081222)
- MELSEC iQ-R CPU Module User's Manual (Startup) (SH-081223)
- MELSEC iQ-R CC-Link IE TSN User's Manual (Startup) (SH-082126)

This section describes the procedure for checking communication using a sequencer that combines these units and its engineering tool GX Works3.

6.1.2 Connection configuration

Connect each cable below.

(a) Connect the Ethernet cable of the evaluation board and the network unit of the sequencer

(b) Connect the sequencer CPU unit and PC with a USB (miniB) cable

After connecting, confirm that the RUN/STOP/RESET switch of the CPU unit of the sequencer is set to STOP (program stop), and then turn on the power of the sequencer.

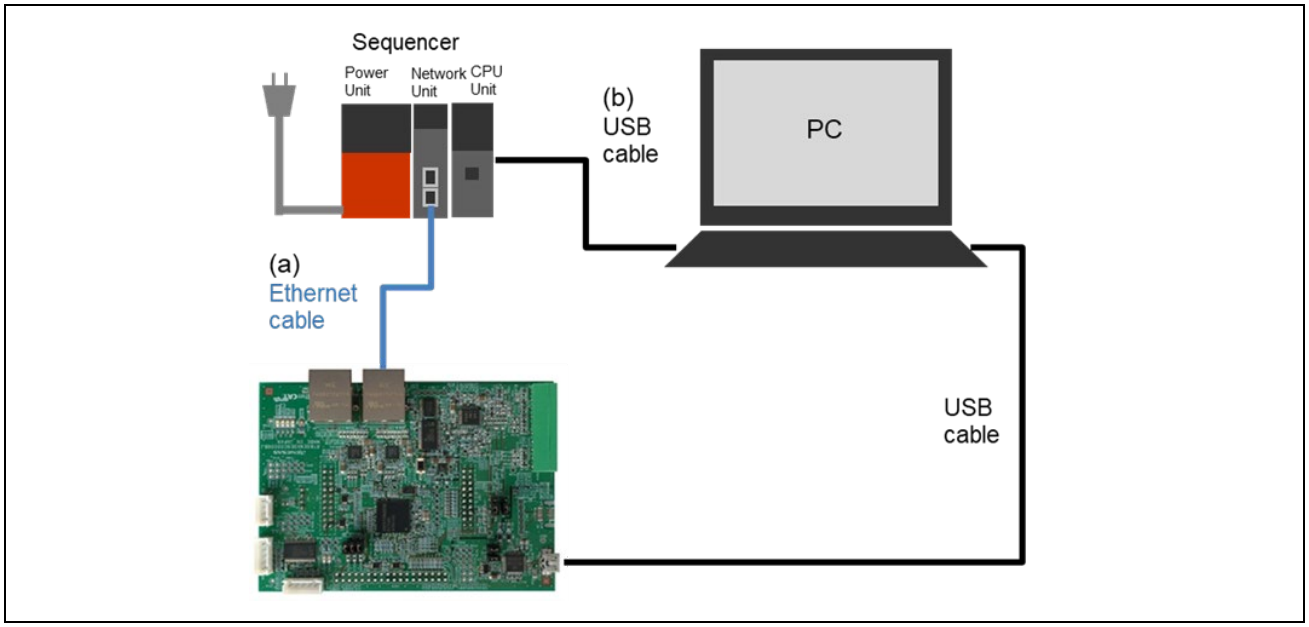


Figure 6.1 Connection configuration

6.1.2.1 Connection with the Communication Board

IP address set in the sample program is set to "192.168.1.10".
When changing the IP address, please change the following IP address settings.
\src\sample\sdai\appl_arm_itron\demo_setup.h
Change DEFAULT_IPADDRESS in #if defined _CCIET_

#define DEFAULT_IPADDRESS 0xC0A8010A /* IP address (192.168. 1. 10) The lower 16 bits are ignored, since setting a CC-Link IE TSN Address Offset. */

```
/*------------------------------------------------------------------------------
 CCIETA Slave
 These are defualut's and demo's macros for CCIETA on RIN_ENGINE.
 Please change the values of the following macros for your sysmtem.
*------------------------------------------------------------------------------*/
#if defined _CCIET_
#define DEMO_VENDORID               0x6700   /* vendor code */
#define DEMO_DEVICEID               0x0003   /* device type */
#define DEMO_DEVICE_VERSION         102      /* device version */
#define DEMO_DEVICE_MODEL_CODE      0x00000001 /* device model code */
#define DEMO_DEVICE_NAME            "dut"

#define DEMO_SERIALNUMBER           1234567890L
#define DEMO_PRODUCTNAME            "Sherpa-sample-dev"
#define DEMO_ORDERID                "SDAI-sample-app"

#define DEFAULT_IPADDRESS           0xC0A8010A /* IP address  (192.168.  1. 10)  The lower 16 bits are ig
#define DEFAULT_SUBNETMASK          0xFFFFFF00 /* Subnet mask (255.255.255.  0) */
#define DEFAULT_GATEWAY             0x00000000 /* Gateway     (  0.  0.  0.  0) */
```

Figure 6.2 IP address setting

IP address "192.168.1.10" is set in the sequencer sample project file.
When changing the IP address, change the sequencer program accordingly.

6.1.2.2 CSP+ file registration

Register the CSP+ file included in the sample program to GX Works3.
CSP+ file is in the following path in the sample program.

CSP+ files:
(root)\devicedescription\cciet\0x6700_SherpaSamp_r01_102_en.zip

From the GX Works3 menu, select [Tool] - [Profile Management] - [Register] to register the CSP+ file.

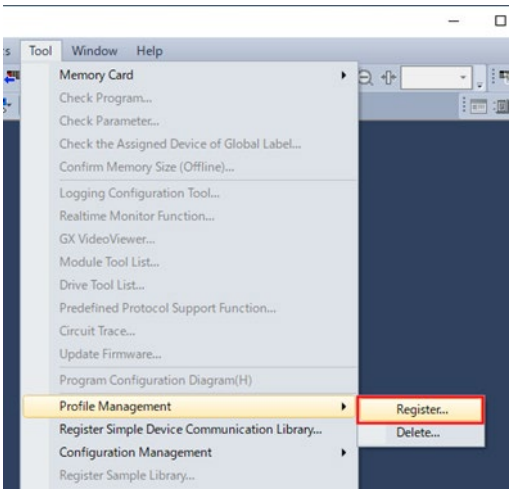


Figure 6.3 Registering CSP+ files

6.1.2.3 Start the sample project.

Double-click the sample project file to start GX Works3.
The project file is in the following path in the sample program.

GX Works3 project file path:
(root)\plc\GxWorks3\SRTE-STK_CCIET_RX72M_R04.gx3

6.1.2.4 Download

Follow the steps below to write to the sequencer.

(1) Select menu [Convert] – [Convert] to build.

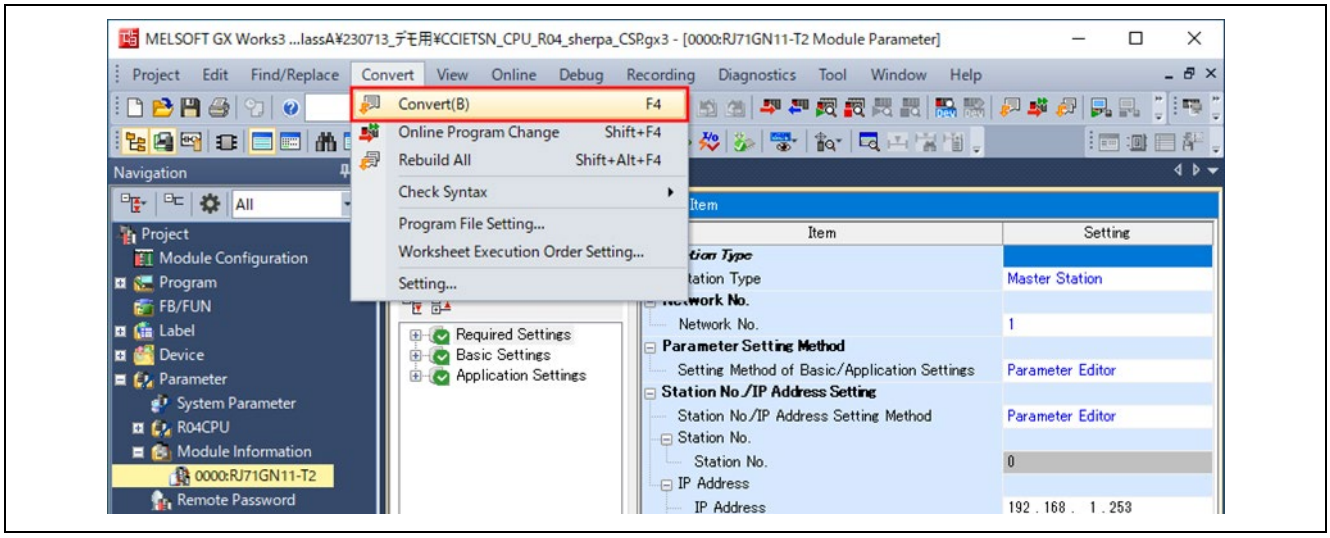


Figure 6.4 GX Works3 download procedure <build display>

(2) Select the menu [Online] → [Write to PLC] to open the online data operation screen.

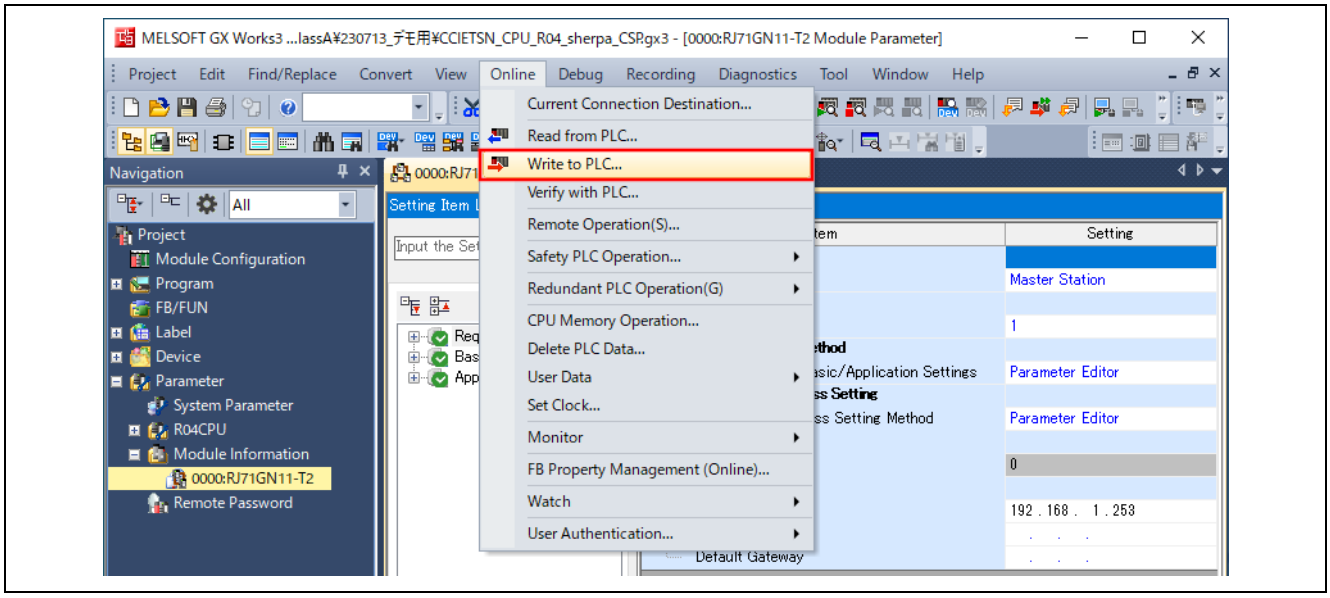


Figure 6.5 GX Works3 download procedure <Main display>

(3) Click [Select All] for the write target.

(4) Start writing with [Execute]. (If an overwrite confirmation dialog appears, click [Yes to all].)

(5) Write to sequencer screen displays the progress of writing to the sequencer, so when writing is complete, click [Close] on the write to sequencer screen and the online data operation screen to close them.

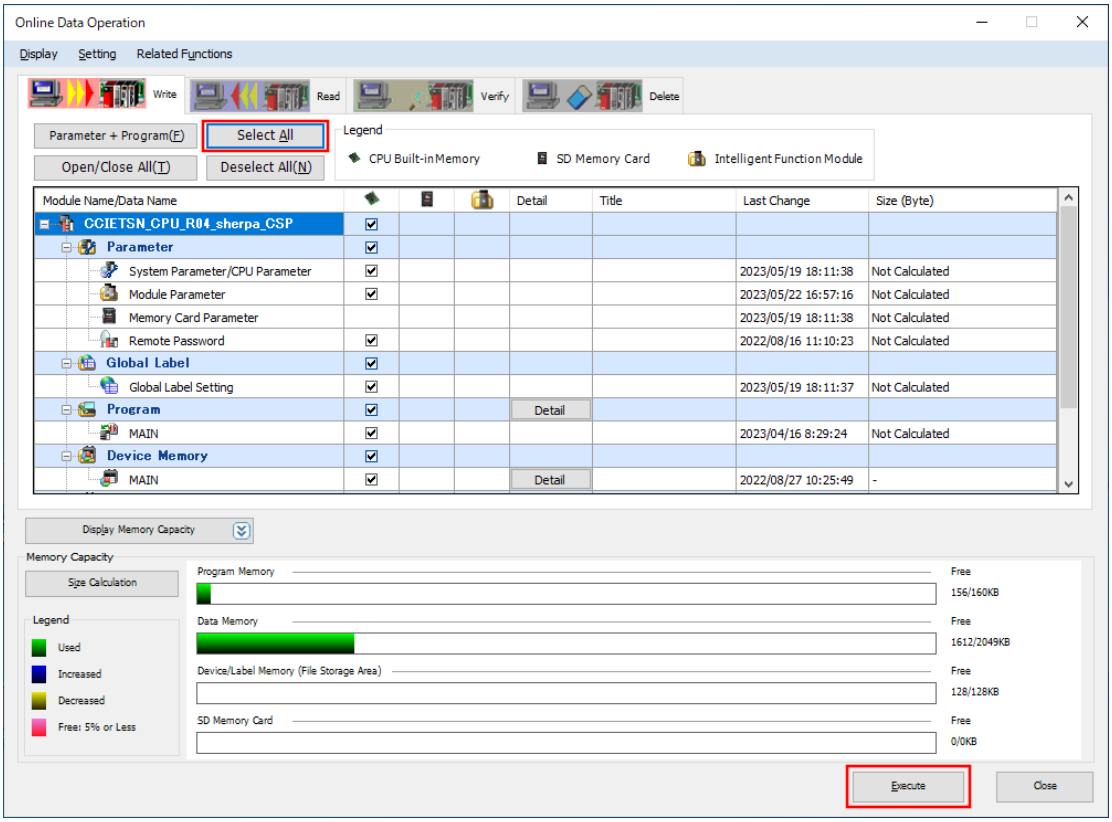


Figure 6.6 GX Works3 download procedure <Online data operation display>

6.1.2.5 Connection confirmation

Hold the RUN/STOP/RESET switch on the sequencer CPU unit to the RESET side for about 1 second to reset the sequencer. After that, push it to the RUN side and execute the written program.

i. Check data link

To establish the data link, confirm that the D.LINK LED is lit on the network module of the sequencer.
It is also possible to check the details of the connection status using the diagnosis function of GX Works3.
Select the menu [Diagnosis] → [CC-Link IE TSN/CC-Link IE Field diagnosis], and check the status of each device on the CC-Link IE TSN/CC-Link IE Field diagnosis screen.

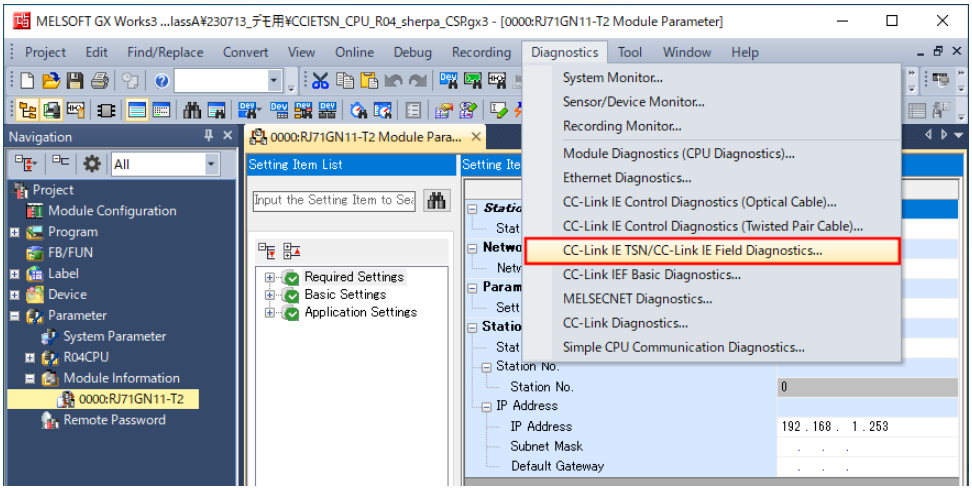


Figure 6.7 GX Works3 connection check procedure <Main display>

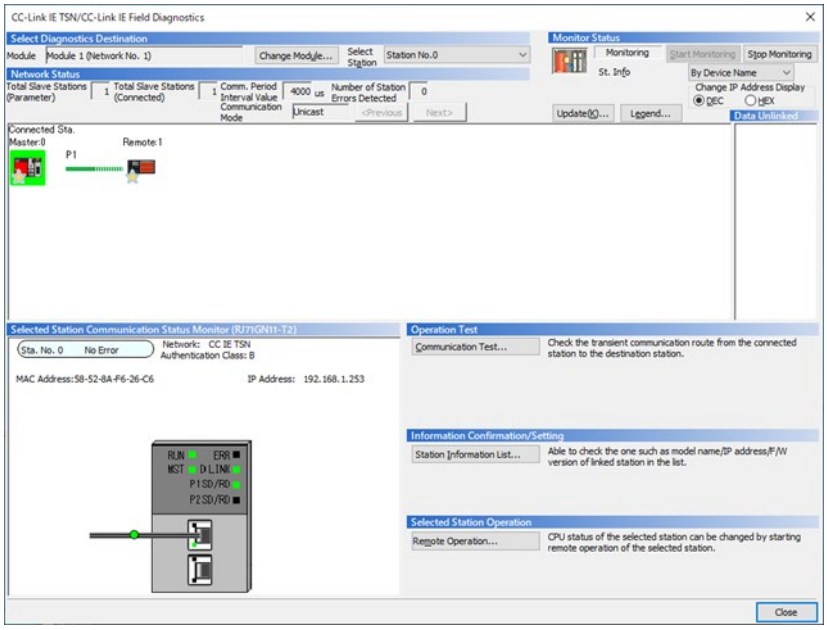


Figure 6.8 GX Works3 connection check procedure <CC-Link IE TSN/CC-Link IE Field diagnosis display>

[Note] For how to read the diagnosis, refer to the following manual.

MELSEC iQ-R CC-Link IE TSN User's Manual (Application) (SH-082128)

ii. Cyclic transmission reception confirmation

Reception of cyclic transmission can be confirmed with the LED.
GX Works3 sample project file increments the cyclic transmission RY output data at regular intervals.
RX72M sample program indicates the lower bits of the received RY data with general-purpose LEDs (LED6, LED7).

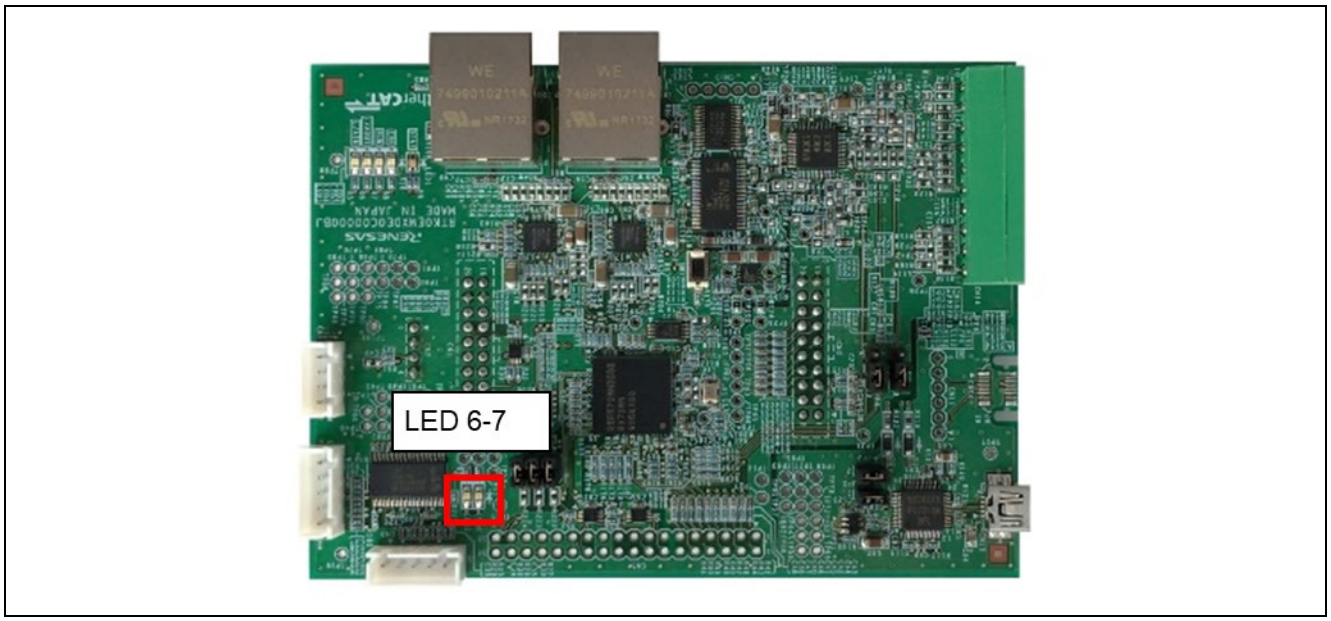


Figure 6.9 Cyclic transmission reception confirmation LED

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Aug. 31, 2023	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
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