

RX72N Group

Precautions Regarding High-Temperature Operation of RX72N Group

Summary

This document provides thermal design considerations for G-version products capable of high-temperature operation and derating examples for typical high-temperature application cases.

Contents

1. Relationship between Actual Usage Environment and Reliability of RX Family Products.....	2
1.1 Conceptualizing MCU Reliability	2
1.2 Derating	2
2. Definitions of Thermal Characteristics.....	3
3. Thermal Design	4
3.1 Tj Calculation Examples	4
3.1.1 Precautions When Calculating Tj	4
3.1.2 Calculating Tj from Temperature at Center of Package Top Tt	4
3.1.3 Precautions when Calculation Tt.....	4
3.2 Thermal Design Parameters	6
3.2.1 RX72N Group Thermal Design Parameters.....	6
3.3 Calculating Power Consumption (Pd)	7
4. Derating Examples for Typical High-Temperature Applications	9
5. Reference Document.....	11
Revision History.....	12

1. Relationship between Actual Usage Environment and Reliability of RX Family Products

1.1 Conceptualizing MCU Reliability

When using RX Family MCUs, the following precautions should be observed in order to ensure device reliability.

The reliability of a semiconductor device is expressed as a failure rate curve (bathtub curve). Device failures can be classified into three types: initial failures, which occur comparatively early on after the device enters use (operation); random failures, which occur over a long period of time; and wear-out (life span) failures, which become more frequent over time at the end of the intended lifetime of the device. For details on bathtub curves, refer to Semiconductor Reliability Handbook, rev. 2.50 (R51ZZ0001EJ0250).

Of the above, wear-out failures have a particularly large dependency on the temperature environment in which the semiconductor device is used. To prevent RX MCUs from undergoing wear-out failure, it is important to think about derating.

1.2 Derating

Derating is defined in JIS Z 8115 reducing a load systematically by operating a device under its rated maximum capacity to enhance reliability.

The quality and reliability of a device are greatly influenced by its usage environment. If a device is used under harsh conditions, its reliability decreases, or it increases when used under mild conditions. If a device is used in an extremely harsh usage environment equivalent to life time tests. Even if the maximum ratings are not exceeded, using a device under very harsh conditions equivalent to lifetime testing can cause wear-out failure. Thus, it is very important to think about derating.

Derating is applied to product groups, such as discrete devices and power ICs, that require adjustment of the operating conditions, such as ambient temperature, junction temperature, voltage, current, and power, which are mutually related. This is because in addition to having wide usage condition ranges these products have the property that even if they are operated within the corresponding usage range (e.g. voltage), concern for the junction temperature will be required due to the relationships between characteristics such as the power generated, ambient temperature, and heat sink used.

For details on derating, refer to 5.2.3, Derating, in Semiconductor Reliability Handbook, rev. 2.50 (R51ZZ0001EJ0250).

This application note presents high-temperature profiles for typical high-temperature applications and derating examples for RX Family MCUs.

2. Definitions of Thermal Characteristics

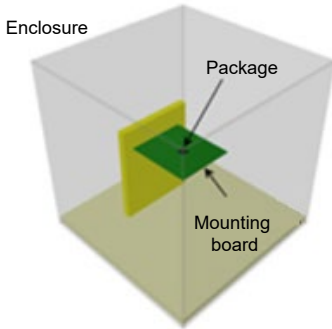
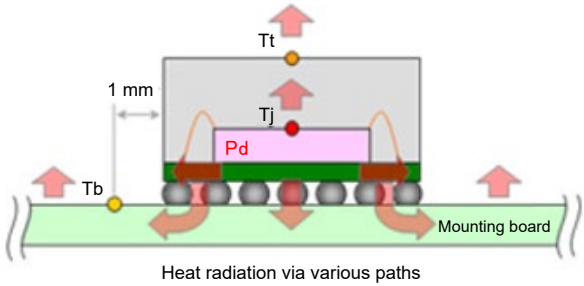
The definitions of thermal characteristics are based on the JEDEC specification referenced below. For details, refer to the following URL:

<https://www.renesas.com/us/en/support/technical-resources/packaging/characteristic/heat-dissipation>

Table 2.1 ICs: Definitions of Thermal Characteristics

θ_{ja}	Definition	The thermal resistance between the junction temperature (T_j) and ambient temperature (T_a) when the package is mounted on the board. Two types of environment are considered: one in which only natural convection occurs, and one in which forced air cooling is assumed
	Application	Comparison of heat radiation performance of different packages
ψ_{jt}	Definition	A thermal design parameter that expresses the temperature difference between the junction temperature (T_j) and the temperature at the center of the package top (T_t), relative to the power consumption (P_d) of the device overall
	Application	Estimation of the junction temperature (T_j), based on ψ_{jt} calculated in an appropriate environment, T_t and P_d

T_a : Temperature in location not affected by heat generation source

Thermal Characteristic	θ_{ja}	ψ_{jt}
Environment		
	<ul style="list-style-type: none"> Enclosure: 304.8 × 304.8 × 304.8 mm (JEDEC51-2 conformant) Mounting board: <ul style="list-style-type: none"> BGA 40 mm square or less → 101.6 × 114.3 × t1.6 mm, 4 layers (JEDEC51-9 conformant) QFP 27 mm square or more → 101.6 × 114.3 × t1.6 mm, 4 layers (JEDEC51-7 conformant) QFP less than 27 mm square → 76.2 × 114.3 × t1.6 mm, 4 layers (JEDEC51-7 conformant) 	
Definition expression	$\theta_{ja} = \frac{T_j - T_a}{P_d}$	$\psi_{jt} = \frac{T_j - T_t}{P_d}$

3. Thermal Design

Generally speaking, the junction temperature of a semiconductor device affects the lifetime of the device and, if it rises too high, can destroy it. For this reason, system chips with high power consumption have a specified junction temperature (T_j) range, and it is necessary to ensure that the thermal design is such that the junction temperature remains within the allowable range during operation.

If the usage environment is such that the limit of the junction temperature (T_j) allowable range is likely to be approached or exceeded, calculate the junction temperature. Calculate the T_j in your own specific use case to confirm that it is below the maximum allowable junction temperature. If the result exceeds the maximum allowable value, reconsider the component layout, enclosure configuration, and power consumption.

It is not possible to measure the junction temperature (T_j) directly, so it is necessary to calculate it from the power consumption or surface temperature by using the thermal design parameters.

3.1 T_j Calculation Examples

3.1.1 Precautions When Calculating T_j

θ_{ja} is calculated in the environment following the JEDEC specifications, so the values may vary greatly according to the layout of the mounting board, enclosure etc. As T_j obtained from θ_{ja} may deviate from T_j measured in actual usage environment of customers, please confirm T_j by [3.1.2 Calculating T_j from Temperature at Center of Package Top (T_t)] at last.

3.1.2 Calculating T_j from Temperature at Center of Package Top T_t

Estimate the temperature at the center of the package top (T_t) in your usage environment and the thermal design parameter (ψ_{jt}) of the chip, calculate the junction temperature (T_j) using the formula given below.

$$T_j = T_t + P_d \times \psi_{jt}$$

T_j: Junction temperature [°C]

T_t: Temperature at center of package top [°C]

P_d: Overall power consumption of chip [W]

ψ_{jt}: Thermal design parameter [°C/W] from junction temperature (T_j) to center of package top

Note 1. For P_d, refer to [3.3, Calculating Power Consumption \(P_d\)](#).

Note 2. For ψ_{jt}, refer to [3.2, Thermal Design Parameters](#).

If the junction temperature (T_j) exceeds 125°C, reconsider the component layout, enclosure configuration, and power consumption, as necessary.

3.1.3 Precautions when Calculation T_t

- Measurement Using a Thermocouple

To ensure accurate temperature measurements, care should be taken regarding the thermocouple used and the manner in which it is attached to the measurement target.

Some precautions and suggestions are presented below:

- Use a thermocouple with wires that are as thin as possible. (Due to limitations on heat extraction, the recommended wire diameter is 150 μm or less.)
- A K-type thermocouple is recommended. (T-type thermocouples tend to generate a lot of heat, and they may provide artificially low temperature measurements.)
- Use heat-resistant plastic tape or a heat-resistant plastic material to secure the thermocouple in place.
- Secure the thermocouple firmly to the measurement target. (Any looseness may result in measurement error.)

- Measurement Point

Confirm that the temperature is in the saturation state and measure T_t at the center of the top surface of the package.

- Measurement Using a Thermographic Camera

To ensure accurate temperature measurements, set the emissivity of the measurement target on the thermographic camera. The emissivity of the board surface is typically 0.8 to 0.9, but that of metal surfaces is generally lower. (Performing measurements of a metal surface with a setting of 0.8 to 0.9 will result in a lower measured value than the actual temperature.) If the emissivity is unclear, prepare the surface by applying black body spray or the like. Setting the emissivity to that of the black body spray will enable you to obtain an accurate temperature measurement.

Note that any objects between the thermographic camera and the measurement target (even a transparent acrylic panel) will prevent you from obtaining accurate measurements. (In this example, the thermographic camera would be measuring the temperature of the transparent acrylic panel.)

Depending on the layout of the measurement target, measurement using a thermographic camera might be more difficult than measurement using a thermocouple, but it is an effective way to determine the temperature distribution. It is therefore recommended that a thermographic camera and a thermocouple be used in combination.

3.2 Thermal Design Parameters

3.2.1 RX72N Group Thermal Design Parameters

The thermal design parameters of the RX72N Group are listed below.

Table 3.1 RX72N Group Thermal Design Parameters

Package	Mounting Board Layers	θ_{ja} [°C/W]	ψ_{jt} [°C/W]
176pin LFQFP PLQP0176KB-C	4	31.5	0.4
144pin LFQFP (PLQP0144KA-B)	4	32.6	0.5
100pin LFQFP (PLQP0100KB-B)	4	34.0	0.6
224pin LFBGA (PLBG0224GA-A)	4	23.1	0.2
176pin LFBGA (PLBG0176GA-A)	4	30.5	0.3
145pin TFLGA (PTLG0145KA-A)	4	22.9	0.2

Note 1. The above values were calculated using the measurement environment specified in the EIA/JEDEC standard. For details of the standard, refer to EIA/JEDEC Standard (LFQFP is based on JESD 51-2 and JESD 51-7, TFLGA/LFBGA are based JESD51-2 and JESD51-9).

3.3 Calculating Power Consumption (Pd)

Use the following formula to calculate the power consumption (Pd):

$$\text{Power consumption} = \text{voltage} \times \text{current} + \sum\{(\text{VOL} \times \text{IOL})\} + \sum\{(\text{VCC} - \text{VOH}) \times | - \text{IOH} |\} \quad \text{--- (1)}$$

Figure 3.1 is a configuration diagram showing the current paths. The current in Formula (1) consists of DC current and AC current, and they are calculated using the following formulas:

$$\text{DC current} = \text{leak current} + \text{analog current} \quad \text{--- (2)}$$

$$\text{AC current} = \text{logic current} + \sum \text{IO_AC current} \quad \text{--- (3)}$$

The $\sum \text{IO_AC}$ current of formula (3) is calculated from the number of and capacitance of the I/O lines (input pin capacitance*1, external load capacitance), and the pin switching frequency, using the following formula:

$$\sum \text{IO_AC current} = \sum (\text{input pin capacitance} + \text{external load capacitance}) \times \text{switching frequency} \times \text{VCC} \quad \text{--- (4)}$$

Note 1. For the input pin capacitance (Cin), refer to chapter of Electric Characteristics, in the hardware manual of the MCU.

Calculate the leak current, analog current, and logic current from the data listed in Table 3.22, Classification of RX72N Group Current Consumption. The logic current is an AC current, so multiply the unitary current (mA/MHz) by the operating frequency (MHz).

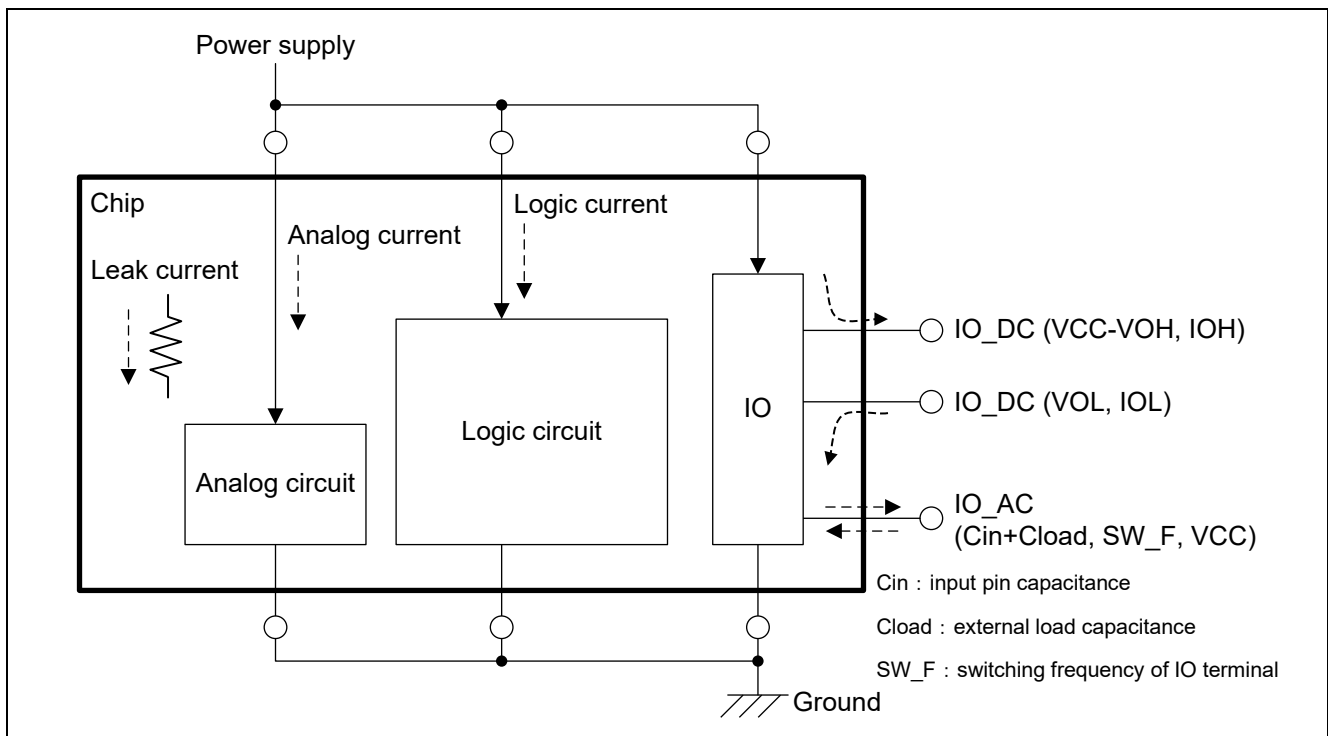


Figure 3.1 Current Path Configuration Diagram

Table 3.2 Classification of RX72N Group Current Consumption

No.	Type	Category	Subcategory	Item	Frequency [MHz]	Unitary Current [mA/MHz]*2	Max. Current [mA]*1	Remarks	
1	DC	Leak			—	—	164		
2		Analog	USBb (USB2.0 FS)		—	—	10		
3			S12ADFa (2 units, channel-specific sample and hold, temperature sensor)		—	—	3.6		
4			R12DA (2 channels, buffered output)		—	—	1.1		
5	AC	Logic	CPU	CoreMark operation	240	0.185	44.40		
6			Peripheral IP modules	DMACa, DTc		120	0.048	11.52	
7				MTU3a			0.024	2.88	For 9 channels
8				GPTW		0.021	2.52	For 4 channels	
9				ETHERC (1 channel)		0.030	3.60	Max. 2 channels	
10				EPTC		0.200	24.00		
11				PMGI (1 channel)		0.005	0.60	Max. 2 channels	
12				RSPIc (1 channel)		0.005	0.60	Max. 3 channels	
13				SCLi (1 channel)		0.005	0.60	Max. 5 channels	
14				GLCDC		0.044	5.28		
15				DRW2D		0.055	6.60		
16				EXDMACa		60	0.036	2.16	
17				Trusted Secure IP		0.250	15.00		
18				TPUa		0.018	1.08		
19				RTCd, IWDTa, WDTA		0.006	0.36		
20				CMT, CMTW, TMR (1unit each)		0.006	0.36	Max. 2 channels	
21				POE3a, POEG, PPG (1unit)		0.004	0.24		
22				USBb		0.018	1.08		
23				SCLj, SCLh (1 channel)		0.006	0.36	Max. 8 channels	
24				RIICa (1 channel)		0.004	0.24	Max. 3 channels	
25				CAN (1 channel)		0.006	0.36	Max. 3 channels	
26				QSPI		0.012	0.72		
27				SDHI		0.018	1.08		
28				MMCIF		0.012	0.72		
29				PDC		0.008	0.48		
30				S12ADFa (1 unit), TEMPS		0.008	0.48	ADC max. 2 units	
31				R12DA (2 channels)		0.020	1.20	Max. 2 channels	
32				DOC		0.004	0.24		
33				CRCA		0.005	0.30		
34				SSIE		0.006	0.36		
35				CAC		0.004	0.24		
36				ELC		0.008	0.48		

Note 1. Worst conditions (VCC=3.6V、Tj=125°C) .

Note 2. The unitary current related to AC is not dependent on the VCC value.

4. Derating Examples for Typical High-Temperature Applications

Table 4.1 lists high-temperature profiles for high-temperature applications assumed to be typical for RX72N Group MCUs as well as recommended high-temperature profiles for derating. This recommendation profiles are estimated from Renesas quality test results.

For product numbers of specific target MCUs, refer to Table 4.2 Target Product Numbers (RX72N Group).

In the derating examples 10 years of operation is assumed, except for example 5.

Choose the example that best approximates your usage conditions. If none of the examples provided is applicable, please contact Renesas individually.

Table 4.1 Typical High-Temperature Applications

Example	Application	Anticipated High-Temperature Profile	Recommended High-Temperature Profile for Derating
1	Cooking devices (cooktops, IH cookers, etc.)	Operating time in high-temperature environment of 3 hours/day In standby or stopped state at other times	$-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$, 3 hours/day. In standby or stopped state at $-40^{\circ}\text{C} \leq T_j \leq 90^{\circ}\text{C}$ at other times
2	Household appliance motors, power tools, etc.	Operating time in high-temperature environment of 6 hours/day In standby or stopped state at other times	$115^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$, 3 hours/day. $-40^{\circ}\text{C} \leq T_j \leq 115^{\circ}\text{C}$, 3 hours/day In standby or stopped state at $-40^{\circ}\text{C} \leq T_j \leq 90^{\circ}\text{C}$ at other times
3	EV chargers, etc.	Operating time in high-temperature environment of 8 hours/day In standby or stopped state at other times	$115^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$, 4 hours/day. $-40^{\circ}\text{C} \leq T_j \leq 115^{\circ}\text{C}$, 4 hours/day In standby or stopped state at $-40^{\circ}\text{C} \leq T_j \leq 85^{\circ}\text{C}$ at other times
4	Smart meters, power controllers, etc., equipment installed out of doors, etc. (24-hour operation)	Operating time in high-temperature environment of 8 hours/day Also operating at other times	$115^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$, 4 hours/day. $-40^{\circ}\text{C} \leq T_j \leq 115^{\circ}\text{C}$, 4 hours/day $-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$ at other times
5	PC server power supplies, etc. (24-hour operation)	In continuous use for 5 years in environment that includes high temperatures	$115^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$, 15,000 hours $-40^{\circ}\text{C} \leq T_j \leq 115^{\circ}\text{C}$, 30,000 hours In continuous use for 5 years
6	Industrial motors (24-hour operation: example 1)	In continuous use in high-temperature environment	$82^{\circ}\text{C} < T_j \leq 112^{\circ}\text{C}$, 80% $-40^{\circ}\text{C} \leq T_j \leq 102^{\circ}\text{C}$, 20%
7	Industrial motors (24-hour operation: example 2)	In continuous use in environment that includes very high temperatures	$90^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$, 5% $85^{\circ}\text{C} < T_j \leq 110^{\circ}\text{C}$, 75% $-40^{\circ}\text{C} \leq T_j \leq 105^{\circ}\text{C}$, 20%
8	Industrial motors (24-hour operation: example 3)	In continuous use in high-temperature environment	$T_j \leq 110^{\circ}\text{C}$, 100%

Note: The ambient temperature (T_a) should be between -40°C and 105°C .

Table 4.2 Target Product Numbers (RX72N Group)

Target Product Numbers	Package
R5F572NNDGFC	LFQFP176
R5F572NNHGFC	
R5F572NDDGFC	
R5F572NDHGFC	
R5F572NNDGFB	LFQFP144
R5F572NNHGFB	
R5F572NDDGFB	
R5F572NDHGFB	
R5F572NNDGFP	LFQFP100
R5F572NNHGFP	
R5F572NDDGFP	
R5F572NDHGFP	
R5F572NNDGBD	LFBGA224
R5F572NNHGBD	
R5F572NDDGBD	
R5F572NDHGBD	
R5F572NNDGBG	LFBGA176
R5F572NNHGGBG	
R5F572NDDGBG	
R5F572NDHGGBG	
R5F572NNDGLK	TFLGA145
R5F572NNHGLK	
R5F572NDDGLK	
R5F572NDHGLK	

5. Reference Document

Semiconductor Reliability Handbook Rev. 2.50 (R51ZZ0001EJ0250) January 2017

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2019.06.19		First edition issued.
2.00	2020.10.06	6,10 9	Added LFBGA224,LFBGA176,TFLGA145 Added example 8 of high-temperature profiles
3.00	2024.01.19	3 8	Updated URL of referenced site Corrected values in Table3.2

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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