

Summary

This application note describes the overview of RZ/V2MA Evaluation Board Kit (made by Shimafuji Electric Inc.).

Please refer to the hardware manual of RZ/V2MA Evaluation Board Kit for details.

Target Device

RZ/V2MA Evaluation Board Kit

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1. Overview

This board is an evaluation kit for the Arm[®]-based RZ/V2MA MPU from Renesas Electronics (RZ/V2MA evaluation board kit, hereafter V2MAEVK). This manual describes the overview of the V2MAEVK.

The V2MAEVK consists of the RZ/V2MA CPU_MODULE (main), RZ/V2MA Base Board (base), and RZ/V2MA Option Board (option) *¹.

Board Name	Overview
RZ/V2MA CPU_MODULE (main)	<ul style="list-style-type: none"> The RZ/V2MA is mounted. Board on which the main functional components for the RZ/V2MA are mounted
RZ/V2MA Base Board (base)	<ul style="list-style-type: none"> Connected to CN301 and CN302 on the RZ/V2MA CPU_MODULE or RZ/V2MA Option Board Board for the generation and supply of power
RZ/V2MA Option Board (option) * ¹	<ul style="list-style-type: none"> Connected to CN503 and CN504 on the RZ/V2MA Base Board Connected to CN501 and CN502 on the RZ/V2MA CPU_MODULE Board on which the PCI express connector is mounted (optional) *¹

Note 1. RZ/V2MA Option Board (option) is an optional board provided by Shimafuji Electric Inc.

The following documents have been prepared for this V2MAEVK. Make sure to refer to the latest versions of these documents.

Document Type	Document Title	Document No.	Description
Hardware Manual	RZ/V2MA Evaluation Board Kit Hardware Manual	Provided by Shimafuji Electric Incorporated	Hardware specifications of the V2MAEVK
Start-up guide	RZ/V2MA Evaluation Board Kit Start-Up Guide	R01UH6587EJ0100	The startup procedure of the first boot loader, second boot loader, and U-Boot on the RZ/V2MA Evaluation Board Kit

1.1 Features

This V2MAEVK includes the following features.

- LPDDR4: 32 Gbits
- eMMC™: 16 GB
- Gigabit Ethernet interface connector: 1 ch
- USB3.1 Gen1 Type-C: 1 ch
- Micro SD card connector: 1 ch
- Pmod™ interface connector: 2 ch
- Debug serial interface micro USB Type-B: 1 ch
- PCI Express® x4 Slot 2lane (optional): 1 ch

1.2 Block Configuration

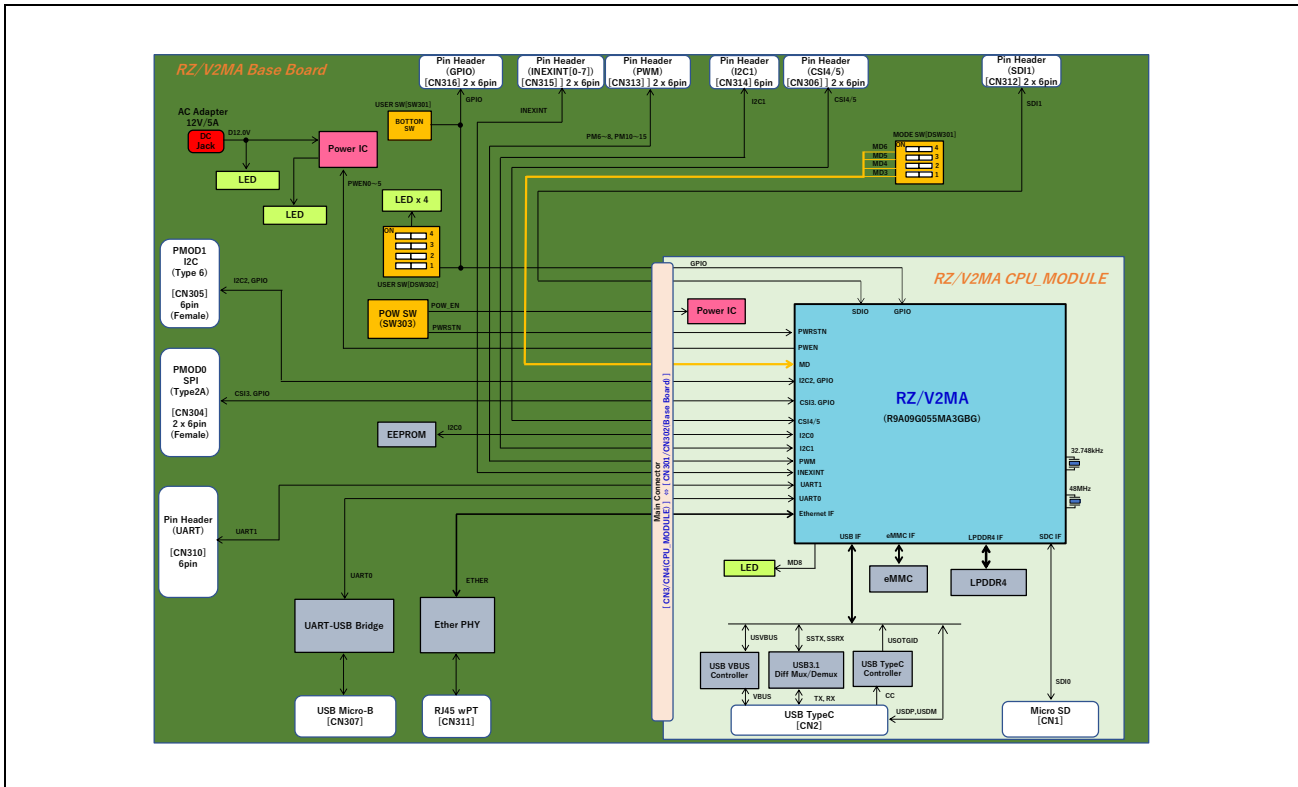


Figure 1.2-1 V2MAEVK Block Diagram

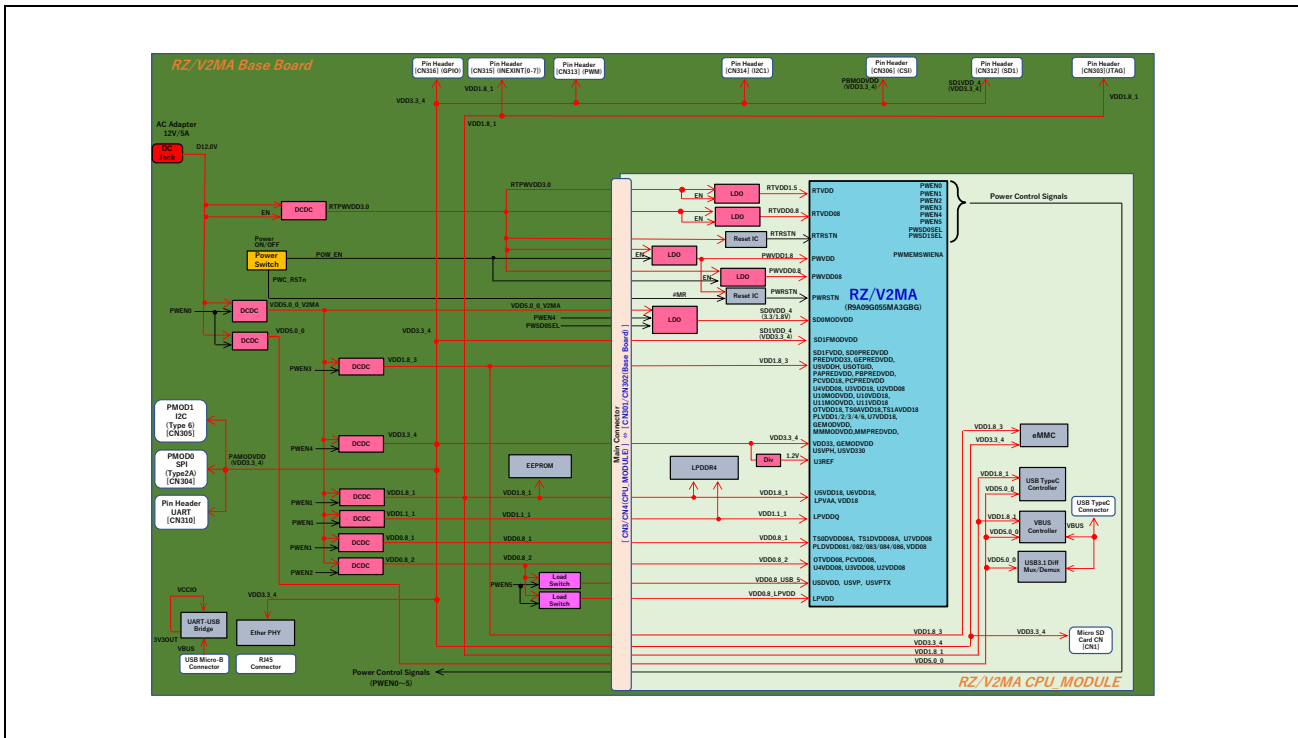


Figure 1.2-2 V2MAEVK Power Supply Block Diagram

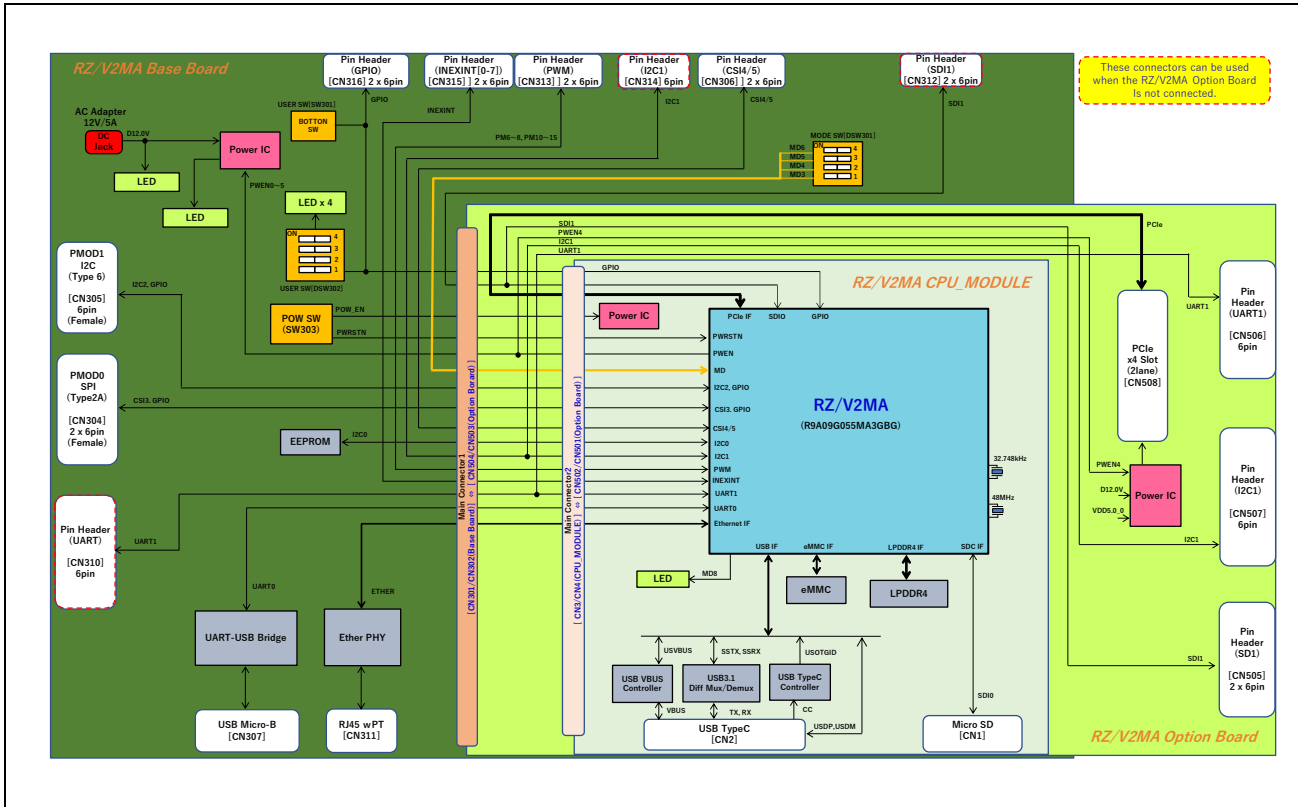


Figure 1.2-3 V2MAEVK Block Diagram (with the Option Board)

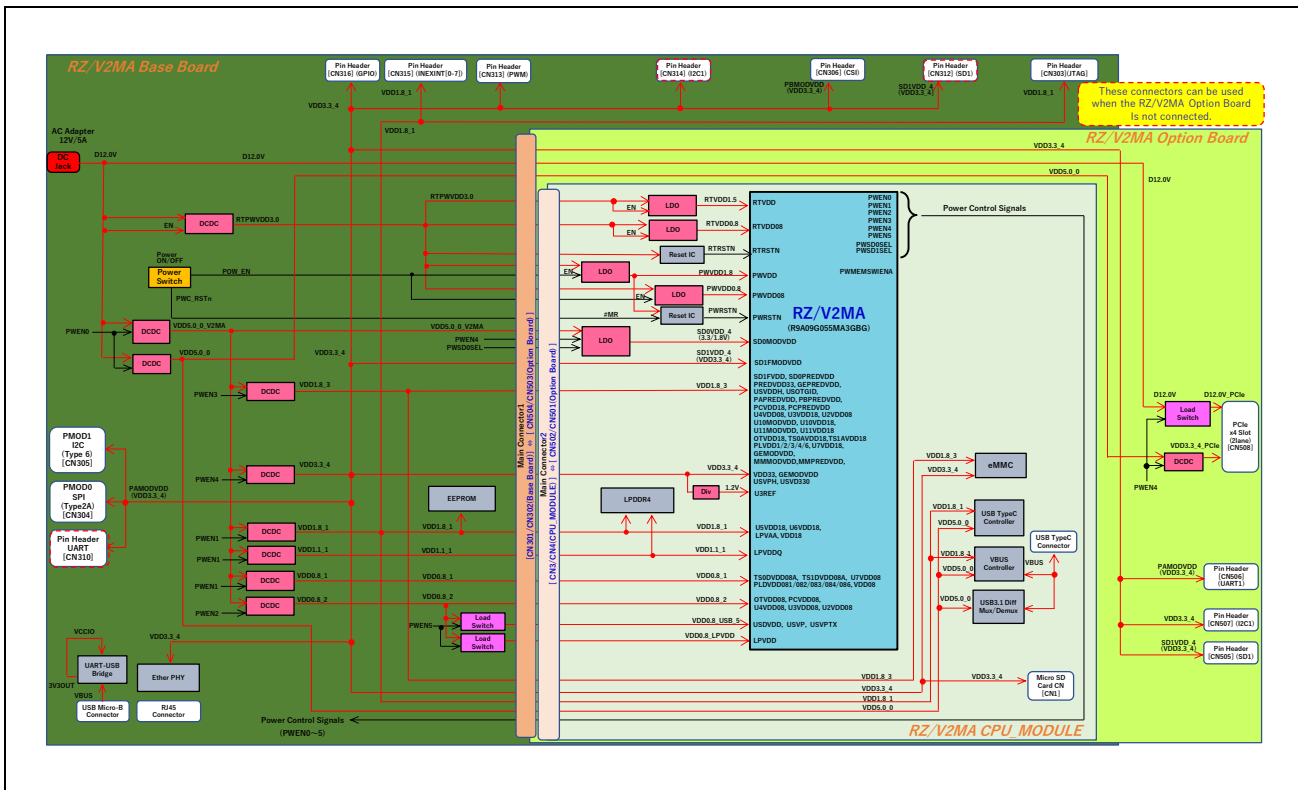


Figure 1.2-4 V2MAEVK Power Supply Block Diagram (with the Option Board)

1.3 Specifications

1.3.1 V2MAEVK Specifications

Table 1.3-1 V2MAEVK Specifications

Item	Specification
MPU	R9A09G055MA3GBG (RZ/V2MA)
Board size	CPU_MODULE: 60 × 55 × 1.6 mm Base Board: 113 × 80 × 1.6 mm Option Board: 90 × 60 × 2.0 mm
LPDDR4	Micron MT53D1024M32D4 32 Gb Dual-Rank
eMMC	Kioxia THGBMJG7C1LBAIL 16 GB
USB	Connector: Type-C
Ethernet	Connector: RJ45 Ethernet PHY IC: RTL8211FG-CG
SD Card I/F	Connector: Micro SD
SDIO I/F	Connector (Pin Header):12 pins with 2.54-mm pitch
Debug I/F	Connector: USB Micro-B UART-USB bridge: FT230XS
CSI I/F	Connector (Pin Header):12 (2 x 6) pins with 2.54-mm pitch
Pmod0 SPI (Type2A) I/F	Connector: 12 (2 x 6) pins with 2.54-mm pitch (Female)
GPIO I/F	Connector (Pin Header):12 (2 x 6) pins with 2.54-mm pitch
PWM I/F	Connector (Pin Header):12 (2 x 6) pins with 2.54-mm pitch
I2C I/F	Connector (Pin Header):6 pins with 2.54-mm pitch
Pmod1 I2C (Type6) I/F	Connector :6 pins with 2.54-mm pitch (Female)
UART I/F	Connector (Pin Header):6 pins with 2.54-mm pitch
Interrupt Connector	Connector (Pin Header):12 (2 x 6) pins with 2.54-mm pitch
LED	For power supply (D12.0): Green (base) For power supply (VDD5.0_0_V2MA): Green (base) For boot (MD8): Green (main) For GPIO check : Green (base) ×4
Switch	For mode setting: DIP ×1 (base) User switch: DIP × 1 (base) For power supply: Slide ×1 (base) User switch: Push ×1 (base)
Power supply	AC adapter: 12V/5A DC plug diameter (inside): 2.1 mm DC plug diameter (outside): 5.5 mm

Table 1.3-2 V2MAEVK Option Board (option)*1 Specification

Item	Specification
PCIe I/F	x4 Slot: 2 lane
SDIO I/F	Connector (Pin Header): 12 (2 x 6) pins with 2.54-mm pitch
UART I/F	Connector (Pin Header): 6 pins with 2.54-mm pitch
I2C I/F	Connector (Pin Header): 6 pins with 2.54-mm pitch

Note 1. RZ/V2MA Option Board (option) is an optional board provided by Shimafuji Electric Inc.

1.3.2 Outer Appearance

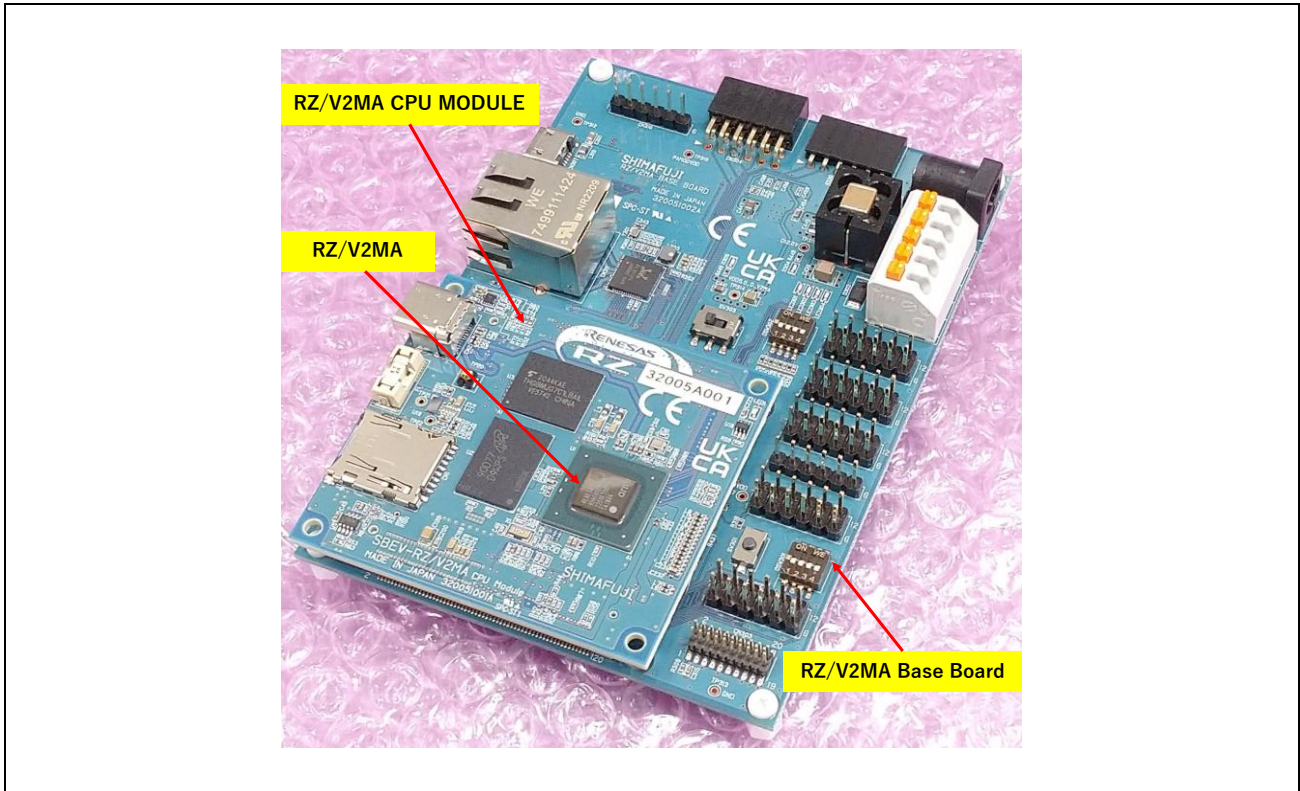


Figure 1.3-1 Outer Appearance of V2MAEVK

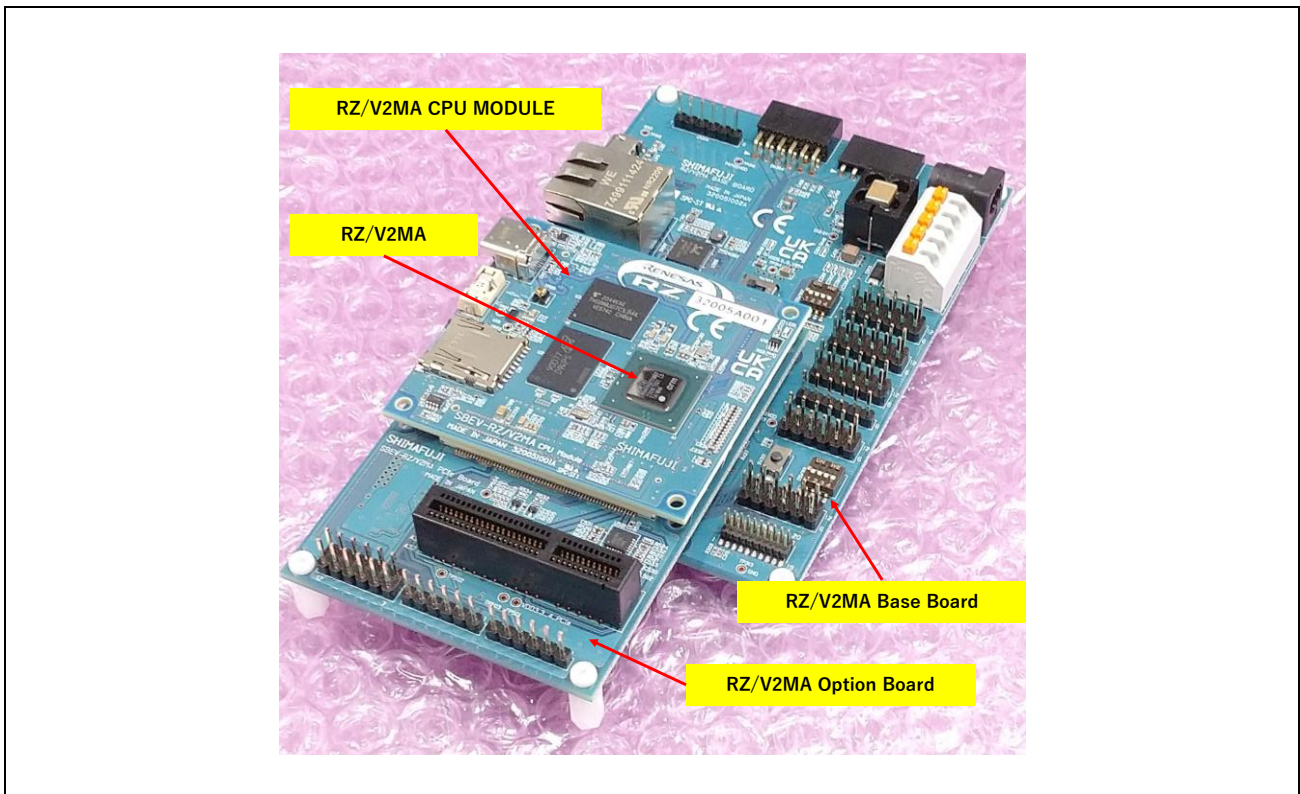


Figure 1.3-2 Outer Appearance of V2MAEVK(with the Option Board)

REVISION HISTORY	RZ/V2MA Evaluation Board Kit Booklet
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Rev.	Date	Description	
		Page	Summary
1.00	Aug 10, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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