Thermal FET

Usage guide

Introduction

This application note explains the characteristics and basic usage of thermal FETs.

Contents

1. Overview of Thermal FET

1.1 Development background

In recent years, high power switches for automobiles have changed from mechanical relays to semiconductors to ensure high functionality and high reliability of the system. Computerization is accelerating to the used switch. Power MOSFETs are commonly used as semiconductor switches, but further to achieve high reliability, protection functions such as "over-temperature protection", "over-current protection", and "over-voltage protection" are required for power devices alone. The need for embedded intelligent power devices is increasing. However, intelligent power devices that make full use of IC technology are often customized for automotive applications. As a result of less versatility, it is often more expensive. Therefore, Renesas has developed a power MOSFET "Thermal FET" with a built-in "overheat cut-off circuit" which is the minimum necessary function for the purpose of device and system protection.

This product will be an intelligent power device with high versatility and low cost. The thermal MOSFET is explained below.

1.2 Features

1. Built-in over temperature shut-down circuit.
2. It has the same basic structure as a power MOS FET and provides low on-resistance.
3. It consists of three pins, which are most commonly use in power MOSFETs, and the packages use is also apply common technology.
4. Reliability in an automotive operating environment is at the same level as a power MOSFET.

1.3 Advantages of Thermal FET

1. Ensures high fracture resistance
   It has sufficient ability to withstand load short circuits, load dumps, and electrostatic surges that are unique to automobiles. Especially it has a load short-circuit resistance that can be used up to 24V vehicles (excluding some products).

2. Supports low current consumption
   With the computerization and high functionality of systems, it has become essential to reduce the burden on batteries. Especially, it is essential to reduce dark current (current that flows regardless of whether it is on or off), and thermal FETs achieve low current consumption. (Items are listed in IDSS, etc., but may not be listed in other companies' catalogs.) For LED (Light Emitting Diode), if it is not 10uA ↓, it will light up slightly when it is not lit, which will be a problem in use. The thermal FET has a power consumption of 1uA and low current consumption, so it can be used for loads that require low current.

3. How to check overheat cutoff operation of thermal FET
   Generally, there is a detection method that uses the A/D detection function of the microcomputer. However, the A/D detection method requires an external shunt resistor, and there is a limit to the number of A/D pins required on the MCU side. (Because it is used as a judgment of another function that is originally necessary) Therefore, when dealing with the same method, our company uses the I/O port of the microcomputer with a margin, monitors the gate voltage of the thermal FET and the voltage between the drain and the source and confirms the synchronous state. This is recommended because it is possible to check whether or not the overheat cutoff operation is performed.

1.4 Main function

1. It detects the rise of the channel temperature in the chip and shuts off the power MOSFET by itself. ⇒ "Built-in over-temperature cut-off circuit“ With this operation, the Power MOSFET is protected from thermal damage due to overpower such as load short circuit.

2. Two specifications are available for returning to the normal state after the operation of the over-temperature cut-off circuit.

   1) Latch Type
   Holds the state of the overheat cutoff operation. (when applying gate voltage continuously). By setting the gate voltage to 0V, the holding state of the overheat cutoff circuit is reset (cancelled), and operation becomes possible by applying the normal bias thereafter.

   2) Temperature Hysteresis Type
   After the overheat shutdown operation, when the channel temperature in the chip drops below a certain temperature, the holding state of the overheat shutdown circuit is reset (released), and normal bias application enables operation. Temperature for overheat shutdown operation (Thermal Shutdown Function). When the channel temperature inside the chip reaches 175ºC (typ.), the overheat shutdown operation occurs and turns off the power MOSFET.

1.5 Precautions for use

1. Please treat the overheat cutoff circuit as a "protection function" against thermal destruction in abnormal power conditions, and do not design a system that actively uses it in expectation of its function.

2. The operating area of the thermal shutdown circuit is limited for each product. Please be sure to check the "safety assurance operation diagram" described in the data sheet and confirm compatibility with the operating conditions in the system. (Especially when the voltage applied to the drain of a battery, etc., exceeds 16V, it is necessary to thoroughly check the usable range.)

3. For normal condition usage, please use the product within the guaranteed range for the "maximum rating", "operating power supply range", "mounting conditions", and others.This product is intended to replace mechanical relays, and its switching time is designed to be slow. Therefore, please note that it is not suitable for controlling loads that require high-speed switching operation. The customer is responsible for verifying the operation speed, so please give us a sufficient evaluation.

2. Thermal FET Configuration and Operation Overview

2.1 Internal Equivalent circuit

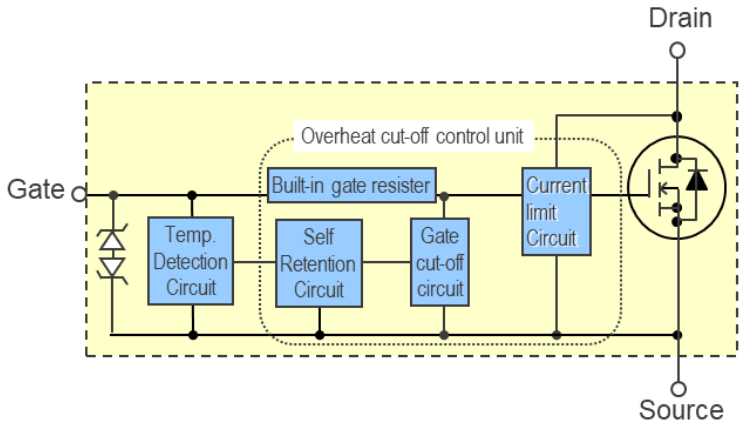


Fig. 2-1 Internal equivalent circuit description of components

1. Temperature detection(sensing) circuit
   Constructed with diode element and circuitry to detect channel temperature inside the chip. This circuit is placed next to the source electrode and in the center of the chip to accurately detect the channel temperature.
2. Self-retention (Latch) circuit
   A circuit to keep the overheat cutoff state.
3. Gate cut-off circuit
   By turning on the overheat cut-off MOSFET, the impedance between the gate and source is lowered, the main MOSFET is turned off, and the drain current is cut.
4. Current limitation circuit
   It operates when the drain current exceeds the rated current.
5. Built in resistance (gate resistance R_g)

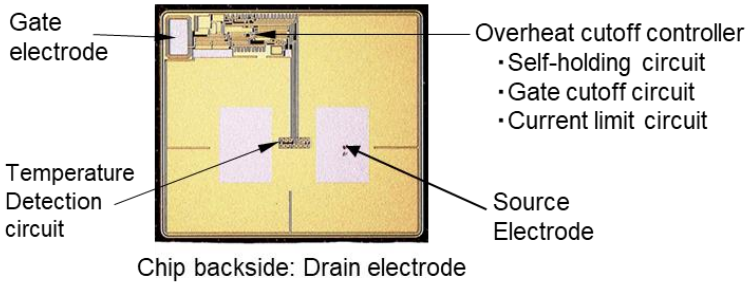


Fig. 2-2 Chip appearance photo (example)

2.2 Mechanism of Overheat shutdown operation (Thermal Shutdown Function)

This section explains on process logic operation of thermal FET overheat shutdown until it recovered by using operation waveform and equivalent circuit.

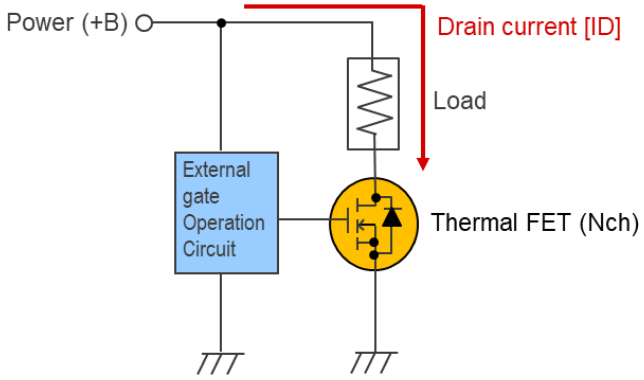


Fig. 2-3 Thermal FET use circuitry example

Operation Mode (1) : Normal Operation (Operation waveform area ①)

A gate voltage is applied and a drain current flows.

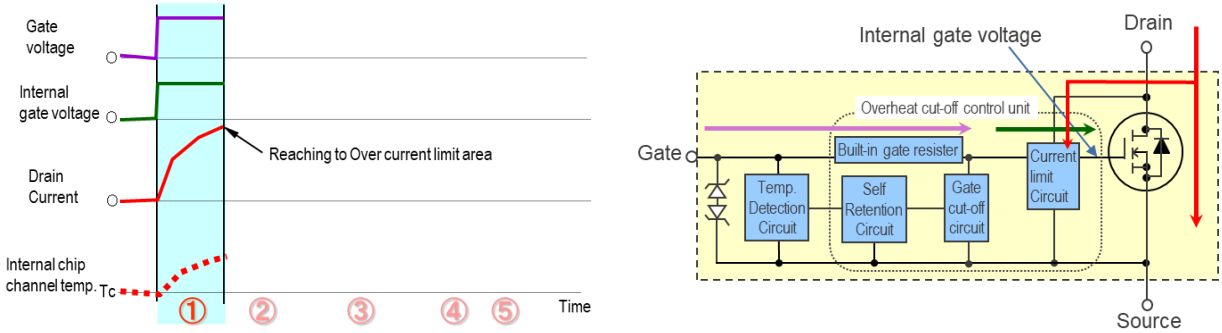


Fig. 2-4 Operation mode (1)

Operation Mode (2) : Current Limit Operation (Operation waveform area ②)

When over current and current limit circuit is judged, internal gate voltage is limited and drain current is lowered.

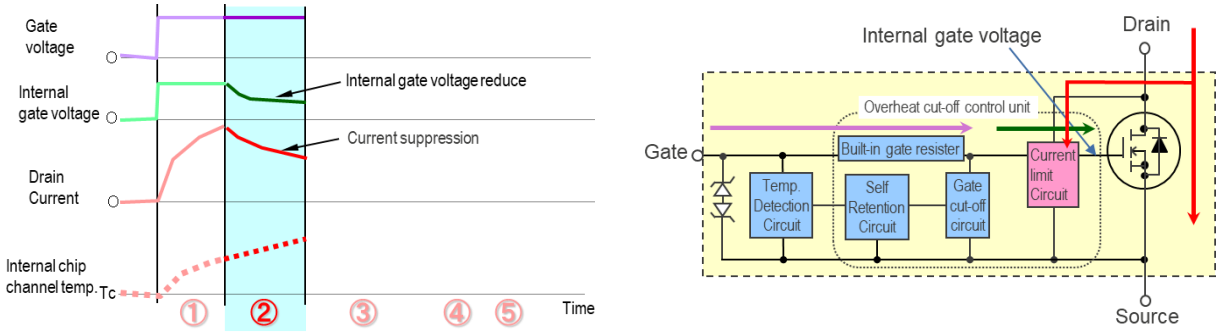


Fig. 2-5 Operation mode (2)

Operation Mode (3) : Overheat Shutdown Operation (Operation waveform area ③)

Even there is a current is limiter, when chip internal channel temperature rises and reaches the cut-off temperature, gate cut-off circuit will function to cuts off.

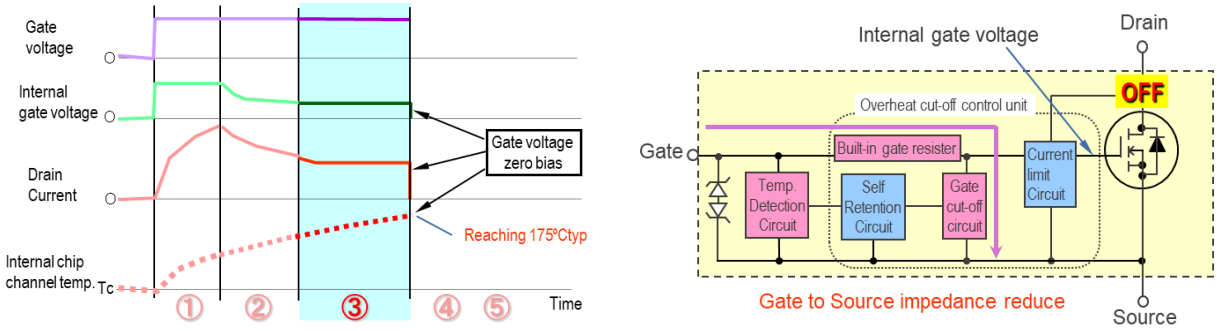


Fig. 2-6 Operation mode (3)

Operation Mode (4) : Self-retention Operation (Operation waveform area ④)

If the gate voltage is continuously applied form the outside after the overheat is cut-off, the Thermal FET will self-hold the OFF state.

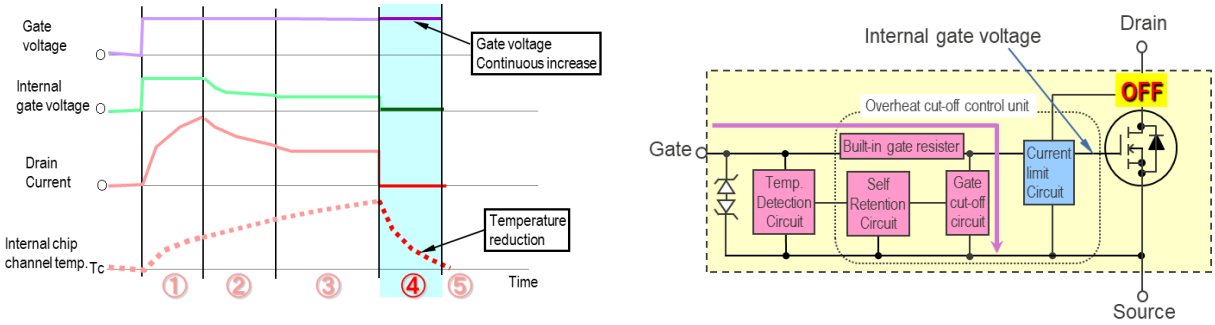


Fig. 2-7 Operation mode (4)

Operation Mode (5-1) : Release of Self-retention Operation(latch release) (Operating waveform area ⑤)

After overheat shutting down, the gate voltage is set to zero bias from the outside, and the system returns to normal control state.

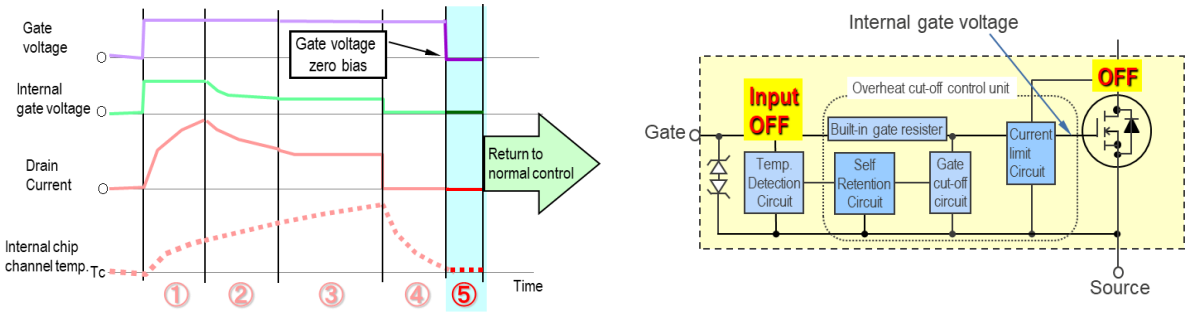


Fig. 2-8 Operation mode (5-1)

Operation Mode (5-2) : Release of Self-retention Operation(latch release) (Operating waveform area ⑤)

After overheat shutting down, the chip internal channel temperature drops to a certain constant temperature level, self-retention is released, and the system returns to normal control state.

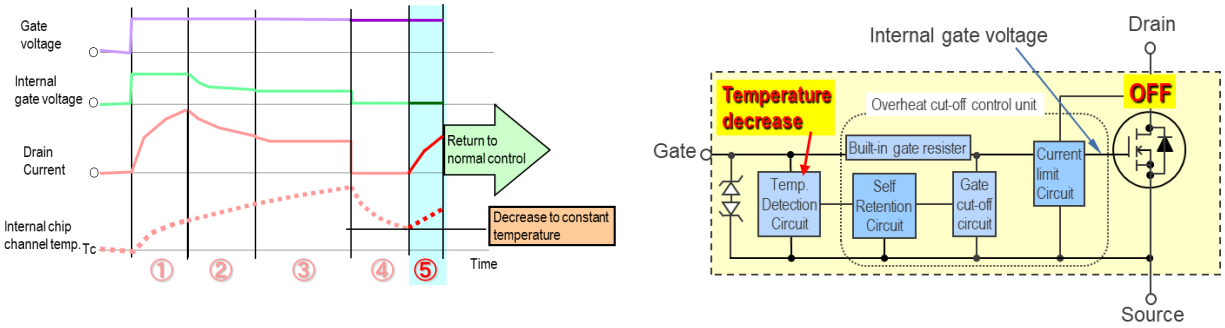


Fig. 2-9 Operation mode (5-2)

3. Thermal FET Datasheet Explanation

As mentioned above, the thermal FET is a power MOSFET with a built-in protection function. For this reason, there are “unique” expressions in the datasheets provided for each product. In addition, for the ratings and characteristics items which are not "unique" expressions, it is conformed to be the same content as power MOSFET datasheet.

3.1 Typical operating characteristics （RJF0618JPE）

Table 3-1 Typical operating characteristics (RJF0618FJPE)

(Ta = 25℃)

item	Symbol	Specification			unit	Measurement condition	Commentary
		Min.	Typ..	Max.			
Input voltage	V_{IH}	3.5	-	-	V		Minimum voltage to operate the breaking circuit
Input voltage	V_{IL}	-	-	1.2	V		Maximum voltage for release self-retention operation
Input current (When gate is not cut off)	I_{IH1}	-	-	100	μA	V_i = 8V, V_{DS} = 0	When the gate bias is applied, maximum dark current consumed at the cutoff control circuit (Same meaning as IGSS)
Input current (When gate is not cut off)	I_{IH2}	-	-	50	μA	V_i = 8V, V_{DS} = 0	
Input current (When gate is not cut off)	I_{IL}	-	-	1	μA	V_i = 8V, V_{DS} = 0	
Input current (When gate is cut off)	$I_{IH(sd)1}$	-	0.8	-	mA	V_i = 8V, V_{DS} = 0	Gate current consumed during cutoff circuit operation. Gate current during normal operation is 100uA Vi=8V, Since the current increases to 0.8mA for the breaking operation. Please secure the capacity of the drive circuit.
Input current (When gate is cut off)	$I_{IH(sd)2}$	-	0.35	-	mA	V_i = 8V, V_{DS} = 0	
Cut-off temperature	Tsd	-	175	-	℃	Channel Temperature	Cut-off operating temperature
Gate operation voltage	Vop	3.5	-	12	V		Cut-off circuit operating voltage[Note1]
Drain current (Current limit value)	$I_{D\ limit}$	40	-	-	A	V_{GS} = 5V, V_{DS} = 10V [Note2]	Current limit value

Note1: Cut-off operation cannot be expected at 12V or higher.

Note2: pulse measurement

3.2 Electrical characteristics (RJF0618JPE)

Table 3-2 Electrical characteristics (RJF0618FJPE)

Item	Symbol	Specification			unit	Measurement	item
		Min.	Typ..	Max.			
Drain current	I_{D1}	-	-	67	A	V_{GS} = 3.5V, V_{DS} = 10V Notes1	At the minimum gate voltage that activates the cut-off circuit maximum drain current
	I_{D2}	-	-	1.2	mA	V_{GS} = 1.2V, V_{DS} = 10V	Maximum drain current at shutdown circuit off voltage
	I_{D3}	40	-	-	A	V_{GS} = 5V, V_{DS} = 10V Notes1	Current limit value
Gate-source breakdown voltage	$V_{(BR)GSS}$	16	-	-	V	I_G = 800 μ A, V_{DS} = 0	For considering direct drive of the automobile power supply, positive voltage side can be input up to 16V. For negative voltage side is -2.5V due to the restrictions of the protection circuit
		-2.5	-	-		I_G = -100 μ A, V_{DS} = 0	
turn-on delay time	$t_{d(on)}$	-	0.8	-	μs	V_{GS} = 10V I_D = 20A R_L = 1.5 Ω	Switching speed is limited by built-in gate series resistor
Rise time	t_r	-	0.35	-			
turn-off delay time	$t_{d(off)}$	-	175	-			
Fall time	t_f	-	12.5	12			
Load short-circuit Cut off operation time	tos	-	0.48	-	ms	V_{GS} = 5V, VDD = 16V	Time for completion form load short circuit occurs until overheat cut-off operation completion. The load short-circuit breaking operation time varies depending on the usage environment, usage conditions, etc.
			0.31			V_{GS} = 5V, VDD = 24V	

Notes 1: pulse measurement.

Notes 2: The parasitic capacitance (C_{iss}//C_{rss}) of thermal FET cannot be quantified and expressed individually due to the built-in control circuit between the gate and source.

3.3 How to View the Safe Operating Area of a Thermal FET

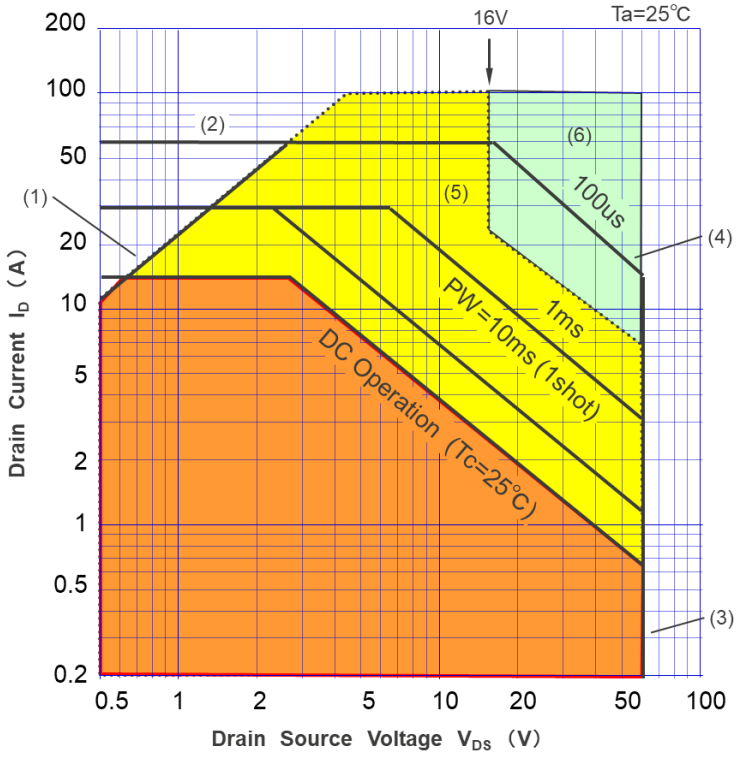


Fig. 3-1 Safe operating area with Thermal FET (SOA diagram)

（1） Area is limited by ON resistance.
（2） Area is limited by drain current rating “I_D”.
（3） Area is limited by drain voltage rating “V_{DSS}”.
（4） Area is the area limited by the safe operating area of the body MOSFET.
For product design under normal conditions, please use within the limits of (1) to (4) region.

（5） If this range is exceeded, an overheat shutdown operation will occur. (Yellow color area) Therefore, regarding the heat shutdown area, the yellow and orange areas are areas where overheat shutdown protection is possible.(In addition, the overheat cutoff mode that occurs in the orange area can be considered that when the channel temperature in the chip reaches 150°C or more due to factors such as "increase in ambient temperature" or "improper heat dissipation.")

（6） The green area (6) is a high voltage and high current area. When a load short circuit occurs, the power becomes high. Because of this, control circuit response from temperature detection until shutdown operation of Thermal FET not able to match and the internal power MOSFET will lead to power (thermal) destruction. Please be careful when using this product in a system with a battery voltage of 16V or higher.

3.4 Relationship between overheat shutdown operation and gate/drain input voltage in Thermal FET

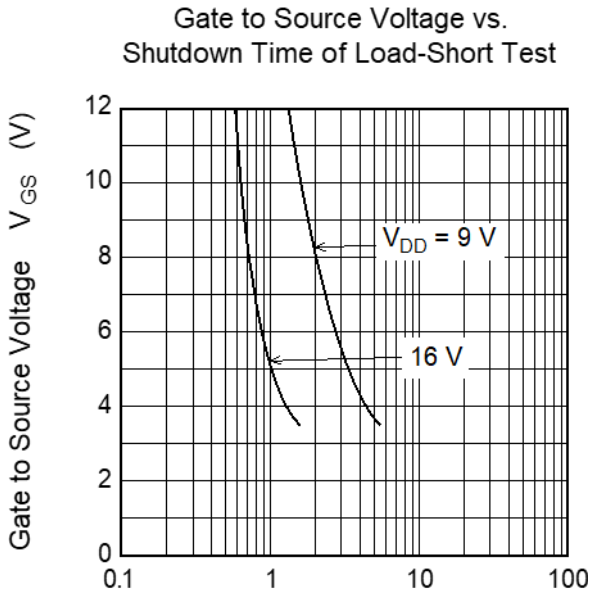


Fig. 3-2 Shutdown Time of Load-Short Test

1) Change in overheat shutdown operation time
The overheat cutoff operation of the thermal FET has the characteristic that the cutoff time changes depending on the applied gate voltage and drain voltage. Since the characteristics are determined individually according to the specifications of each product, please confirm it characteristic as describe in right side diagram in each product datasheet. Please take this into consideration when designing your system. The reason for such a change in the overheat cutoff time is When a load short circuit occurs, the amount of drain current that flows in depends on the characteristics of the thermal FET itself, the gate voltage, and the drain voltage. Therefore, the time it takes for the channel temperature in the chip to reach the temperature at which the cutoff operation occurs It is for change.

2) Change in overheat shutdown temperature (typ. value)
The overheat cutoff temperature (typ. value) of the thermal FET does not vary greatly with the gate voltage being driven and it has almost constant characteristics.

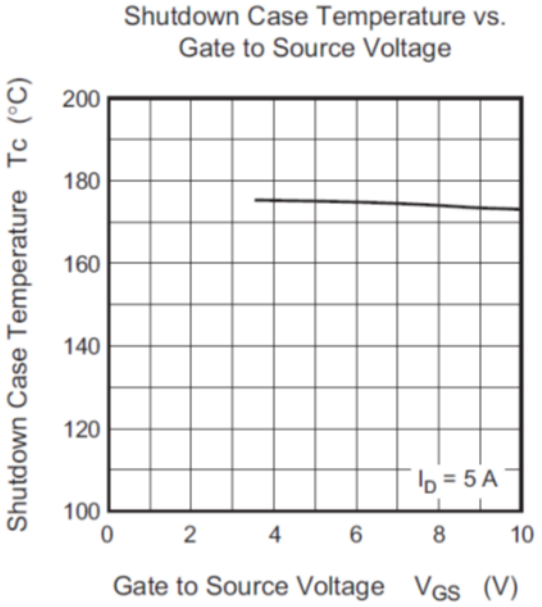


Fig. 3-3 Shutdown case temperature dependence

4. Important Notes About Thermal FET Control

4.1 Gate drive method

The guideline for the internal current consumption of the thermal FET is as below:

①Gate current consumed during normal operation (gate charge current and gate leakage current to MOSFET)
— $I_{G1} \geqq 100uA$ （V_{GS}=3.5V, full temperature range）

②Gate current consumed during overheat shutdown operation
— $I_{G2} \geqq 0.7mA$ （The main current is determined by the internal resistance Rg, full temperature range at 3.5V）

Therefore, ①+② ($I_{G1}+I_{G2} \geqq 0.8mA$) is consumed during the cut-off operation. Considering this current consumption, at the gate voltage please design a drive that can secure $V_{GS} \geq 3.5V$, which is the minimum operating voltage for the cut-off circuit. In addition, when the gate sink current becomes less than the specified current, the overheat cut-off operation cannot be maintained since the internal gate voltage is divided by the influence of the internal resistance and the self-retention mode (latch situation) is reset (released). It will return to normal operation, please be careful.

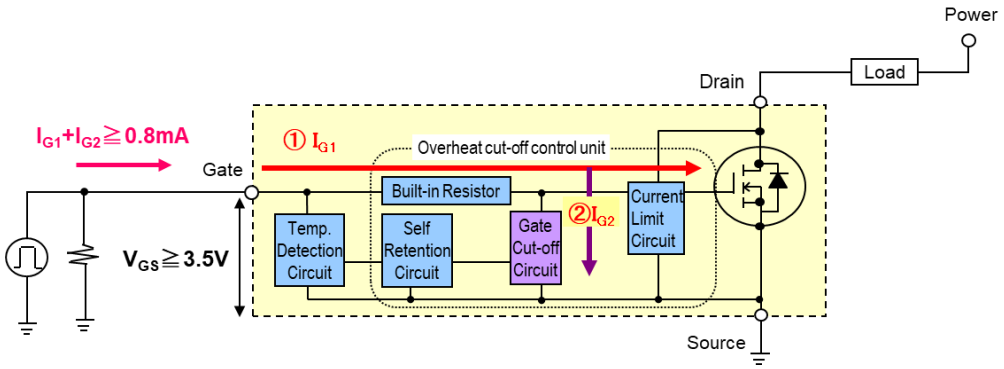


Fig. 4-1 Internal equivalent circuit diagram

4.2 Concept of external gate resistor

1. Nch Type

As shown in section 4.1, the gate current required for overheat cutoff operation is $I_{G1} + I_{G2} \geq 0.8mA$.When inserting an external resistor, please consider this gate current and design an external resistor that can secure the cut-off operating voltage $V_{GS} \geqq 3.5V$.

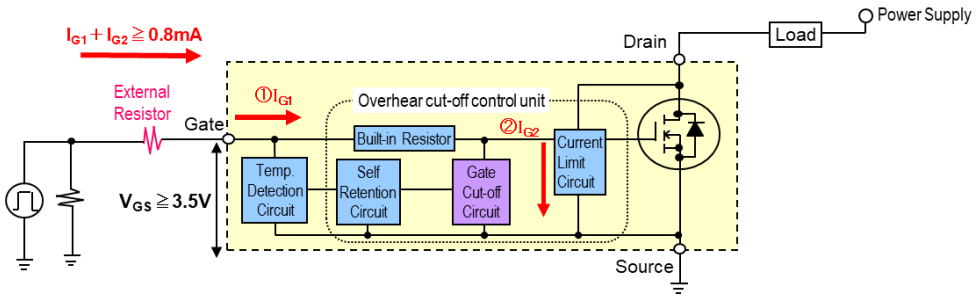


Fig. 4-2 Internal equivalent circuit diagram (Nch type)

2. Pch Type

When inserting an external resistor as voltage divider,

① Cut-off operating voltage $V_{GS} \geq 3.5V$ is required.

② A gate current of $I_{G1} + I_{G2} \geq 0.8mA$) is required for overheat cut-off operation.

③ Therefore, from VDD=Va+Vb, please set the resistance value considering the required gate current ($I_{G1}+I_{G2} \geqq 0.8mA$).

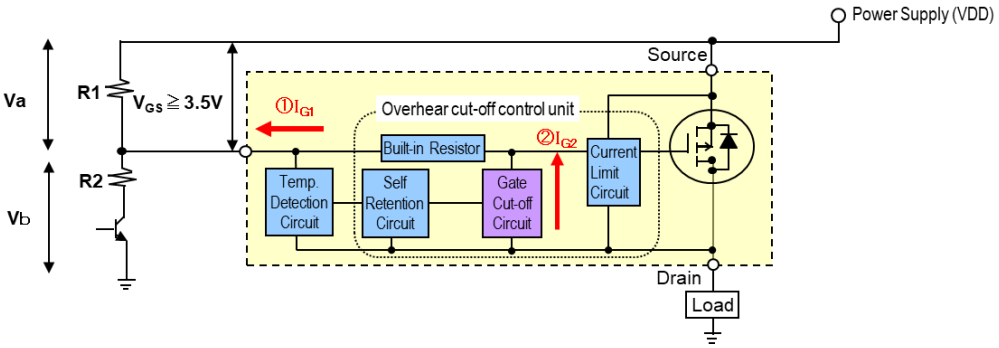


Fig. 4-3 Internal equivalent circuit diagram (Pch type)

4.3 Precautions for inductance load control

Notes (1)

The thermal FET has resistance to avalanche operation like the power MOSFET. However, the avalanche operation originally occurs when the gate is turn off. It is an operation that absorbs (extinguishes) the back electromotive force of the inductance load using the drain withstand voltage of the product. The device that absorbs this avalanche energy causes a temperature rise in the chip, but overheating shutdown operation cannot be performed against this temperature rise. As mentioned above, the overheat cutoff operation of the thermal FET is based on assumption that the gate voltage is supplied within the specified range. There is no protection against events that occur in the gate voltage off state.

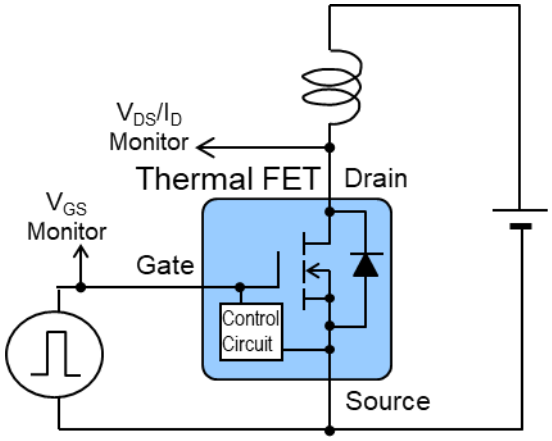


Fig. 4-4 Basic circuit example for inductance load control

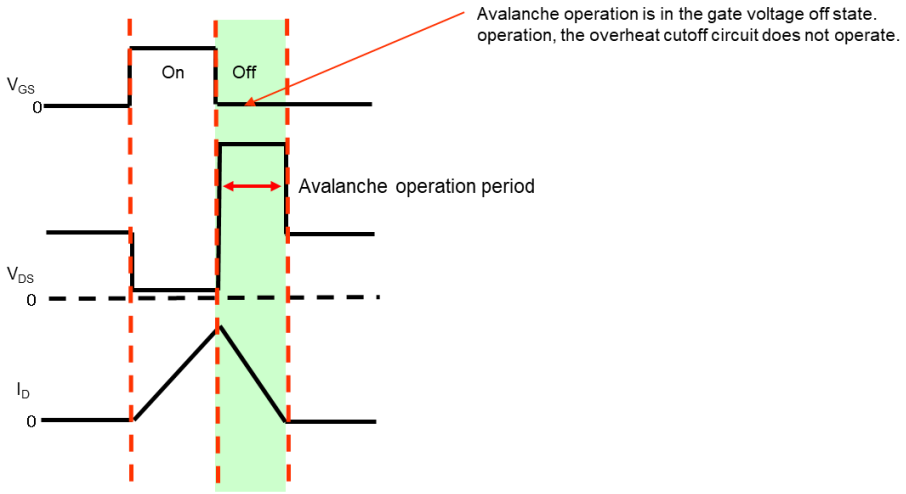


Fig. 4-5 Waveform during avalanche operation with inductive load

Notes (2)

When using Nch Thermal FET as high side switch for inductance load control, same as power MOSFET the gate is turned on at an extremely low voltage. Back electromotive force is absorbed (extinguished) by using the operation in the non-saturation operation area of the power MOSFET. However, for the temperature rise inside the chip that occurs due to back electromotive force absorption, the gate voltage has not reached the specified range, so the overheat shutdown operation cannot be performed. The principle that the Thermal FET uses the non-saturation operating region in this operation is that when the Nch Thermal FET turns off, the potential of the source terminal drops, and a voltage difference occurs between the gate and source. The potential difference is a very low voltage, but when it exceeds the $V_{GS(off)}$ voltage, the Nch Thermal FET turns on and starts absorbing back electromotive force. (Since the absorption starts, the gate voltage remains low and stabilizes.) Therefore, only a low gate voltage that slightly exceeds the $V_{GS(off)}$ voltage is generated at the gate, so overheat shutdown operation is not possible. This Drain to Source Voltage (V_{DS}) ON time is becoming VDD +voltage difference of gate to source.

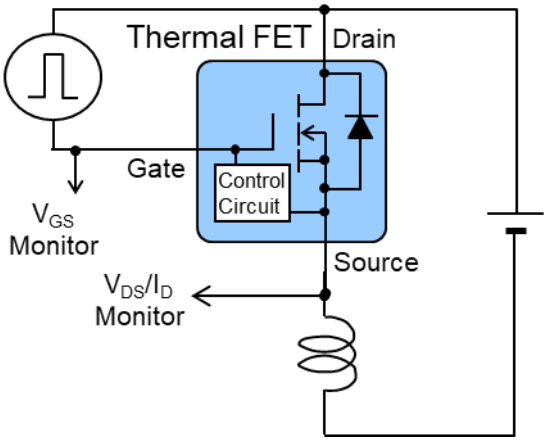


Fig. 4-6 Example of inductance load control circuit in high-side configuration

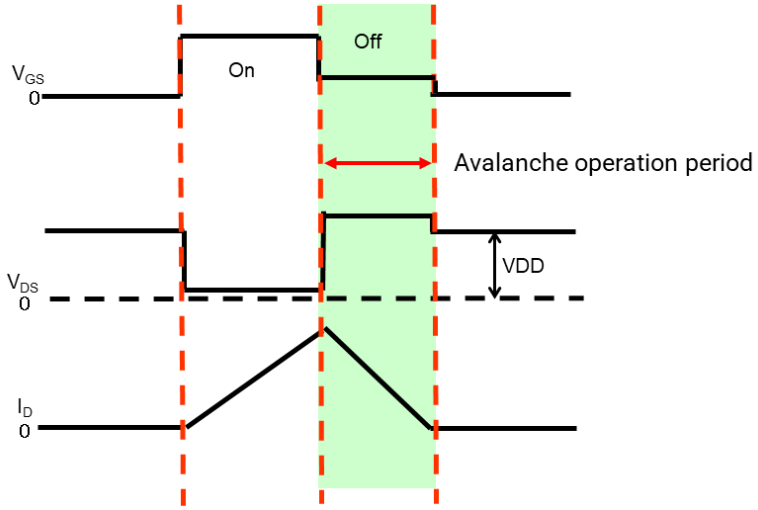


Fig. 4-7 Operating waveforms during avalanche operation

4.4 Precautions for reverse battery connection and use of built-in diode

A thermal FET has a similar built-in parasitic diode between the drain and source to a power MOSFET. Therefore, if the power supply such as a battery is connected in reverse, the thermal FET will generate heat because the current will flow from the source to the drain via the parasitic diode. However, this diode current can flow regardless of the gate control method, so even if the channel temperature in the chip reaches the cutoff start temperature and the overheat cutoff operation occurs, the current cannot be cut off.
Also, even if the customer expects the characteristics of the built-in parasitic diode to be used in a way that is not an abnormal mode (regenerative current arc extinguishing, etc.), the current that flows in the forward direction of the diode due to the original thermal FET cut-off operation for the above reason. cannot be blocked.

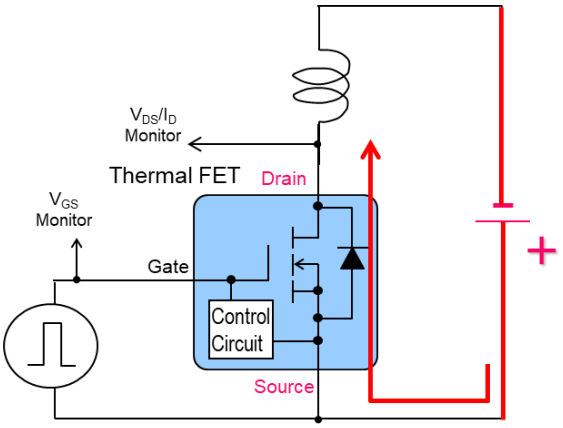


Fig. 4-8 Reverse battery connection.

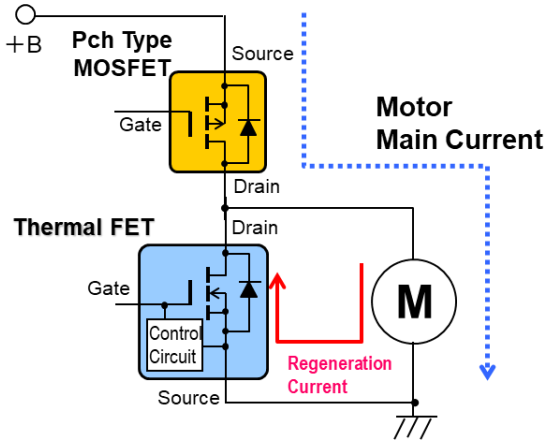


Fig. 4-9 Example of using regenerative current with a motor load.

4.5 Precautions for repeated use of overheat shutdown operation.

In the overheat shutdown operation caused by the load short circuit, the channel temperature in the chip becomes 150℃ or more, so if the operation leading to that state is repeated, the initial structure cannot be maintained because the chip is exposed to high temperature for a long time. It may disappear and destroy. Therefore, please consider not to design a system that expected to have active usage of cut-off operation due to load short circuit.

4.6 Precautions when exceeding Tch=150℃ or higher

In the event of system failure such as load short circuit, it has been set that the permissible limit number of load short circuits for each product. Please set the fail-safe function within this allowable number of times for safety design of the system.

Table 4-1 Load short circuit allowable limit number of times[Note.]

Product	Test condition	Allowable number of load short circuits
RJF0618JPE	VDD=16V, V_{GS}=5V, R_L=0, T_a=25℃, Independently implement	10k times

Note: For inquiries about individual products, please contact our sales representatives.

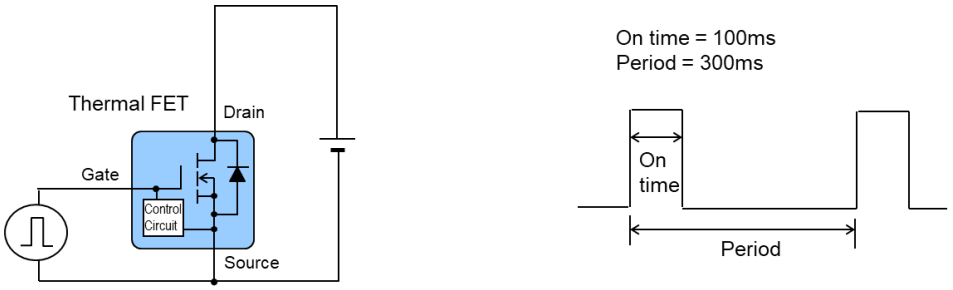
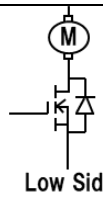
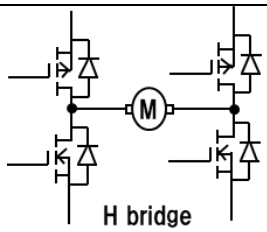
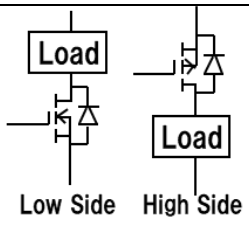
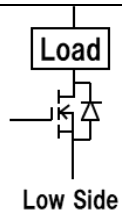
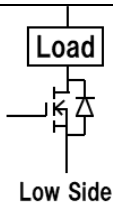


図 4-10 Load short-circuit test condition

5. Application

Table 5-1 Application example

Field	Use	Usage purpose	Usage example	Product Adoption
Vending Machine	Motor Drive	Preventing damage due to motor lock		HAF2026RJ
Farming Machine	Motor drive, Buzzer, Body control, Engine control	Short circuit protection		RJE0620JPD RJF0618JSP
Industrial Equipment	Power supply distribution switch, PLC, Various sensors	Short circuit protection		RJF0622JSP RJF0604JPD
Printer	Drawer Drive	Short circuit protection		RJF0610JSP
Amusement	Motor Drive	Short circuit protection		RJF0622JSP

Revision History

Rev.	Date	Description	
		Page	Summary
Rev.1.00	Feb-29.2024		Create a new entry

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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