Transitioning from RC210xxA (VersaClock) to RC2121xA (AutoClock)

This document describes how to design a PCB to support the transition from RC210xxA (RC21008A, RC21012A) VC7 devices to RC2121xA (RC21211A, RC21212A, RC21213A, RC21214A) AutoClock devices.

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1. Introduction

The RC21012A is a 48-pin VFQFPN VersaClock® 7 (VC7) clock generator developed primarily for data center applications. The device does not have FuSa features. The RC21211A and RC21212A are 48-pin VFQFPN AutoClock™ devices with added FuSa features. The 40-pin variants of each device (RC21008A [VC7], RC21213A, RC21214A [AutoClock]) are also referenced in this document.

2. Device Pinouts

2.1 48-Pin Devices

The RC210xxA VC7 and RC2121xA AutoClock are 48-pin VFQFPN devices with many pins in common. Figure 1 shows a mark-up of the device pin commonalities and differences between RC210xxA and RC2121xA.

Legend

- Black text: Common pins for both RC210xxA and RC2121xA devices
- Black with green text: Renamed pin for RC2121xA devices
- Red text with strikethrough: Previous pin name for RC210xxA devices
- Green text: New pin name for RC2121xA devices
- Red text: Renamed pin for RC2121xA devices
- Red with green text: Renamed pin for RC2121xA devices

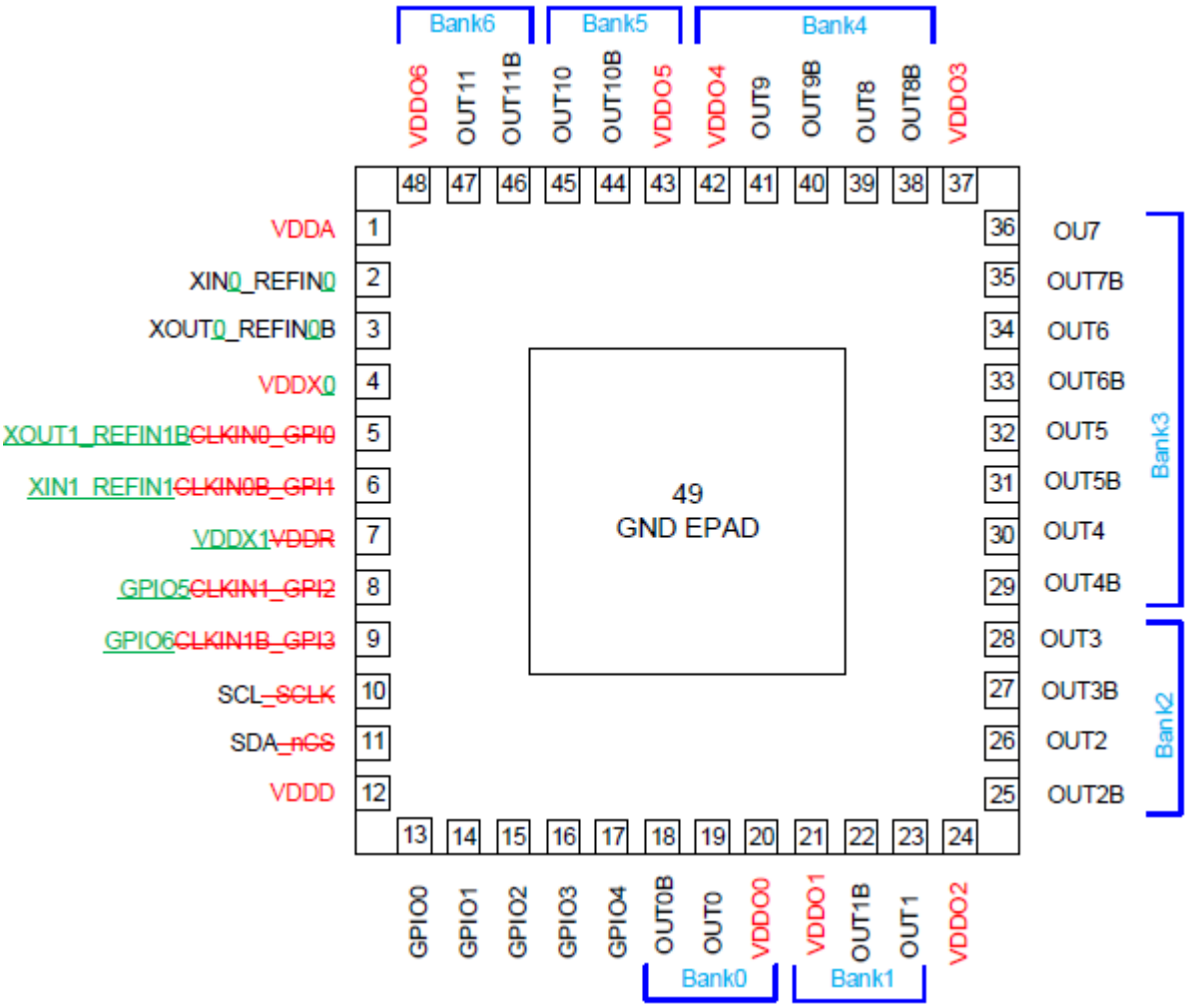

Figure 1. Pinout Differences between 48-VFQFPN RC210xxA and RC2121xA Devices

2.2 40-Pin Devices

The RC21008A and RC21213A/4A are 40-pin VFQFPN devices with many pins in common. Figure 2 shows a mark-up of the device pin commonalities and differences between RC21008A and RC21213A/4A.

Legend

- Black text: Common pins for both RC21008A and RC21213A/4A devices
- Black with green text: Renamed pin for RC21213A/4A devices
- Red text with strikethrough: Previous pin name for RC21008A devices
- Green text: New pin name for RC21213A/4A devices
- Red text: Renamed pin for RC2121xA devices
- Red with green text: Renamed pin for RC21213A/4A devices

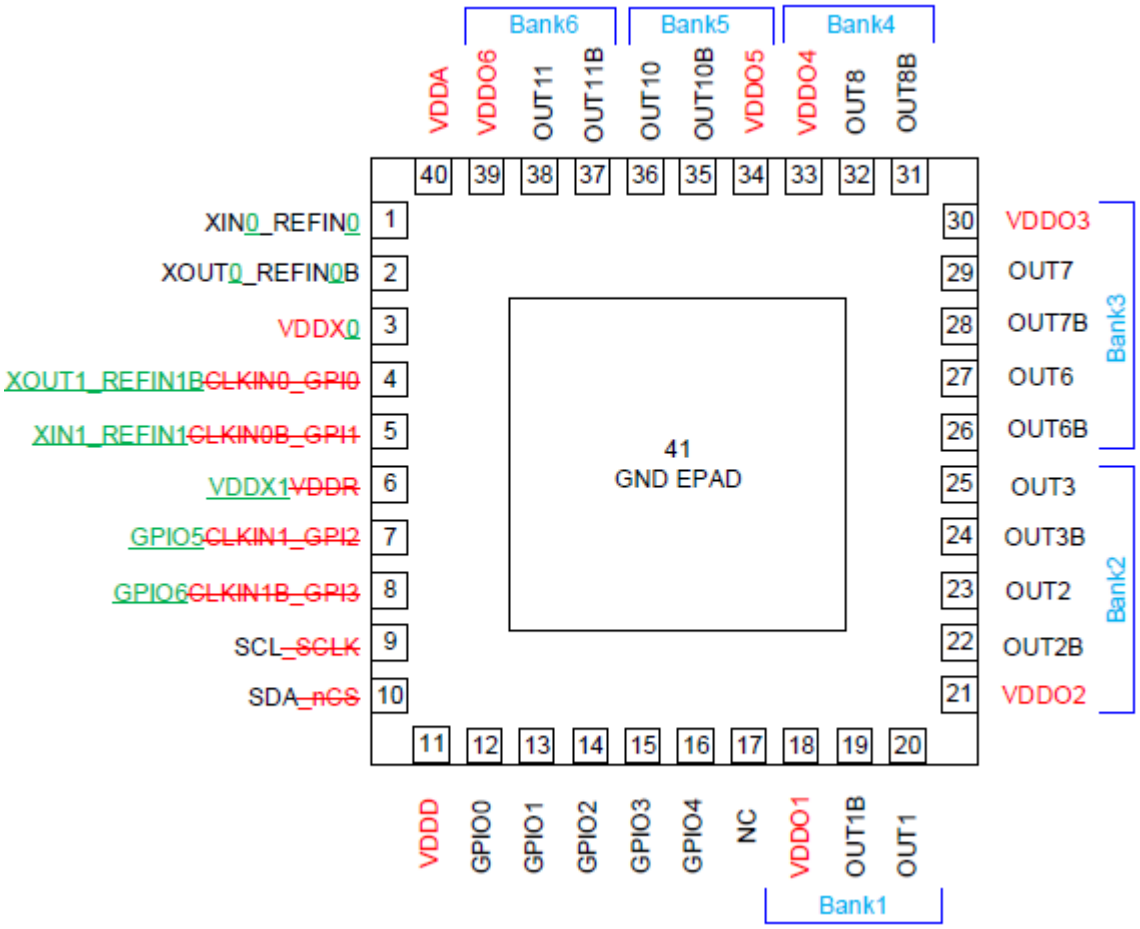

Figure 2. Pinout Differences between 40-VFQFPN RC21008A and RC21213A/4A Devices

3. I²C

I²C is associated with the SDA and SCL pins. The RC210xxA devices needed be configured to use I²C (not SPI). The RC2121xA devices implement I²C only on the SDA and SCL pins.

4. Backup Crystal

The XOUT1_REFIN1B and XIN1_REFIN1 pins of the following devices make use of a backup crystal.

- RC21012A/08A (VC7) must be configured as GPI with no function assigned; PCB may populate the crystal.
- RC21212A/4A (AutoClock) must be used as backup crystal pins.
- RC21211A/3A (AutoClock) may be used as GPI pins.

5. GPIO

GPIO[4:0] are common to both VC7 and AutoClock devices and must be used as OE (output enable) or SEL (select) as needed. OE can be configured in both devices to enable different outputs as needed. When multiple images are used, the SEL function is used to select which OTP image to load. The RC2121xA devices support up to four OTP images, therefore, no more than four images may be used. In addition, RC210xxA devices must use GPIO[2:0] for SEL.

GPIO[6:5] are new for RC2121xA devices and make use of new functions INT and FAULT.

- RC210xxA (VC7) devices must be configured as GPI with no function assigned.
- RC2121xA (AutoClock) devices must use the GPIO as INT and FAULT pins.

6. 3.3V Tolerant

3.3V tolerant is defined when powering the V_{DDD} pin at 1.8V and the GPIO pins being 3.3V tolerant, in other words, an input of 3.3V will not damage the input pad. When powering V_{DDD} at 3.3V, digital pins are always 3.3V tolerant.

- VC7 and AutoClock devices support 3.3V tolerant on I^2C (in other words, SDA and SCL pins)
- VC7 and AutoClock devices are not 3.3V tolerant on GPI pins
- RC210xxA VC7 devices GPIO pins are *not* 3.3V tolerant
- RC2121xA AutoClock devices GPIO[6:1] pins *are* 3.3 V tolerant
- RC2121xA AutoClock devices GPIO[0] pin is *not* 3.3 V tolerant.

Note: INT and FAULT GPIO[6:5] pins [9:8] are open drain and require an external pull-up.

7. INT and FAULT

Figure 3 shows the recommend schematic for INT and FAULT with input levels to SoC and PMIC being 3.3V. The INT and FAULT pins are open drain and require pull-ups.

- RC210xxA (VC7) does not support INT or FAULT and is *not* 3.3V tolerant
  - R1 = not populated
  - R2 = 10kΩ pull-up
- RC2121xA (AutoClock) supports INT and FAULT and is 3.3V tolerant
  - R1 = 0 ohms
  - R2 = 10kΩ pull-up

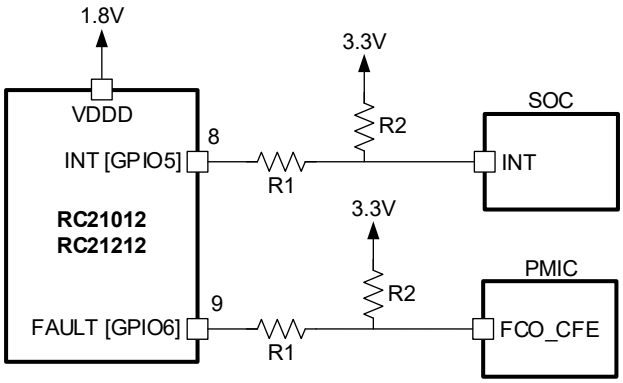

Figure 3. Interrupt and Fault Schematic

8. 1.2V LVCMOS

Some devices, (for example, UFS) require a 1.2V single-ended clock input. Figure 4 shows VDDO6 is supplied with 1.8V. R2 is either populated, or not to drop voltage at destination, and assumes a 50Ω impedance.

- RC210xxA (VC7) supports 1.8V single-ended
  - R1 = 33Ω, source-series termination
  - R2 = 100Ω, destination termination to reduce voltage from 1.8V to 1.2V
- ▪ RC2121xA (AutoClock) supports 1.2V single-ended.
  - • R1 = 33Ω, source-series termination
  - • R2 = not populated

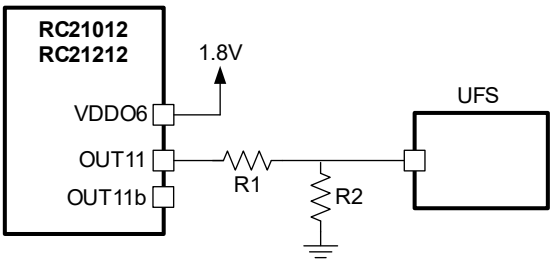

Figure 4. 1.2V LVCMOS Schematic

9. LP-HCSL Termination

LP-HCSL is series-terminated with 50Ω to match the transmission line (see Figure 5). Other output types use the same termination.

- RC210xxA (VC7) has internal termination of 50Ω
  - R1 = 0 ohms
- RC2121xA (AutoClock) requires external termination when using output clock monitoring
  - R1 = 33Ω combined with the internal source impedance of 17Ω; total is 50Ω

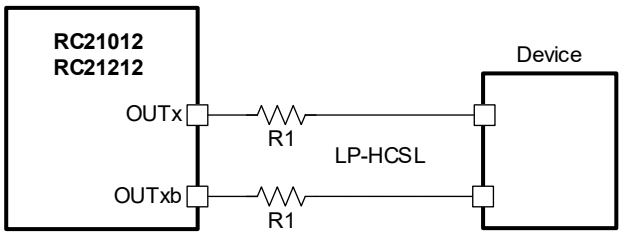

Figure 5. LP-HCSL Termination

10. Revision History

Revision	Date	Description
1.00	Apr 22, 2024	Initial release.

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